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SCR MANUAL

SECOND EDITION

Silicon Controlled Rectifier Manual

SECOND EDITION

SILICON CONTROLLED RECTIFIER MANUAL

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FOREWORD

The First Edition of the General Electric Controlled Rectifier Manual has unquestionably been a determining factor in the rapid and world-wide acceptance of the SCR as a major power control component. New applications of the SCR have been many and diverse, and the learning curve has been steep. Within the brief year and a half since the publication of the First Edition, much additional information has been gained on the SCR, its characteristics, and its uses. New SCR types with uniquely useful characteristics and ratings have been developed. Circuit designs have been refined and in many cases reduced in complexity and cost. Circuit design criteria are more precise and easy to use. The Second Edition of the General Electric SCR Manual incorporates these improvements in its 109 additional pages. I sincerely hope this Manual will prove useful and informative to you.

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This manual is dedicated to General Electric engineer
Gordon N. Hall
who developed and fabricated the first commercial
Silicon Controlled Rectifier

AN INTRODUCTION TO THE SILICON CONTROLLED RECTIFIER

Since 1957, when General Electric introduced the Silicon Controlled Rectifier (SCR), this unique component has carved a niche for itself in military, industrial, commercial and residential applications. In hundreds of different jobs it has replaced:

> Thyratrons . . . Relays . . . Magnetic Amplifiers and Saturable Reactors . . . Contactors . . . Variable Autotransformers . . . Fuses . . . Timers . . . Rheostats . . . Vacuum Tubes . . . Power Transistors.

But more important than the replacing of existing components, the SCR has made possible many new products hitherto unfeasible, among them ultra-high-speed protective devices and lightweight, compact power controls.

In *military applications* the SCR has played a key role in power and control circuitry, in satellites, guided missiles, and aircraft of many types. Its jobs have ranged from explosive squib firing to shipboard power conversion. The extremely high reliability and compactness of the SCR have also made it a particularly useful device for automatic checkout and ground support equipment, where unquestioned performance for many years is essential. To meet the needs of United States armed services, General Electric has been the first to qualify an SCR to a military specification, MIL-S-19500/108.

Industrial and commercial applications were among the first uses of the SCR. It has been used in the motor speed control circuits of continuous flow paper mill drives since 1959 and has given excellent performance in this sensitive role where short interruptions may cost thousands of dollars. The SCR has also been widely used in automated machinery as a relay replacement, as well as in remote control gas turbine supervisory equipment. Thousands of SCR's have been used to dim studio lighting in major TV studios and theaters and many more thousands have been used in industrial power circuits throughout the country.

Now volume production and the resulting price reductions have brought General Electric SCR prices down to a level where it can do hundreds of new jobs more reliably, at less cost and with simpler circuitry. For example,

> —Striking decorative affects can be obtained with the new home lamp dimmers using General Electric SCR's. A 300 to 500 watt dimmer suitable for the average living room is small enough to fit in a standard wall switch enclosure without expensive alteration.
>
> —Small power tools can do their jobs better, and faster, using new low cost SCR motor speed controls.

The SCR has gained an enviable reputation for operating reliability and new low prices have greatly increased the applications where it can help the job at hand. Small wonder that thousands of people inside and outside of the electronic industry are now investigating the SCR for many new jobs. With this introduction we at General Electric welcome you to the study of this fascinating device. Perhaps the simplest approach is to discuss just what the SCR *is* and *isn't*.

The SCR *is* a semiconductor—a rectifier—a latching static switch capable

of operating in microseconds—and a sensitive amplifier. It *isn't* an overgrown transistor, as it has far greater power capabilities, both voltage and current, under continuous and surge conditions.

As a *silicon semiconductor*—the SCR is compact, static, capable of being hermetically sealed, silent in operation and free from the effects of vibration and shock. A properly designed and fabricated SCR has no inherent failure mechanism. When properly chosen and protected, it will have virtually limitless operating life even in harsh atmospheres. Thus countless billions of operations can be expected, with complete safety, even in explosive environments.

As a *rectifier*—the SCR will conduct current in only one direction. But this serves as an advantage when the load requires DC, for here the SCR serves both to control *and* rectify.

As a *latching switch*—the SCR is an ON-OFF Switch, unlike the vacuum tube or transistor which are basically variable resistances (even though they too can be used as on-off switches). The SCR can be turned on by a momentary application of control current to the gate (as short as a fraction of a microsecond will do), while tubes or transistors (and the basic relay) require a continuous ON signal. In short the SCR *latches* into conduction, providing an inherent memory useful for many functions. The SCR can be turned ON in 1 to 4 microseconds, and OFF in 10 to 20 microseconds.

Just as a switch or relay contact is commonly rated in terms of the current it can safely carry and interrupt, as well as the voltage at which it is capable of operating, the SCR is rated in terms of peak voltage and forward current. General Electric offers a complete family of SCR's with current carrying capacities from ½ amp to 110 amps DC, and up to 500 volts at this writing. (See Frontispiece). Higher voltage and current loads are readily handled by series and parallel connection of SCR's.

As an *amplifier*—the smallest General Electric SCR's can be latched into conduction with control signals of only a few microwatts and a few microseconds duration. These SCR's are capable of switching up to 400 watts. The resulting control power gain of approximately 100 million makes the small SCR one of the most sensitive control devices available. With a low cost unijunction transistor firing circuit driving the larger SCR's (Chapter 4) stable turn-on control power gains of many billions are completely practical.

This extraordinary control gain makes possible inexpensive control circuits using very low level signals, such as produced by Thermistors, Cadmium Sulfide light sensitive resistors, and other transducers.

The material in this Manual elaborates further on the SCR and some of its main circuit applications. The illustrated circuits are intended as a starting point for the equipment designer in achieving the detailed requirements of his application. Since these circuits are not necessarily "ultimate" for every application, it is hoped the imaginative designer will use them simply as a jumping-off point for his own development. Likewise, many of these circuits can be used for many other functions besides those specifically mentioned in the text. As a guide to some of the various SCR circuits for accomplishing specific tasks, the Application Index on page 341 has been formulated.

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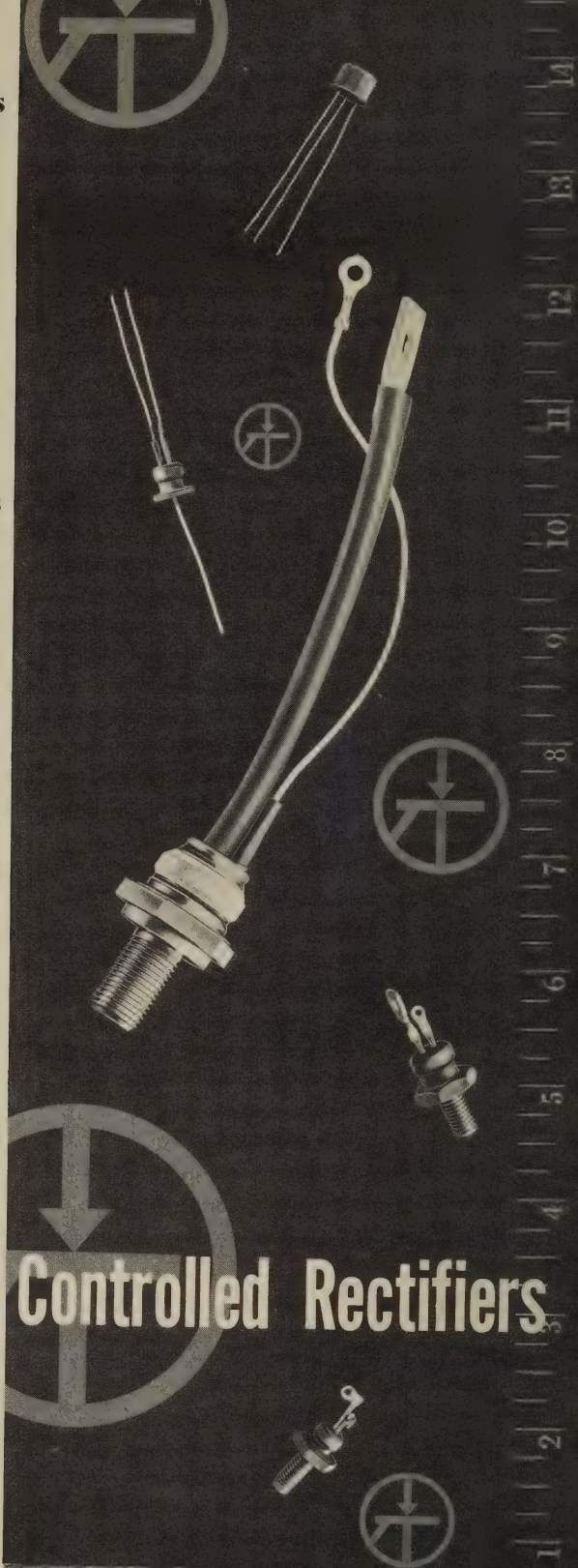
1.6 AMPS

1.1 AMPS

110 AMPS

25 AMPS

7 AMPS



Silicon Controlled Rectifiers

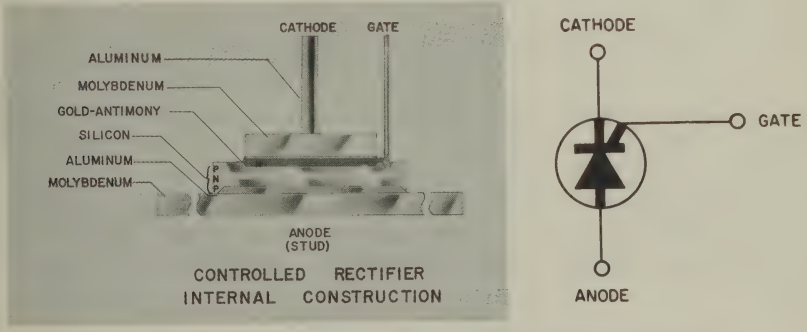
CHAPTER 1

CONSTRUCTION AND BASIC THEORY OF OPERATION

1.1 SCR CONSTRUCTION

The successful and reliable operation of an SCR depends to a large extent on the design and fabrication of the SCR itself. The heart of the SCR is the disc of four alternate layers of N and P type silicon that gives the SCR its unique electrical characteristics. The layers and junctions between them are formed by precision gaseous diffusion and alloying techniques.

In order to protect the fragile silicon junctions against thermal and mechanical stresses, the silicon disc is brazed between substantial plates of molybdenum or tungsten as shown typically in Figure 1.1. These plates have the same coefficient of expansion as silicon. In small SCR's which are lead mounted, the bottom backup plate acts as the base of the housing enclosure. In larger SCR's (roughly above 1 ampere) the bottom plate is soldered to a copper stud which acts as the anode terminal and a thermal path for the SCR's heat losses to the outside ambient. For this reason the stud is usually screwed to a cooling fin of some kind.



Typical Controlled Rectifier Internal Construction and Circuit Symbol
Figure 1.1

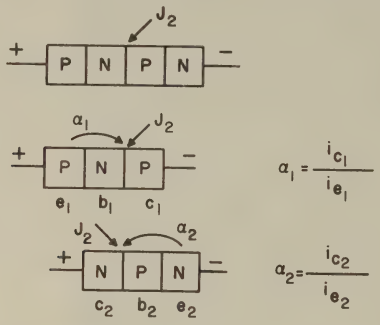
In General Electric's higher rated SCR's, particularly those designed for high junction temperature operation, special high temperature hard solders are used to attach the NPNP-tungsten sandwich to the copper stud and to the cathode terminal in order to minimize any possibility of thermal fatigue of these joints under the stresses of cyclical loads.

The entire SCR assembly is fabricated in a super-clean environment to assure long term stability of the SCR's electrical characteristics. To maintain the stability of these characteristics throughout the long life of the SCR, the finished assembly is sealed off from the outside atmosphere by welded hermetic seals. All electrical connections are also made by resistance welding. Extensive

electrical and mechanical tests at room temperature and both extremes of the operating temperature range assure that the individual SCR's meet their specification sheet ratings and characteristics. Cycled life tests on significant samples continuously monitor and control the long-term reliability of SCR's coming off the production line.

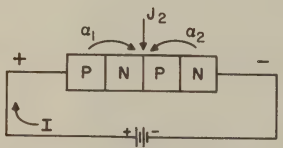
1.2 TWO TRANSISTOR ANALOGY TO SCR OPERATION

The operation of an NPNP structure can best be understood with reference to Figure 1.2. An NPNP structure may be considered to consist of a PNP and an NPN transistor with a common collector junction. The PNP section of the bar



Two Transistor Analogy of NPNP Structure
Figure 1.2

as indicated at the center of Figure 1.2 has an α_1 which defines the fraction of hole current injected at emitter 1 that reaches collector 1. The NPN structure on the bottom of Figure 1.2 has an α_2 which defines the fraction of electron current injected at emitter 2 which reaches collector 2. By combining these two structures as in Figure 1.3, the total current flowing in an NPNP structure can be pictured as the sum of the current flowing in the individual transistor sections.



$$I_{J_2} = I\alpha_1 + I\alpha_2 + I_{CO}$$

I_{CO} ← (LEAKAGE CURRENT)

$I\alpha_2$ ← (ELECTRON CURRENT FROM END N REGION)

$I\alpha_1$ ← (HOLE CURRENT FROM END P REGION)

$$\text{SINCE } I_{J_2} = I, \quad I = \frac{I_{CO}}{1-\alpha_1-\alpha_2}$$

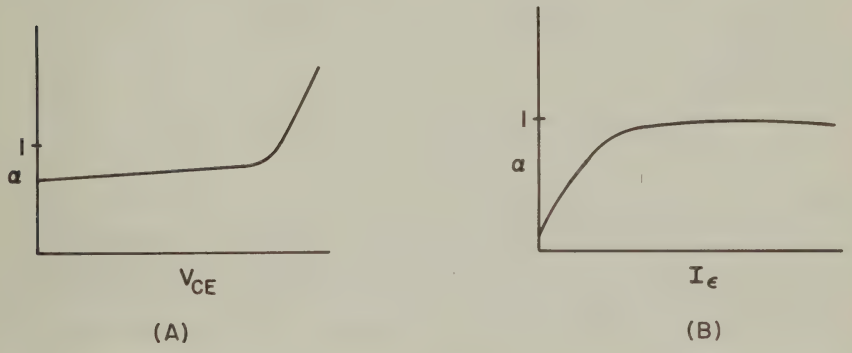
Approximate Expression for Currents Flowing in SCR
Figure 1.3

The current crossing junction J_2 consists of three components: $I\alpha_1$, the hole current from the P end region; $I\alpha_2$, the electron current from the N end region; and I_{CO}, the leakage current. Since the total current at junction J_2 must be equal to the external current I, a slight rearrangement will show that the external current is given by:

$$I = \frac{I_{CO}}{1 - \alpha_1 - \alpha_2}$$

From the above equation, it is obvious that if $\alpha_1 + \alpha_2$ is equal to 0.9, then the current flowing will be equal to the leakage current multiplied by a factor of ten. Since the leakage current in a silicon PN junction can be made very small, the total current flowing will also be very small and this corresponds to the "off" condition of the SCR. If $\alpha_1 + \alpha_2$ is nearly unity, however, the denominator is almost zero and the current is limited only by the external circuit. This corresponds to the "on" condition of the SCR. Physically, in the "on" condition, the two center regions of the SCR are saturated with carriers, making all three junctions have forward biases. Hence, the entire potential drop across the SCR is about that of one forward biased PN rectifier.

There are two mechanisms which may be employed for increasing the alphas of the component junction transistors in order to turn-on an SCR. Figure 1.4 illustrates these two mechanisms.

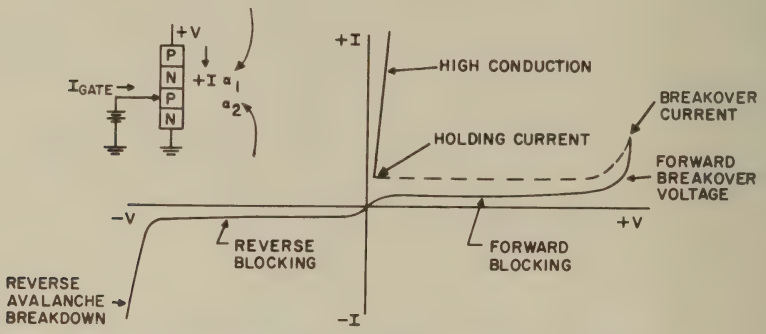


Variation of α with V_{CE} and Emitter Current
Figure 1.4

The current gain, α, increases slightly as the collector to emitter voltage is increased until a voltage is reached where the energy of carriers arriving at the collector P-N boundary is sufficient to dislodge additional carriers producing a form of avalanche breakdown analogous to a Townsend discharge in gases. This causes an increase in α with voltage as indicated in Figure 1.4(A). In most typical silicon transistors, α is quite low at low emitter currents, but increases fairly rapidly as the emitter current is increased. This effect (Fig. 1.4B) is due to the presence in the silicon of special impurity centers. Both methods for increasing α may be used to turn-on the SCR; the former by increasing the anode-cathode voltage, the latter by introduction of current at one of the bases (transistor action).

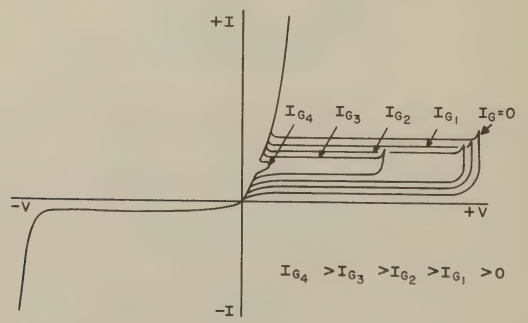
1.3 V-I CHARACTERISTICS

Figure 1.5 illustrates the typical V-I characteristics of an SCR and the various regions of operation. In the forward blocking region, increasing the forward voltage does not tend to increase current until the point is reached where avalanche multiplication begins to take place. Past this point, the current increases quite rapidly until the total current through the device is sufficient to maintain the sum of the α's ≥ 1 (Figure 1.4A). At this point the SCR will go into the high conduction region, provided that the current through the device remains greater than a minimum value called the holding current. If the current through the device ever drops below the holding current, the SCR will revert to the forward blocking region. In the reverse direction, the SCR has essentially two back-biased PN junctions in series so that it exhibits characteristics very similar to ordinary back-biased silicon rectifiers.



Typical SCR Electrical Characteristics ($I_{GATE} = 0$)
Figure 1.5

For increasing magnitudes of gate current, the region of characteristics between breakover current and holding current (Fig. 1.6) is narrowed and the forward breakover voltage reduced. For sufficiently high gate currents, the entire forward blocking region is removed, and the V-I characteristics of an SCR are essentially identical to those of a PN rectifier. This is shown in Figure 1.6.



Effect of Increasing Gate Currents on SCR Characteristics
Figure 1.6

In typical operation the SCR is biased well below the forward breakover voltage, and triggering is accomplished by injecting current into the gate lead. As can be seen in Fig. 1.6, injecting current into the gate lead increases the current flowing through the device (by transistor action), thereby increasing both alphas, as alpha is current sensitive. This is a very advantageous mode of operation, both from the circuit design and reliability standpoint, since it is then possible to use a forward breakdown voltage much higher than any that will be normally encountered in the circuit and use only a moderate amount of trigger power to start the high conduction mode of operation. Once the gate has triggered the SCR into the high conduction mode, it no longer has any control over the device and the only method of turning off the SCR is to reduce the main current below the holding current level.

Since forward leakage current through the SCR in its blocking state increases with temperature, the forward breakover voltage will generally be quite sensitive to junction temperature also. At a high enough temperature (well above its maximum rating) the SCR loses its ability to block forward voltage as the forward leakage current acts similar to gate current in raising the alphas of the SCR.

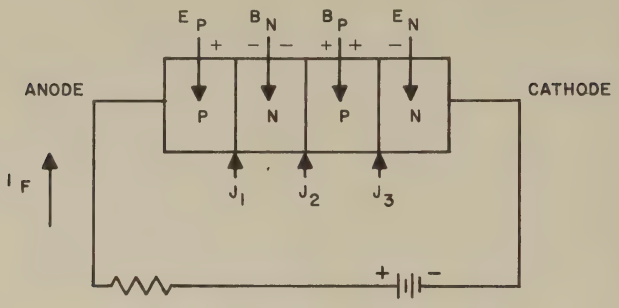
In smaller SCR's, this temperature effect on the breakover voltage can be minimized by extracting the forward leakage current from the gate. This prevents this current from passing through the emitter of the NPN section of the SCR, and maintains a low alpha in this section. It is also possible to actually increase the forward breakover voltage point on some small SCR's by this means. The effect of negative gate current on the forward blocking characteristics, however, becomes negligible on higher current SCR's due to the ineffectiveness of the gate in removing leakage current from the entire broad area of the NPN base.

As might be expected, the gate-cathode V-I characteristics of an SCR are essentially those of a forward biased PN junction diode. Since the increase in α with current is utilized, the SCR is a current triggered device as opposed to a voltage triggered device like a gas thyratron. This distinction must be kept in mind when designing firing circuits in that a low impedance voltage source or a current source must be used for triggering the SCR.

1.4 TURN-OFF MECHANISM

When the SCR is in the conducting state, each of the three junctions of Figure 1.7 are in a condition of forward bias and the two base regions (B_P, B_N) are heavily saturated with holes and electrons (stored charge).

To turn-off the SCR in a minimum time, it is necessary to apply a reverse voltage. When this reverse voltage is applied the holes and electrons in the vicinity of the two end junctions (J_1, J_3) will diffuse to these junctions and result in a reverse current in the external circuit. The voltage across the SCR will remain at about +0.7 volts as long as an appreciable reverse current flows. After the holes and electrons in the vicinity of J_1 and J_3 have been removed,



Silicon Controlled Rectifier Biased in Conducting State (Gate Open Circuited) Figure 1.7

the reverse current will cease and the junctions J_1 and J_3 will assume a blocking state. The reverse voltage across the SCR will then increase to a value determined by the external circuit. Recovery of the SCR is not complete, however, since a high concentration of holes and electrons would still exist in the vicinity of the center junction (J_2). This concentration decreases by the process of recombination in a manner which is largely independent of the external bias conditions. After the hole and electron concentration at J_2 has decreased to a low value, J_2 will regain its blocking state and a forward voltage (less than V_{BO}) may be applied to the SCR without causing it to turn-on.

1.5 COMPARISON WITH OTHER SEMICONDUCTORS

It will be noted that the low current alphas of the PNP and NPN parts of the SCR must be low in order to have the device block in the forward direction. In an ordinary three layer silicon power transistor, it is desirable to have alpha as close to unity as possible in order to achieve a high current gain. Unfortunately, however, high alphas are obtained in most silicon transistors by using very thin base regions, and a thin base between two low resistivity regions is incompatible with high voltage. The wide base regions in the SCR, necessary to achieve low alphas, are compatible with high voltages so that the SCR is inherently a higher voltage device. The use of wide base regions is also an advantage from the standpoint of ease of manufacture and reproducibility of characteristics. An advantage of the SCR over power transistors is the amount of drive necessary to full conduction. In many silicon power transistors, it is necessary to inject up to half an ampere of base current in order to conduct 5 amps. from collector to emitter. In an SCR, the amount of current conducted is dependent only on the external circuit once the device has been triggered. Thus a trigger current of 50 ma is all that is necessary to allow conduction of any current from 0.1 to hundreds of amperes. The high current capabilities of the SCR, as contrasted to a transistor, are due to more effective use of junction area for current conduction.

CHAPTER 2

DEFINITION OF TERMS USED IN SCR SPECIFICATIONS

2.1 SCR RATINGS

The following tabulation defines the terminology used in SCR specifications. This terminology is closely allied to that used in describing semiconductor diode rectifiers. Certain additions are necessary to adequately describe a switching device with gate control characteristics.

Ratings are limiting values assigned by the manufacturer, which, if exceeded, may result in permanent impairment of device performance or life.

Terminology	*Symbol*	*Definition*
Repetitive Peak Reverse Voltage (Cyclical Peak Reverse Voltage)	PRV PIV	Maximum allowable instantaneous value of repetitive reverse (negative) voltage that may be applied to the SCR anode with the gate open. Voltage may be applied as a sine wave but it does not necessarily mean a continuous DC rating which is defined separately below. While this value of PRV does not represent a "breakdown" voltage, it should never be exceeded except by the transient rating if the device has such a rating.
Transient Peak Reverse Voltage	$PRV_{trans.}$ $PIV_{trans.}$	Maximum allowable instantaneous value of reverse (negative) voltage that may be applied on a non-recurrent basis to the SCR anode with gate open for the duration and conditions specified.
RMS Reverse Voltage	V_{RMS}	Maximum allowable RMS value of a full cycle sine wave which may be applied to anode when working into resistive or inductive load and with gate open.
Continuous Reverse DC (or Blocking) Voltage	V_{RDC}	Maximum allowable reverse (negative) voltage which may be applied to the SCR anode on a continuous basis. If this DC reverse voltage is applied immediately after forward conduction, other limitations may apply.

Definition of Terms Used in SCR Specifications

Terminology	*Symbol*	*Definition*
Peak Forward Blocking Voltage	PFV	Maximum instantaneous value of forward blocking voltage which may be applied to anode. If anode breakover occurs at voltage above this limit, the SCR may be damaged. If anode breakover occurs at a voltage lower than the PFV, no damage to the SCR will result.
Average Forward Current	I_F	Maximum continuous DC current which may be allowed to flow in the forward direction (from anode to cathode) under stated conditions of frequency, temperature, and reverse voltage. It is the average value of current when working in a single phase circuit feeding a resistive or inductive load with no firing angle delay. A derating factor is usually applied for other conditions such as three-phase operation or capacitive loading.
RMS Forward Current	I_{RMS}	Maximum continuous RMS current which may be allowed to flow in the forward direction under stated conditions. "Average forward current" rating above applies simultaneously.
Peak One Cycle Surge (or Fault) Current	I_{surge}	Peak one cycle surge. Maximum allowable non-recurrent (100-500 times in life of SCR) peak current of a single forward cycle (8.3 milliseconds duration) in a 60 cps single phase resistive load system. The surge may be preceded and followed by maximum rated voltage, current, and junction temperature conditions, and maximum allowable gate power may be concurrently dissipated. However, specified limitations on anode current during switching should not be exceeded.
I - squared t	I^2t	This is a measure of maximum forward non-recurring (100-500 times in life of SCR) overcurrent capability for very short pulse durations (8.3 milliseconds or less, unless otherwise specified). I is in RMS amperes, and t is pulse duration in seconds. The same conditions as listed above for I_{surge} apply.

Terminology	*Symbol*	*Definition*
Gate Power Dissipation	P_G	Power dissipation between gate and cathode terminals.

2.2 SCR CHARACTERISTICS

Characteristics are measurable properties or attributes of a device which are inherent to its design.

Breakover Voltage	V_{BO}	The value of positive anode voltage at which an SCR switches into the conductive state with gate circuit open.
Forward Current	i_F	Instantaneous value of anode current flowing into SCR.
Forward Voltage Drop	v_F	Instantaneous voltage drop between anode and cathode during conduction of current from anode to cathode with gate open.
Full Cycle Average Forward Voltage Drop	$V_{F\ Avg.}$	Forward voltage drop averaged over one complete cycle with maximum allowable continuous DC output current flowing in a 60 cps single phase half wave rectifier with resistive load and no firing angle delay.
Gate Current	i_g	Instantaneous current flowing between gate and cathode.
Gate Voltage	v_g	Instantaneous voltage between gate and cathode with anode open.
Gate Current for Firing	I_{GF}	Gate current required to fire an SCR with anode at +6 volts with respect to cathode and with device at stated temperature conditions.
Gate Voltage for Firing	V_{GF}	Gate voltage with I_{GF} flowing but prior to start of anode conduction.
Holding Current	I_H	Value of i_F below which SCR returns to forward blocking state after having been in forward conduction. Gate open.
Forward Saturation (or Leakage Current)	i_S	Instantaneous anode current at stated conditions of forward blocking voltage and junction temperature. Gate open.
Reverse Leakage Current	i_R	Instantaneous anode current at stated conditions of negative anode voltage and junction temperature. Gate open.

Definition of Terms Used in SCR Specifications

Terminology	*Symbol*	*Definition*
Full Cycle Average Leakage Current	$I_{S\ Avg.}$ $I_{R\ Avg.}$	For polarity indicated by subscript, leakage current averaged over one complete cycle at specified voltage and temperature in a 60 cps sinusoidal single phase half wave circuit with resistive load.
Delay Time	t_d	Time interval between initiation of gate current signal and reduction of forward voltage to 90% of blocking value during switching to conduction under stated conditions.
Rise Time	t_r	Time interval required for forward voltage to decrease from 90% to 10% of blocking value during switching to conduction under stated conditions.
Turn-off Time	t_o	Time interval required for gate to regain control of forward blocking characteristic after forward conduction under stated circuit and temperature conditions.
Steady-State Thermal Resistance	R_T	Steady-state temperature rise per unit power dissipation of the junction above the temperature of the external reference point. For stud-mounted cells, R_T is expressed in °C/watt between junction and the bottom face of the stud.
Transient Thermal Resistance	r_T	Apparent thermal resistance defining temperature rise per unit power dissipation of junction above reference point for specified period of time after application of step function of heat to junction previously at equilibrium with ambient. (See Section 3.4.)

CHAPTER 3

RATINGS AND CHARACTERISTICS OF SILICON CONTROLLED RECTIFIERS

3.1 JUNCTION TEMPERATURE

The operating junction temperature range of SCR's varies for the individual types. A low temperature limit may be required to limit stress in the silicon crystal to safe values. This type of stress is due to the difference in the thermal coefficients of expansion of the materials used in fabricating the cell subassembly. The upper operating temperature limit is imposed because of the temperature dependence of V_{BO}, the forward breakover voltage, and because of thermal stability considerations. The upper storage temperature limit in some cases may be higher than the operating limit. It is selected to achieve optimum reliability and stability of characteristics with time.

Methods for determining the load current carrying limits of SCR's limit the peak temperature reached by the junction to a value not exceeding the maximum operating temperature. (Exception is taken for non-recurrent phenomena of very short duration, such as fault currents during an accidental short circuit.) The rating methods for continuous and recurrent loads assume uniform temperature across the entire semiconductor junction area. Since there are three junctions in an SCR, a composite temperature as indicated by the variation in anode to cathode forward voltage drop with temperature is used as a means of defining junction temperature.

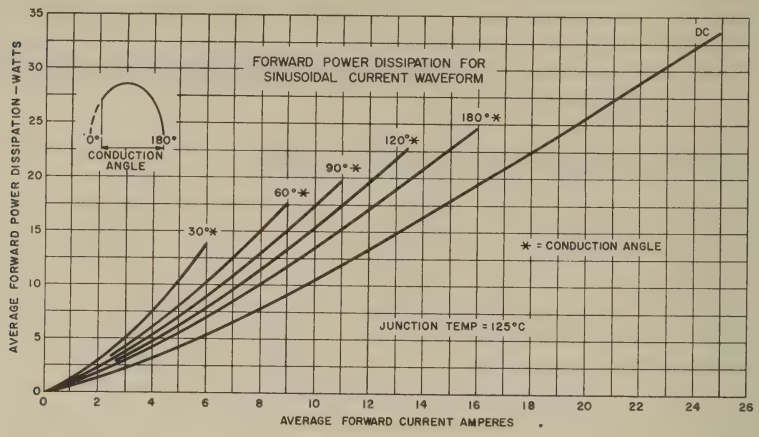
3.2 POWER LOSSES

Heat is generated in the junction region by electrical losses that may be classified into five types:

a. Forward voltage drop during load current conduction.
b. Forward leakage current during forward blocking.
c. Reverse leakage current during reverse blocking.
d. Losses in the gate circuit due to firing signal.
e. Losses occurring during switching.

Forward conduction losses are the major source of junction heating for normal duty cycles and power frequencies. Figure 3.1 gives forward conduction loss in watts for the 2N681 SCR as a function of average current in amperes for various conduction angles. This type of information is given on the specification sheet for each type of SCR. These curves are based on a current waveform which is the remainder of a half-sine wave which results when delayed angle firing is used in a single phase resistive load circuit. They are conservative for rectangular current waveforms with the same average value and conduction angle. These power curves are the integrated product of the instantaneous anode current and forward voltage drop. This integration can be performed

graphically or analytically for conduction angles other than those listed, using the forward voltage-current characteristic curves for the specific device.



Average Forward Power Dissipation
For 2N681 Series SCR
Figure 3.1

Both the forward and reverse blocking losses are determined by integration of the appropriate blocking E-I curves on the specification sheet.

Gate losses are negligible for pulse types of firing signals. Losses may become more significant for gate signals with a high duty cycle, or for SCR's in a TO-5 or smaller package.

The losses may be calculated from the gate E-I curves shown on the Firing Characteristics for the specific type of SCR. Highest gate dissipation will occur for an SCR whose gate characteristics intersect the gate circuit load line at its mid-point. For a more detailed discussion of the gate characteristic and its load line, see Chapter 4.

Switching losses, both turn-on and turn-off, are discussed in Section 3.6.6.

3.3 THERMAL RESISTANCE

The heat developed at the junctions by the foregoing power losses flows into the stud and thence to the heatsink. The junction temperature rises above the stud temperature in direct proportion to the amount of heat flowing from the junction and the thermal resistance of the device to the flow of heat. The following equation defines the relationship under steady-state conditions:

$$T_J - T_S = PR_T \tag{3.1}$$

where T_J = average junction temperature, °C

T_S = stud temperature, °C

P = average heat generation at junction, watts

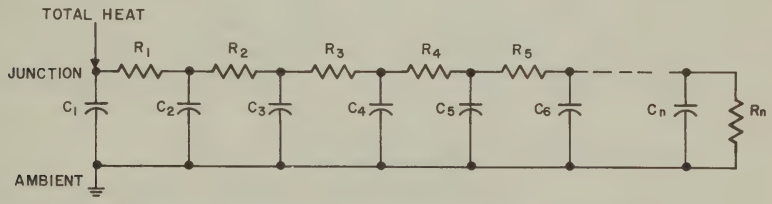
R_T = steady-state thermal resistance between junctions and bottom face of stud, °C/watt

Equation 3.1 can be used to determine the allowable power dissipation and thus the continuous pure DC forward current rating of an SCR for a given stud temperature through use of the forward E-I curves. For this purpose, T_J is the maximum allowable junction temperature for the specific device. The maximum values of R_T and T_J are given in the specifications.

3.4 TRANSIENT THERMAL RESISTANCE

Equation 3.1 is not satisfactory for finding the peak junction temperature when the heat is applied in pulses such as the recurrent conduction periods in an AC circuit. Solution of Equation 3.1 using the peak value of P is over-conservative in limiting the junction temperature rise. On the other hand, using the average value of P over a full cycle will underestimate the peak temperature of the junction. The reason for this discrepancy lies in the thermal capacity of the semiconductor, that is, its characteristic of requiring time to heat up, and its ability to store heat.

Compared to other electrical components such as transformers and motors, semiconductors have a relatively low thermal capacity, particularly in the immediate vicinity of the junction. As a result, devices like the SCR heat up very quickly upon application of load, and the temperature of the junction may fluctuate during the course of a cycle of power frequency. Yet, for very short overloads this relatively low thermal capacity may be significant in arresting the rapid rise of junction temperature. In addition, the heatsink to which the semiconductor is attached may have a thermal time constant of many minutes. Both of these effects can be used to good advantage in securing attractive intermittent and pulse ratings sometimes well in excess of the published continuous DC ratings for a device.



Simplified Equivalent Thermal Circuit for SCR
Figure 3.2

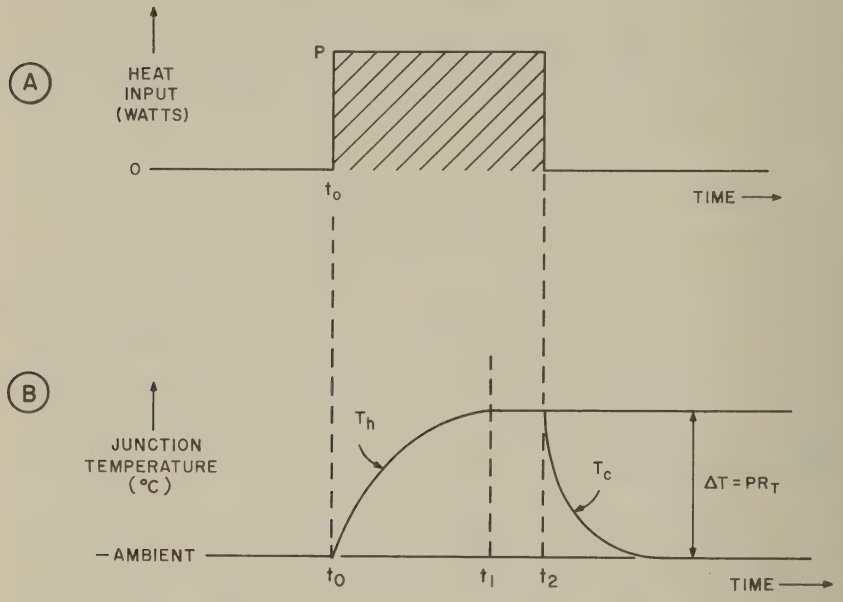
The thermal circuit of the SCR can be simplified to that shown in Figure 3.2. This is an equivalent network emanating in one direction from the junctions and with the total heat losses being introduced at the junctions only. This simplification is valid for current amplitudes at which I^2R losses are small in comparison with the junction losses. In Figure 3.2 the ambient is the reference level. If a stud type device is mounted to an infinite heatsink, the heatsink temperature can be used as a reference.

When a step pulse of heating power P is introduced at the junctions of the SCR (and of the thermal circuit) as shown in Figure 3.3A, the junction temperature will rise at a rate dependent upon the response of the thermal

network. This is represented by the curve T_h in Figure 3.3B. After some sufficiently long time t_1, the junction temperature will stabilize at a point $\Delta T = PR_T$ above the ambient (or stud) temperature. This is the same as Equation 3.1. R_T is the sum of R_1 through R_n in the equivalent thermal circuit of Figure 3.2.

If the power input is terminated at time t_2 after the junction temperature has stabilized, the junction temperature will return to ambient along the locus indicated by T_c in Figure 3.3B. It can be shown that curves T_h and T_c are conjugates of one another, that is,

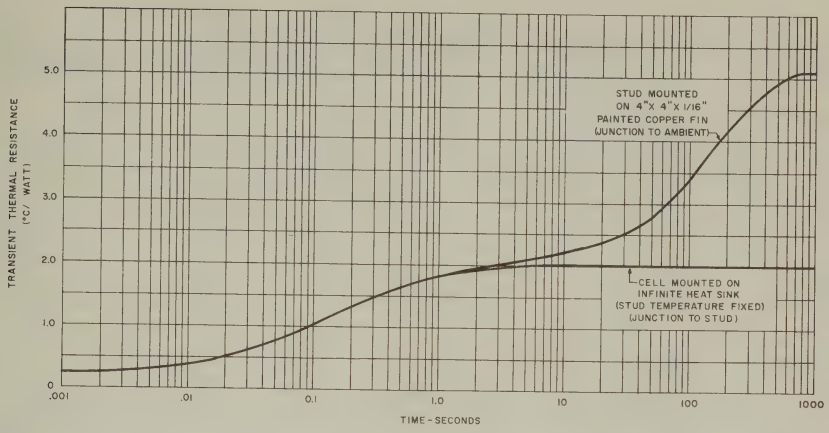
$$T_c = \Delta T - T_h = PR_T - T_h \tag{3.2}$$



Response for SCR Junction to Step Pulse of Heating Power
Figure 3.3

By dividing the instantaneous temperature rise of curve T_h in Figure 3.3B by the power P causing the rise, the dimensions of the ordinate can be converted from °C to °C/watt. This latter set of dimensions is that of thermal resistance, or as it is more precisely termed: the transient thermal resistance r_T. Figure 3.4 shows a plot of transient thermal resistance for the 2N681 SCR both when mounted to an infinite heatsink and to a four-inch square copper fin.

Transient thermal resistance information for a device can be obtained by monitoring junction temperature at the end of a well-defined power pulse or after a known steady-state load has been removed. Junction temperature is measured by use of one of the temperature-sensitive junction characteristics such as forward voltage drop at low currents. Conversion of heating data to cooling data, or vice versa, can be accomplished through the use of Equation 3.2.



Transient Thermal Resistance of 2N681 SCR
Figure 3.4

So that the transient thermal resistance curve can be used with confidence in equipment designs, the curve represents the highest values of thermal resistance for each time interval on the curve that can be expected from the manufacturing distribution of the products. An additional slight safety factor is included to provide conservative application under all types of repetitive pulse loads.

The transient thermal resistance curve approaches asymptotic values at both the long time and short time extremes. For very long time intervals the transient thermal resistance approaches the steady-state thermal resistance, R_T.

For times less than 1 millisecond the value at 1 millisecond may be extrapolated by $1/\sqrt{t}$. For example, the 2N681 transient thermal resistance at 10 μseconds may be estimated as $0.2/\sqrt{10^{-3}/10^{-5}} = 0.02°C/W$. It is not suggested to extrapolate below 10 μseconds. For maximum utilization of semiconductor devices in the microsecond region additional factors must be considered and other methods of rating and life testing must be used.

3.5.1 BASIC LOAD CURRENT RATING EQUATIONS

In order for a device to be properly applied for recurrent load duty its maximum allowable peak operating junction temperature must not be exceeded. By knowing the dissipation of a semiconductor device and its thermal response it is possible to meet this requirement.

The information given on the G-E specification sheet, in conjunction with the proper equation in Figure 3.5, allows the designer to calculate power semiconductor ratings for a variety of conditions.*

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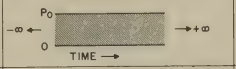
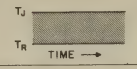
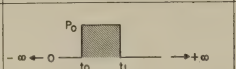
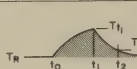
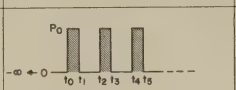
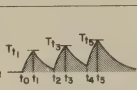
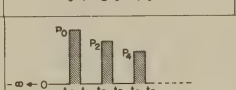
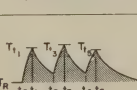
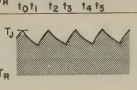
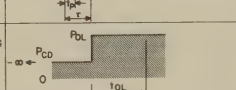
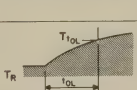
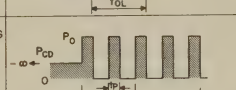
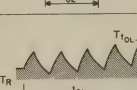
*For detailed development and discussion of these equations, write for Application Note 200.9, "Power Semiconductor Ratings Under Transient and Intermittent Loads."

LOAD CONDITION	WAVEFORM OF POWER LOSS AT JUNCTION	WAVEFORM OF JUNCTION TEMPERATURE RISE (T_R = REFERENCE TEMP.)	SOLUTION FOR JUNCTION TEMPERATURE AND POWER LOSS R_T = STEADY-STATE THERMAL RESISTANCE r_{t_1} = TRANSIENT THERMAL RESISTANCE AT TIME t_1 $r_{(t_2-t_1)}$ = TRANSIENT THERMAL RESISTANCE AT TIME (t_2-t_1), ETC.
NTINUOUS LOAD			$T_J - T_R = P_O R_T$ $P_O = \frac{T_J - T_R}{R_T}$
NGLE LOAD PULSE			$T_{t_1} - T_R = P_O r_{t_1}$ $T_{t_2} - T_R = P_O \left[r_{t_2} - r_{(t_2-t_1)} \right]$ $P_O = \frac{T_{t_1} - T_R}{r_{t_1}}$
ORT TRAIN OF AD PULSES QUAL AMPLITUDE)			$T_{t_1} - T_R = P_O r_{t_1}$ $T_{t_3} - T_R = P_O \left[r_{t_3} - r_{(t_3-t_1)} + r_{(t_3-t_2)} \right]$ $T_{t_5} - T_R = P_O \left[r_{t_5} - r_{(t_5-t_1)} + r_{(t_5-t_2)} - r_{(t_5-t_3)} + r_{(t_5-t_4)} \right]$ ETC.
RAIN OF UNEQUAL MPLITUDE OAD PULSES			$T_{t_1} - T_R = P_O r_{t_1}$ $T_{t_3} - T_R = P_O r_{t_3} - P_O r_{(t_3-t_1)} + P_2 r_{(t_3-t_2)}$ $T_{t_5} - T_R = P_O r_{t_5} - P_O r_{(t_5-t_1)} + P_2 r_{(t_5-t_2)} - P_2 r_{(t_5-t_3)} + P_4 r_{(t_5-t_4)}$
ONG TRAIN OF QUAL AMPLITUDE OAD PULSES APPROX SOLUTION)			$T_J - T_R = P_O \left[\frac{t_p R_T}{\tau} + \left(1 - \frac{t_p}{\tau}\right) r_{(\tau+t_p)} - r_{(\tau)} + r_{(t_p)} \right]$ $P_O = \frac{T_J - T_R}{\frac{t_p R_T}{\tau} + \left(1 - \frac{t_p}{\tau}\right) r_{(\tau+t_p)} - r_{(\tau)} + r_{(t_p)}}$
VERLOAD FOLLOWING ONTINUOUS DUTY NON-PULSED)			$T_{t_{OL}} - T_R = P_{CD} R_T + (P_{OL} - P_{CD}) r_{t_{OL}}$ $P_{OL} = \frac{T_{t_{OL}} - T_R - P_{CD} R_T}{r_{t_{OL}}} + P_{CD}$
VERLOAD FOLLOWING ONTINUOUS DUTY PULSED) APPROX SOLUTION)			$T_{t_{OL}} - T_R = P_{CD} R_T + P_O \left\{ \left[\frac{t_p}{\tau} - \frac{P_{CD}}{P_O} \right] r_{(t_{OL})} + \left(1 - \frac{t_p}{\tau}\right) r_{(\tau+t_p)} - r_{(\tau)} + r_{(t_p)} \right\}$ $P_O = \frac{T_{t_{OL}} - T_R - P_{CD} R_T}{\left[\frac{t_p}{\tau} - \frac{P_{CD}}{P_O} \right] r_{(t_{OL})} + \left(1 - \frac{t_p}{\tau}\right) r_{(\tau+t_p)} - r_{(\tau)} + r_{(t_p)}}$

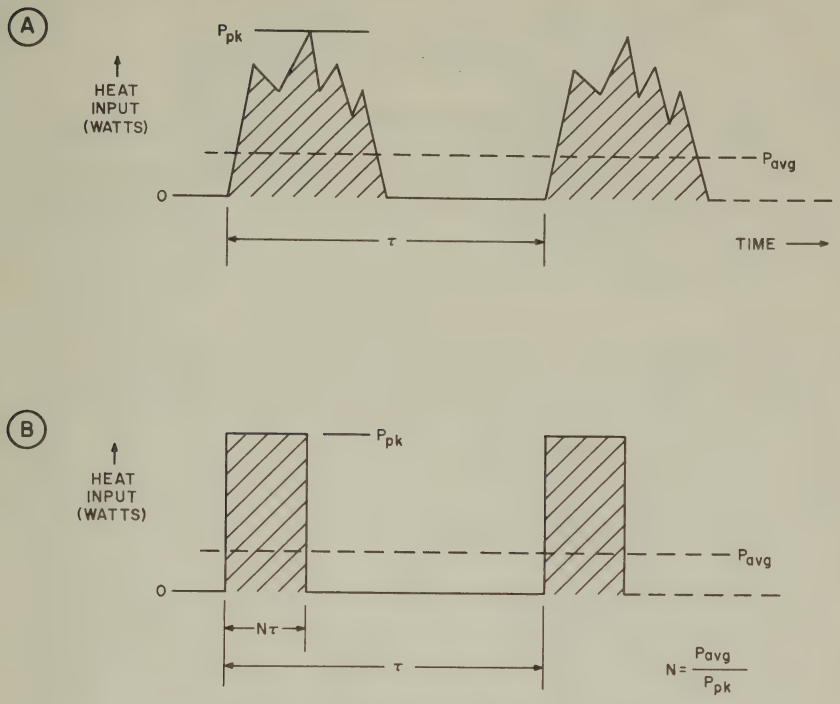
Basic Load Current Rating Equations
Figure 3.5

3.5.2 TREATMENT OF IRREGULARLY SHAPED POWER PULSES — APPROXIMATE METHOD

In the preceding section solutions for junction temperature were given in response to step functions of power input. In many practical applications, the power pulse is not of this ideal shape for computation, and appropriate approximations must be made to convert the actual waveshape into a rectangular form if the subsequent calculations are to be made as outlined.

Figure 3.6A illustrates the arbitrary waveshape of a power pulse that reoccurs at a period of τ seconds and has a peak value of P_{pk} watts and a full-cycle average of P_{avg} watts. For the purpose of calculating peak junction temperatures, this waveshape can be approximated by the rectangular waveshape of Figure 3.6B. This rectangular waveshape is selected to have the identical values of peak power P_{pk} and average power P_{avg} as Figure 3.6A by altering the pulse duration by a constant N to maintain the peak to average relationship. N is defined as the ratio of P_{avg} to P_{pk}.

This translation into rectangular pulses of power ensures a "worst case" approximation since a rectangular pulse of power will always have an effect on temperature rise which is equal to or greater than the effect of any other pulse

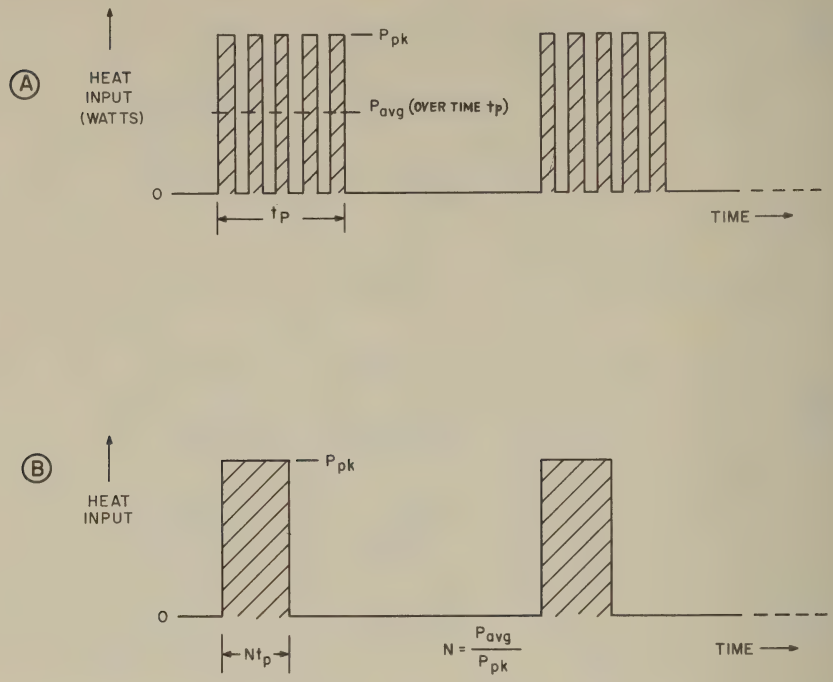


Approximating Irregularly Shaped Heating Pulse with Rectangular Waveshape
Figure 3.6

having the same peak and average power. In other words, a rectangular power pulse will raise the junction temperature higher than any other waveshape with the same peak and average values since it concentrates its heating effects into a shorter period of time, thus minimizing cooling during the pulse.

Figure 3.7A illustrates a case where a similar type of approximation can be used to shorten the calculations for peak junction temperature when the problem would otherwise be too laborious. It involves the case where a sequence of power pulses is periodically interrupted by a longer "off" period of zero power. This is typical of any repetitive or cyclical on-off type of load. Each burst of pulses can be represented by a single square-wave with introduction of only a relatively small error. This error will always yield a junction temperature higher than actual, and will thus provide a conservative application. In the equivalent waveshape shown in Figure 3.7B, the peak value of power P_{pk} is maintained the same as in Figure 3.7A. The duration of the equivalent rectangular waveshape is reduced to Nt_P where N is defined as P_{avg}/P_{pk}.

Sample Problem: Half wave sinusoidal current flows through a 2N681 SCR at 60 cps. The full cycle average value of this current is 10 amperes. Approximate the heating effect of a sequence of four cycles of current by a single rectangular wave of power.



Approximating Bursts of Pulses with Single Rectangular Pulse of Power
Figure 3.7

Solution:

$$I_{peak} = \pi I_{avg} = 10\pi = 31.4 \text{ amperes}$$

V_{peak} = 1.8 volts at 31.4 amps from published specifications on 2N681

$$P_{peak} = I_{peak} \times V_{peak} = 31.4 \times 1.8 = 56.5 \text{ watts}$$

Full cycle average P = 13.7 watts at 10 amps average current from published specifications on 2N681

P_{avg} over 3½ cycles (actual duration of heating) $= 13.7 \times \frac{4}{3\frac{1}{2}} = 15.6$ watts

$$N = P_{avg}/P_{peak} = 15.6/56.5 = 0.28$$

$$t = 3.5 \text{ cycles} \times 1/60 \text{ cps} = .0585 \text{ second}$$

$$Nt = 0.28 \times .0585 = 0.0163 \text{ second}$$

Thus the heating effect of the four cycles of current can be approximated by a single rectangular pulse of power with amplitude of 56.5 watts and a duration of 0.0163 second. This is a conservative approximation.

3.5.3 THE EFFECT OF HEATSINK DESIGN ON THE TRANSIENT THERMAL RESISTANCE CURVE

Since the heatsink is a major component in the heat transfer path between junction and ambient, its design affects the transient thermal resistance curve (Figure 3.4) substantially. When a semiconductor is manufactured and shipped to the user in a stud-mounted version, the manufacturer has no control over the ultimate heatsink and can only provide data on the heat transfer system between junction and stud, which is the part he manufactured. This type of data is presented in Figure 3.4 as the "Cell Mounted to Infinite Heatsink" curve.

The equipment designer can use this curve in developing a transient thermal resistance curve for the cell when mounted to a particular heatsink of his own design by means of a few simple calculations. These calculations assume that the temperature throughout the heatsink is uniform even under transient loading, thus permitting the heatsink to be represented by a single time constant. This is a good assumption for fins of relatively thick cross-section and fin effectiveness close to unity. This approach also assumes that the thermal capacity of the heatsink is large compared to the thermal capacity of the cell. By adding the calculated (or measured) transient thermal resistance of the fin to the "Infinite Heatsink" curve for the cell, the applicable curve can be plotted for the complete thermal system. The method can best be explained through an example illustrating how the second curve on Figure 3.4 (4" x 4" fin) can be calculated.

3.5.4 EXAMPLE OF CALCULATING THE TRANSIENT THERMAL RESISTANCE CURVE FOR A SPECIFIC HEATSINK DESIGN

Problem: A cell is mounted on a painted copper fin 1/16" thick and 4" on a side. The fin is subjected to free convection air conditions. Find the transient thermal resistance curve for a device mounted on this fin if the infinite heatsink curve in Figure 3.4 represents the thermal characteristics of the stud-mounted semiconductor. Assume that the stud to fin contact resistance is negligible.

Solution: From fin design curves (See Chapter 11):

$h_r = .005$ watt/inch^2 °C $\qquad h_c = .005$ watt/inch^2 °C

$h_{total} = h_r + h_c = .010$ watt/inch^2 °C

Fin thermal conductance $k = h \times A = .01 \times 4 \times 4$ inches$^2 \times 2$ sides $=$ 0.32 watt/°C

Fin thermal resistance $R_F = \frac{1}{k} = \frac{1}{0.32} = 3.1$ °C/watt

$$\text{Fin thermal capacity } C = c\rho V = \frac{175 \text{ watt-seconds}}{\text{lb}^\circ\text{C}} \times 0.32 \text{ lb/in}^3$$
$$\times 4 \text{ in} \times 4 \text{ in} \times 1/16 \text{ in} = \frac{56 \text{ watt-seconds}}{^\circ\text{C}}$$

$$\text{Thermal RC time constant} = 3.1^\circ\text{C/watt} \times \frac{56 \text{ watt-seconds}}{^\circ\text{C}} = 174 \text{ seconds}$$

Equation of transient fin thermal resistance, r_F:

$$r_F = R_F (1 - e^{-t/RC}) = 3.1 (1 - e^{-t/174})$$

The values of r_F are added to the infinite heatsink curve to secure the overall r_T of the system as indicated in Figure 3.4. Note that this fin has negligible resistance at periods of time one second or less after application of power. In this area, it behaves like an infinite heatsink which has no resistive element. The fin and the entire thermal system reach equilibrium around 1000 seconds. Thereafter the thermal capacity is no longer effective in holding down the junction temperature.

3.6.1 RECURRENT AND NON-RECURRENT CURRENT RATINGS

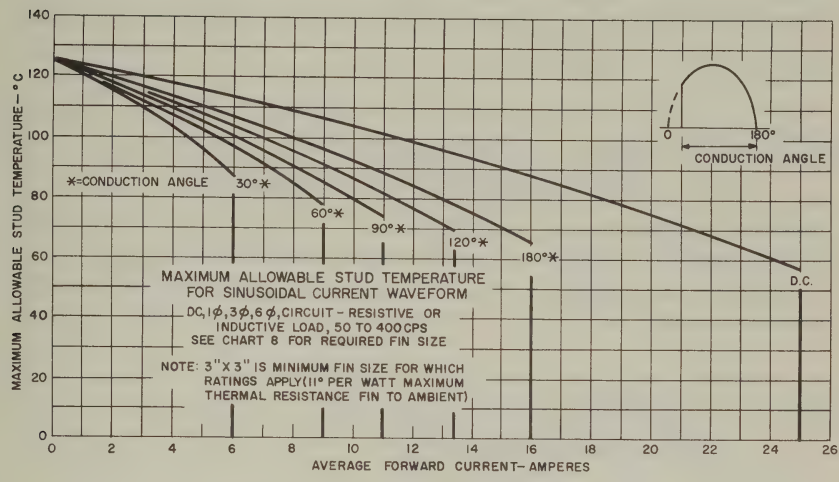
When a semiconductor device is applied in such a manner that its maximum allowable peak junction temperature is not exceeded at any time the device is applied on a *recurrent* basis. Any condition that is a normal and repeated part of the application or equipment in which the semiconductor device is used must meet this condition if the device is to be applied on a recurrent basis. The foregoing sections on intermittent duty give methods of checking peak junction temperature which enable the designer to properly apply the device on a recurrent duty basis.

A class of ratings that makes the SCR truly a power semiconductor are the *non-recurrent* current ratings. These ratings allow the maximum (recurrent) operating junction temperature of the device to be exceeded for a brief instant. This gives the device an instantaneous overcurrent capability allowing it to be coordinated with circuit protective devices. The specification bulletin gives these ratings in terms of surge current and I^2t. These ratings, then, should only be used to accommodate unusual circuit conditions not normally a part of the application, such as fault currents. Non-recurrent ratings are understood to apply to load conditions that will not occur more than a limited number of times in the course of the operating life of the equipment in which the SCR is finding application. For most SCR's this number of times is in the order of from one hundred to several hundred. Operation beyond this point may lead to a permanent degradation of the device's characteristics.

3.6.2 AVERAGE CURRENT RATING (RECURRENT)

This is perhaps the most basic of current ratings. It is shown in the specification sheet as for the 2N681 series SCR in Figure 3.8. These curves specify the maximum allowable average anode current ratings of the SCR as a function

of stud temperature and conduction angle. Points on these curves are selected so that the junction temperature under the stated conditions does not exceed the maximum allowable value. The maximum rated junction temperature of the 2N681 SCR is 125°C.



Maximum Average Current Ratings
for 2N681 Series SCR
Figure 3.8

The curves of Figure 3.8 include the effects of the small contribution to total dissipation by reverse blocking, gate drive, and switching. For devices which are lead mounted or housed in small packages, like the TO-5 or TO-18, the forward current rating may be substantially affected by gate drive dissipation. Where this becomes important it is so indicated on the specification sheet.

If the 2N681 in a single phase resistive load circuit is fired as soon as its anode swings positive, the device will conduct for 180 degrees. If the stud temperature is maintained at 80°C or less, the 2N681 is capable of handling 13 amperes average current as indicated in Figure 3.8. If the firing angle is retarded by 120 degrees, the 2N681 will conduct for only the 60 remaining degrees of the half cycle. Under these conditions, the maximum rated average current at 80°C stud temperature is 8.7 amperes, substantially less than for 180 degrees conduction angle.

3.6.3 RMS CURRENT (RECURRENT)

It will be noted in Figure 3.8 that the curves for the various conduction waveshapes have definite end points. These points represent identical RMS values and as such give a rating implicit in the curves of Figure 3.8.

For example, the 2N681 is rated 25 amperes DC or $\frac{25}{1.57} = 16$ amperes average in a half-wave, or 180° conduction angle, circuit. The factor 1.57 is the form factor giving the ratio of RMS to average values for a sinusoidal waveform. By the definition of RMS values, the RMS and average values are iden-

tical for a direct current. The RMS current rating, as shown on the specification sheet for individual SCR's, is necessary to prevent excessive heating in resistive elements of the SCR, such as joints, leads, etc.

The RMS current rating can be of importance when applying semiconductors to high peak current, low duty cycle waveforms. Although the average value of the waveform may be well within the ratings, it may be that the allowable RMS rating is being exceeded.

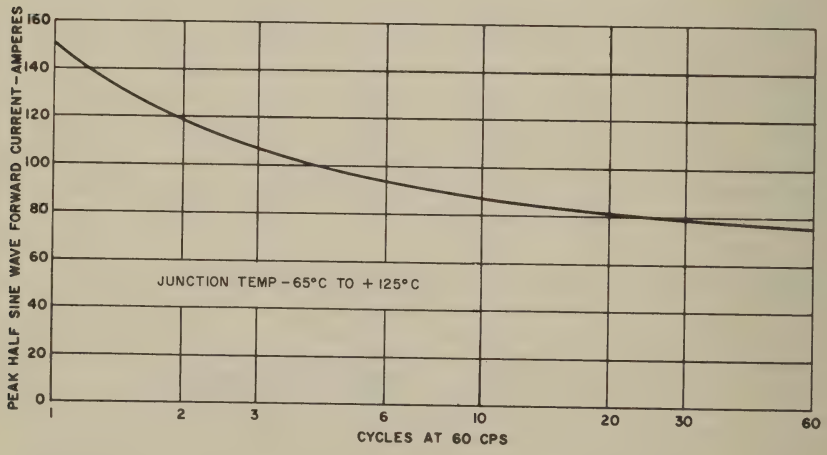
3.6.4 ARBITRARY CURRENT WAVESHAPES AND OVERLOADS (RECURRENT)

Recurrent application of arbitrary waveshapes, varying duty cycles, and overloads requires that the maximum peak allowable junction temperature of the SCR not be exceeded at any time. Sections 3.5.1 through 3.5.4 give information for determining this.

3.6.5 SURGE AND I^2t RATINGS (NON-RECURRENT)

In the event that a type of overload or short circuit can be classified as non-recurrent, the rated junction temperature can be exceeded for a brief instant, thereby allowing additional overcurrent rating. Ratings for this type of non-recurrent duty are given by the Surge Current curve and by the I^2t rating.

Figure 3.9 shows the maximum allowable non-recurrent surge current at rated load conditions. Note that the junction temperature is assumed to be at its maximum rated value (125°C for the 2N681); it is therefore apparent that the junction temperature will exceed its rated value for a short time.



Maximum Allowable Non-Recurrent Surge Current at Rated Load Conditions for 2N681 Series SCR
Figure 3.9

The data shown in this curve are values of peak rectified sinusoidal waveforms on a 60 cycles per second basis in a half-wave circuit. The "one cycle" point therefore gives an allowable non-recurrent half sine wave of 0.00834 seconds duration (half period of 60 cycle frequency) of a peak amplitude of 150 amperes. The "20 cycle" point shows that 20 rectified half sine waves are permissible (separated by equal "off" times), *each* of an *equal* amplitude of 80 amperes.

I^2t ratings apply for non-recurrent overloads shorter than one cycle. For such times the SCR behaves essentially like a resistance with a fixed thermal capacity and no power dissipating means, and displays a current capability which can be expressed as a constant I^2t, where I is the RMS value of current over an interval t. The I^2t rating of the SCR is given in the specifications. This rating assumes that the SCR is already in the conducting state. If the SCR is turned on into a fault, the fault current must be kept below the peak allowable switching current specification for the first 3 or 4 microseconds to prevent excessive switching power dissipation from destroying the cell. Section 3.6.6 deals with switching losses.

Provided the above precautions are observed, fault and overcurrent protection can be approached in the same manner as for power diode rectifiers. Protection methods are discussed in Chapter 11.

3.6.6 OPERATING FREQUENCY OF SCR AND SWITCHING LOSSES

The frequency response of the SCR is given basically by its turn-on time and its turn-off time. In practice, however, the required duty cycle, the nature of the circuit, and the required waveform also enter the picture. Chapter 5 discusses these matters in detail.

Turn-on time is generally in the order of 1 to 3 microseconds and turn-off time is typically in the order of 7 to 20 microseconds, depending on the SCR type and the current level being turned off. Since turn-off time is usually larger than turn-on time it is the limiting consideration when desiring highest frequency for a given duty cycle. Special inverter types of SCR's are available having low and guaranteed turn-off times.

The current rating curves, such as Figure 3.8, are valid over a range of 50 to 400 cps. For higher frequencies it becomes necessary to take the increase in switching dissipation into account. Equations with which to do this are available for the particular SCR being considered. For example, for the 2N681 series SCR the following stud temperature derating equation applies:

$$\Delta T = 1.30\, f\, V_M\, I_M \cdot 10^{-6} \qquad (3.3)$$

where ΔT = Stud temperature derating in °C

f = Operating frequency in cps

V_M = Instantaneous anode voltage immediately prior to switching

I_M = Instantaneous anode current immediately after switching

As the SCR switches into a conducting state, its peak current during the turn-on interval must be limited to a value such that the peak energy dissipa-

tion is held within the capability of the junction. The instantaneous heating of the junctions as determined by the product of the instantaneous current and the voltage across the SCR is very high if inductance in the anode circuit is low enough so as not to retard the build-up of current through the SCR. The energy dissipated at the junction of an SCR during a single switching action can be approximated by equation 3.4. This is a more general form of equation 3.3 and can also be used to estimate reverse recovery dissipation.

$$W = \frac{V_M I_M t_r}{4.6} \text{ watt-seconds} \tag{3.4}$$

where V_M = anode voltage immediately prior to switching

I_M = anode current immediately after switching

t_r = time in seconds for voltage across SCR to fall from 90% to 10%. (See Chapter 4.)

The average heating in watts due to switching action may be calculated by multiplying equation 3.4 by the frequency in cycles per second.

The specification sheet also gives values of peak recurrent current during the turn-on interval (switching current) which should not be exceeded. It is often more convenient to refer to these values directly rather than to calculate the losses. For example, the 2N681 SCR when switching 100 volts should have its recurrent turn-on current limited to 300 amperes; at 400 volts it should be limited to 65 amperes.

A method of limiting switching dissipation in the SCR is to use a small series connected saturable reactor. The SCR will initially be blocking forward voltage. As gate drive is applied to the SCR, the voltage will transfer to the small saturable reactor. Upon reaching core saturation the voltage will be applied to the load. As load current builds up through the SCR it will do so with the SCR in a low impedance forward conducting state. Thus the junction dissipation will be at a minimum.

Reverse recovery dissipation is generally much less than the turn-on energy due to the usually shorter reverse recovery time. However, its magnitude may be estimated by the use of equation 3.4 by letting V_M be the voltage across the SCR immediately after recovery, I_M the peak reverse recovery current, and t_r the time for the reverse voltage across the SCR to build up from 10% to 90% of the value immediately following recovery.

3.7.1 VOLTAGE RATINGS

The voltage rating of SCR's is designated by the suffix letter in the model number of the device (e.g., C35B) or by its JEDEC number. The designation is translated in the specifications and defines the continuous peak voltage which the device will withstand in both the forward and reverse directions without breaking down. It is applicable to any junction temperature within the specified operating range. This symmetry of forward and reverse voltage ratings is characteristic of all standard SCR's today. The following discusses each voltage rating in more detail.

3.7.2 PEAK REVERSE VOLTAGE (PRV)— REPETITIVE AND TRANSIENT

In the reverse direction, the SCR behaves like a conventional silicon diode rectifier. The device has a PRV rating and is able to withstand transient overvoltage as listed in General Electric specifications. However, if these ratings are substantially exceeded the device will go into avalanche breakdown. If reverse current under this condition is not limited to low values, the device will destroy itself. Where transient reverse voltages are excessive, additional PRV margin may be built into the circuit by inserting a diode rectifier of equivalent current rating in series with the controlled rectifier to assist it in handling inverse voltage. For a detailed discussion on voltage transients, see Chapter 12.

A specified minimum heatsink is required for the device to meet its maximum PRV rating. The reverse stability criterion of a semiconductor rectifier requires that the *total* junction-to-ambient thermal resistance be kept below a critical maximum value. (Ref. 2)

3.7.3 FORWARD BREAKOVER VOLTAGE (V_{BO})

The minimum forward breakover voltage is given on the specification bulletin at maximum allowable junction temperature (worst case) and for open gate conditions (worst case) unless specifically mentioned otherwise. It is only with some of the smaller SCR's that gate resistors are specified with G-E SCR's.

V_{BO} is sensitive to temperature, gate drive, and rate of rise of forward voltage (dv/dt). As temperature increases, V_{BO} tends to decrease; it is, therefore, important that V_{BO} be specified at maximum temperature. As gate drive is increased, V_{BO} decreases. This characteristic is used for turning the SCR "on" by means of the gate and is discussed in Chapter 4. Rate of voltage rise is discussed in Section 3.7.5.

3.7.4 PEAK FORWARD VOLTAGE (PFV)

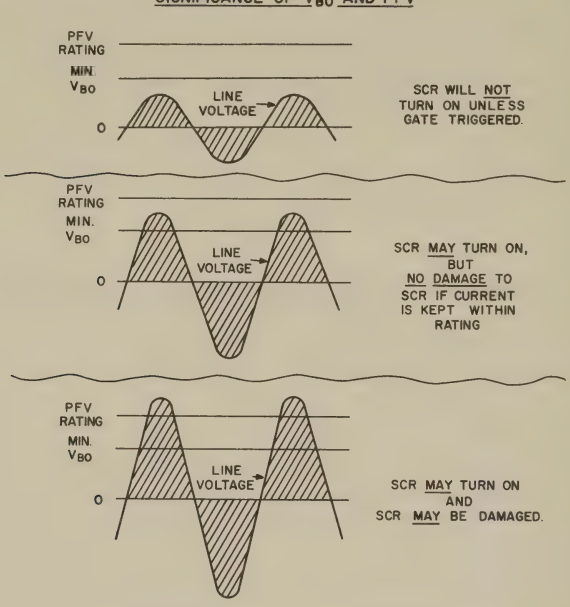
An SCR can be turned on in the absence of any gate drive by exceeding its forward breakover voltage (V_{BO}). Although SCR's, in contrast to four layer diodes, are designed to be brought into conduction by means of driving the gate, breakover in the forward direction is non-destructive provided it takes place below a value noted in the specification sheet as Peak Forward Voltage (PFV). Voltage beyond the PFV rating may cause degradation of some SCR's, and eventual failure. Figure 3.10 illustrates the relationship of PFV to V_{BO}.

It will be noted that usually a given SCR has a single PFV rating independent of its PRV-V_{BO} voltage class designation. This is due to the fact that the limit on PFV is not an inherent characteristic of the bulk properties of the semiconductor junction but rather one of the construction of the device and the pellet surface properties of the entire line of a particular device class.

The PFV rating is often of practical importance when SCR's are tested for V_{BO} at room temperature; often a unit will have a V_{BO} beyond its PFV rating

at temperatures lower than maximum rated junction temperature. A proper test for V_{BO} under these circumstances would be to conduct it at the elevated temperature at which the minimum V_{BO} for the device is specified.

In applications where the PFV rating of an SCR may be exceeded it is suggested that a network be connected anode to gate so that the device will fire by gate drive rather than by forward breakover. A zener diode may be used to effect gate firing at a predetermined level, or a Thyrector diode may be used to obtain a similar action.



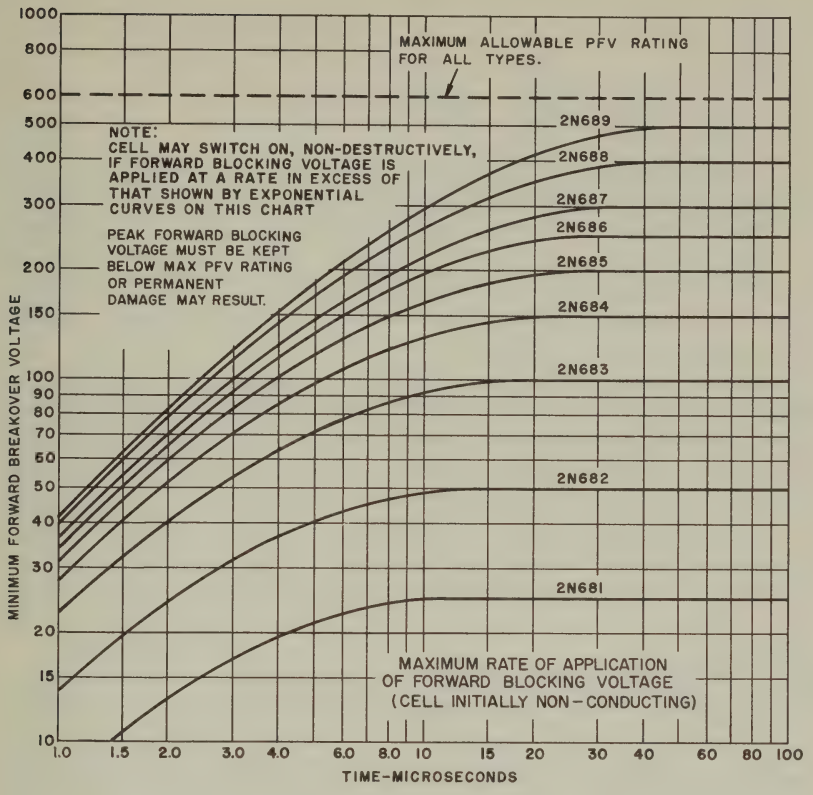
Significance of V_{BO} and PFV
Figure 3.10

3.7.5 *RATE OF RISE OF FORWARD VOLTAGE (dv/dt)*

A high rate of rise of forward voltage may cause an SCR to switch into the "on" or low impedance forward conducting state. This is of some importance when SCR's are either energized in circuits having fast rise times or are subject to high frequency transient voltages. This is discussed further in Chapter 13.

General Electric SCR's are characterized with respect to this parameter in a "worst case" sense; that is, maximum rates of rise are given beyond which an SCR may turn on at its maximum rated junction temperature (again worst case). These data enable the designer to tailor his circuitry in such a manner that these ratings will not be exceeded. Figure 3.11 shows the dv/dt specifications for the 2N681 series SCR's.

A dv/dt requirement is also given as a part of the turn-off time specification for inverter type SCR's. The information given in Figure 3.11 is not di-



Maximum Rate of Application of Forward Blocking Voltage for 2N681 Series SCR
Figure 3.11

rectly applicable as a part of the turn-off time specification. Chapter 5 discusses turn-off time in detail.

Since a high circuit dv/dt effectively reduces V_{BO} under given temperature conditions, a higher voltage classification unit will allow a higher rate of rise of forward voltage *for a given peak circuit voltage*. For example, for a peak circuit voltage of 150 volts, Figure 3.11 shows that a 2N685 (200 volt minimum V_{BO}) will allow an exponential rise to this voltage in 8 μseconds; a 2N687 (300 volt minimum V_{BO}) will require only 5 μseconds.

However, as Figure 3.11 shows, dv/dt capability for a rise of voltage to rated level decreases as one goes to higher voltage class units. Operation at lower junction temperatures allows the device to withstand higher rates of rise of forward voltage than shown in Figure 3.11.

Reverse biasing of the gate with respect to the cathode substantially increases dv/dt withstand capability beyond that shown in Figure 3.11. The reader is referred to Section 4.5 for quantitative data. A small capacitor connected in shunt from anode to cathode may also be used to minimize the effect of high dv/dt.

3.8 GATE CIRCUIT RATINGS

Maximum ratings for the gate circuit are discussed in Chapter 4.

3.9 HOLDING CURRENT

Somewhat analogous to the solenoid of an electromechanical relay, an SCR requires a certain minimum anode current to maintain it in the "closed" or conducting state. If the anode current drops below this minimum level, designated as the holding current, the SCR reverts to the forward blocking or "open" state. The holding current for a typical SCR has a negative temperature coefficient; that is, as its junction temperature rises, its holding current requirement decreases.

A somewhat higher value of anode current than the holding current is required for the SCR to initially "pickup." If this higher value of anode current is not reached, the SCR will revert to the blocking state as soon as the gate signal is removed. Immediately after this initial pickup action, however, the anode current may be reduced to the holding current level. Where circuit inductance limits the rate of rise of anode current and thereby prevents the SCR from switching solidly into the conducting state, it may be necessary to make alterations in the circuit. This is discussed further in Chapter 4.

3.10 RELIABILITY, STABILITY, AND FAILURE MECHANISMS

General Electric SCR's, like diode rectifiers, are subject to very stringent quality control standards. The concept of quality control is total; that is, it is integrated into all the steps from initial design through evaluation, incoming parts inspection, in-process control, design center testing, environmental testing, acceptance testing, and life testing.

Failure criteria are based on variation out of specification of a given device parameter rather than any type of catastrophic failure. On full load tests, all parameters are operated at their maximum rated values. For this reason, failures under these conditions represent the most pessimistic case, since in an actual application it is rare that all parameters are being operated at their maximum rated values.

Where required, specific reliability information can be supplied on controlled rectifier products under specified conditions of operation. The high cost associated with accumulating meaningful reliability data to significant levels of confidence is usually justified only for high reliability military programs. However, an example of meeting a general reliability standard can be given for the 2N681 series medium current SCR in its meeting MIL-S-19500/108/USN. This specification spells out a reliability level in conformance with specified test conditions equivalent to a 4% AQL. The experience gained in qualifying to this specification, however, was so favorable that other means of designating reliability standards have been proposed which would be equivalent to a 1% AQL level.

Stability of device parameters is considered very important in obtaining high levels of reliability. One of the most stringent tests to which a controlled rectifier can be subjected is that of an elevated temperature blocking life test. This is a test performed on all General Electric controlled rectifiers for a duration determined by statistical criteria of confidence level. It has been found that if a device is subject to a possible drift in any of the parameters due to the onset of a degradation mechanism, it will show up by the end of a blocking life test. This test may be considered a type of accelerated "ageing" test to screen a production line for possible future failures.

Failure mechanisms of controlled rectifiers generally fall into three categories:

First, there is the possibility of an increase of surface conductivity of the silicon pellet as a result of chemical activation of sealed-in contaminants or by an imperfect hermetic seal allowing moisture penetration from the atmosphere. The electrical consequences are reduction in forward blocking capability and an increase in reverse leakage current. However, reduction of forward blocking capability is also often the first indication that some rating of the device is being over-stressed by such causes as current surges or voltage transients.

Fracturing of the silicon pellet is another possible failure mechanism. Usually, high current overloads, extreme temperature cycling, or excessive mechanical abuse lead to this condition.

Finally, thermal fatigue which develops as a result of many temperature cycles may lead to ultimate failure if the thermal impedance of the device structure increases and leads to increased dissipation and finally junction temperatures above rated value. Certain so-called "soft" solders used in attaching the silicon sandwich to the stud in some devices can recrystallize, over certain extreme temperature cycles, causing deterioration of the solder joints. This type of failure mechanism was first noticed among some of the older types of diode rectifiers. It has, however, not been a problem with G-E controlled rectifiers for two reasons. Higher temperature SCR's use improved, so-called "hard," soldering techniques and SCR's using soft solder techniques are limited by their temperature ratings to operation over narrower temperature ranges and hence are subjected to negligible thermal fatigue stresses.

These failure mechanisms cause the characteristics of the SCR to change in the manner discussed in Section 11.7.

In certain high reliability applications it is often required to take additional steps to increase the reliability and stability of the device even beyond the high levels already being achieved with standard products. Junction temperature derating by derating current or larger heatsinking is perhaps the single most effective way of going in the direction of increased potential reliability. Other steps that can be taken in this direction are above all to keep the device applied well within ratings and not subjected to either over-voltages or over-currents in excess of specified ratings. Applied within its ratings, the controlled rectifier has taken its place among the most reliable of all semiconductor devices.

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CHAPTER 4

FIRING CHARACTERISTICS AND GATE CIRCUITS

The proper design of firing circuits for SCR's involves three important considerations: (1) choice of a suitable circuit which will supply the firing signal under the required circuit conditions, (2) determination of the maximum voltages and currents which the firing circuit can supply to the gates of the SCR's to ensure that the maximum allowable gate ratings are not exceeded, and (3) determination of the minimum voltages and currents which the firing circuit will supply to the gates of the SCR's to ensure that the SCR's will be fired reliably under all conditions. This chapter describes in detail the firing characteristics of the SCR and the considerations for the proper design of firing circuits. The different types of basic firing circuits are described in this chapter and examples of the use of these firing circuits in practical applications are given in Chapters 8 and 9.

4.1 GATE V-I CHARACTERISTICS

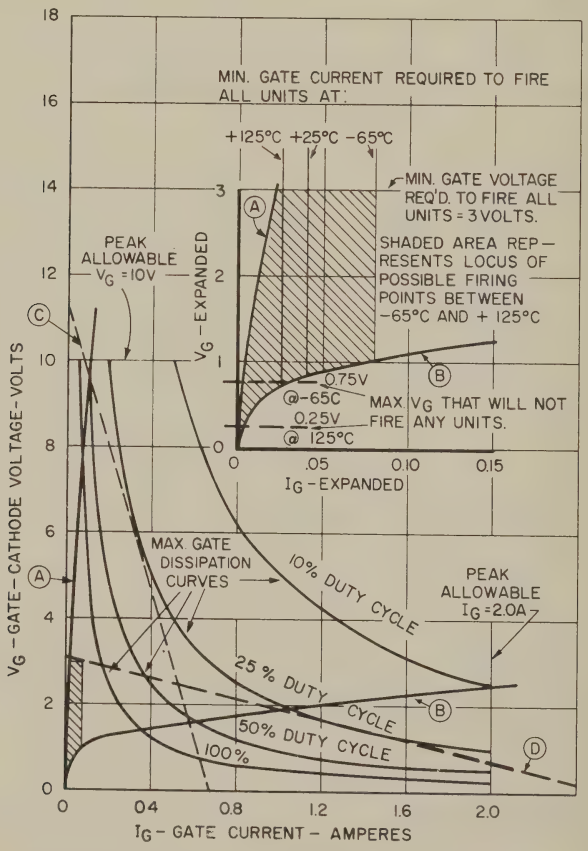
The gate characteristics and firing characteristics of an SCR are normally presented in the form of a graph similar to Figure 4.1. This graph indicates the range of gate currents and gate voltages required to fire the 2N681 series SCR. It also indicates the limit values of the voltage-current characteristic between gate and cathode (curves A and B). From this figure it can be seen that gate current requirements for firing decrease substantially as the junction temperature increases. Although not specifically portrayed in this figure, the gate current requirements also decrease slightly as the anode to cathode voltage is increased. Because of the temperature and anode effects on the control characteristic, it is desirable to fire SCR's with a steep wavefront of gate current whenever precise timing or phase control is required. For strictly on-off control, however, adjustment of gate current magnitude rather than timing is satisfactory provided ample current is furnished for positive firing.

To prevent damaging the SCR, several limitations must be imposed on the gate signal. These are spelled out in G-E specification bulletins. For the 2N681, for example, the peak positive voltage between the gate and cathode should not be allowed to exceed 10 volts and the peak negative voltage between the gate and cathode should not be allowed to exceed 5 volts. The peak forward gate current should be limited to 2 amperes. Peak allowable gate power dissipation is 5 watts and the average gate power dissipation is 0.5 watts.

4.2 LOAD LINES

For reliable firing under all temperature conditions, the gate signal source should be designed to produce voltages and currents in excess of the values

indicated by the shaded area in Figure 4.1 without exceeding the maximum limitations specified above. To assist in constructing gate signal load lines, the maximum allowable power dissipation curves for various duty cycles of gate signal have been plotted in Figure 4.1. For positive firing of all cells within the entire temperature range without exceeding the power limitations, load lines should be chosen so that they remain above and to the right of the shaded area. However, the lines must also remain below and to the left of the maximum allowable power dissipation curve that applies for the particular duty cycle being used. These maximum power dissipation curves assume that negligible gate dissipation occurs during the interval that negative voltage is applied to the gate. For example, if gate signal duration is one-quarter of the cycle, the duty cycle is 25%. Dashed lines C and D in Figure 4.1 illustrate the maximum limits of load lines for the 2N681 controlled rectifier at 25% duty cycle. For load line C, the peak open circuit voltage of the gate source is 11.2 volts and its short circuit current is 680 ma. For load line D, the values of open circuit voltage and short circuit current are 3.1 volts and 2.6 amperes, respectively.


MIN. GATE CURRENT REQUIRED TO FIRE ALL UNITS AT:
+125°C +25°C -65°C
MIN. GATE VOLTAGE REQ'D. TO FIRE ALL UNITS = 3 VOLTS.
SHADED AREA REPRESENTS LOCUS OF POSSIBLE FIRING POINTS BETWEEN -65°C AND + 125°C
PEAK ALLOWABLE V_G = 10V
V_G - EXPANDED
0.75V @ -65C
0.25V @ 125°C
MAX V_G THAT WILL NOT FIRE ANY UNITS.
I_G - EXPANDED
MAX GATE DISSIPATION CURVES
10% DUTY CYCLE
25 % DUTY CYCLE
50% DUTY CYCLE
100%
PEAK ALLOWABLE I_G = 2.0A
V_G - GATE - CATHODE VOLTAGE - VOLTS
I_G - GATE CURRENT - AMPERES

Gate and Firing Characteristics of 2N681 Series SCR
Figure 4.1

4.3 MINIMUM FIRING LEVEL

Figure 4.1 also indicates the gate voltage level below which no 2N681 SCR will fire. At 125°C junction temperature this value is 0.25 volt; at −65°C it is 0.75 volt. A linear variation occurs between these two temperature limits. This limit is important when designing a firing circuit which has a standby leakage current when no firing signal is present. Examples of this are saturable reactors and unijunction transistor firing circuits. To prevent misfiring under these circumstances, a resistor should be connected across the output of the firing circuit. Its value of resistance in ohms should not exceed 0.25 volt divided by the maximum standby current in amperes.

4.4 NEGATIVE GATE VOLTAGE AND CURRENT

The gate should never be allowed to become more negative with respect to the cathode than is indicated on the specification bulletin. For the 2N681 this is 5 volts negative. If there is a possibility that the gate will swing more negative than the allowable value, a diode should be connected either in series with the gate or from cathode to gate to limit the reverse gate voltage.

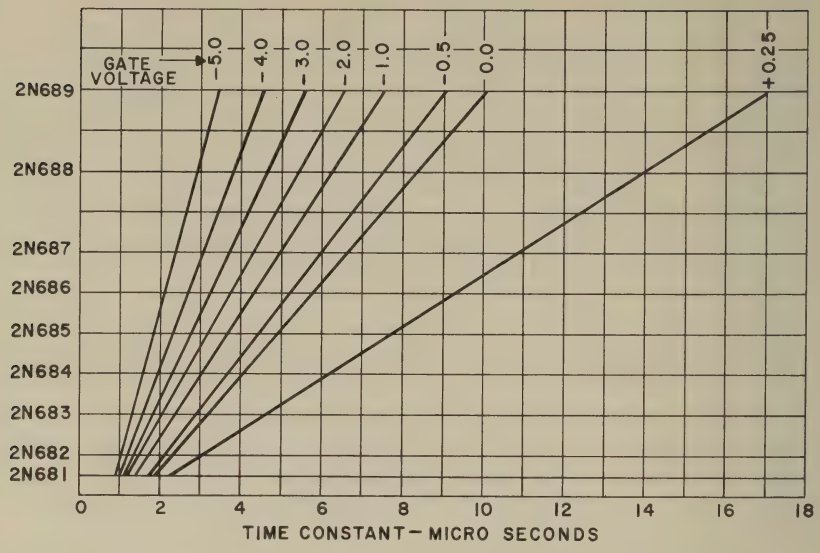
A considerable negative gate current (conventional current flow out of the gate) can be caused to flow if the cathode circuit between cathode and gate is opened for any reason while the SCR is conducting forward load current (conventional current flow from anode to cathode). This current would initially be limited only by the impedance of the gate circuit and could easily cause the allowable gate dissipation to be exceeded, thus leading to failure of the SCR.

4.5 NEGATIVE GATE BIASING

All General Electric SCR specifications are for "open" gate conditions except where specifically noted. This is a "worst case" condition inasmuch as any amount of negative biasing (current, voltage, or both) tends to maintain or increase the forward breakover voltage (V_{BO}) at a given temperature.

Generally speaking, this effect is greatest for the smaller junction area devices. In the medium current SCR lines available on the market at this writing, a representative cross section indicates that an identical conclusion applies across the board: out of a sample of devices available from each of several sources some medium current units showed V_{BO} improvement, others did not. Where V_{BO} improvement is not warranted for each individual SCR it is felt that conservative equipment design practice should not depend on increasing V_{BO} by negative gate biasing.

However, there is a great improvement in dv/dt withstand capability (see Section 3.7.5) that can be achieved by negative gate biasing. Figure 4.2 shows the effect of gate bias on the allowable time constant of application of forward blocking voltage without the possibility of having the SCR switch on. Figure 3.11 in Section 3.7.5 gives this information for an "open" or zero bias gate condition for the 2N681 series SCR. Figure 4.2 extends the usefulness of this information for different values of gate bias.



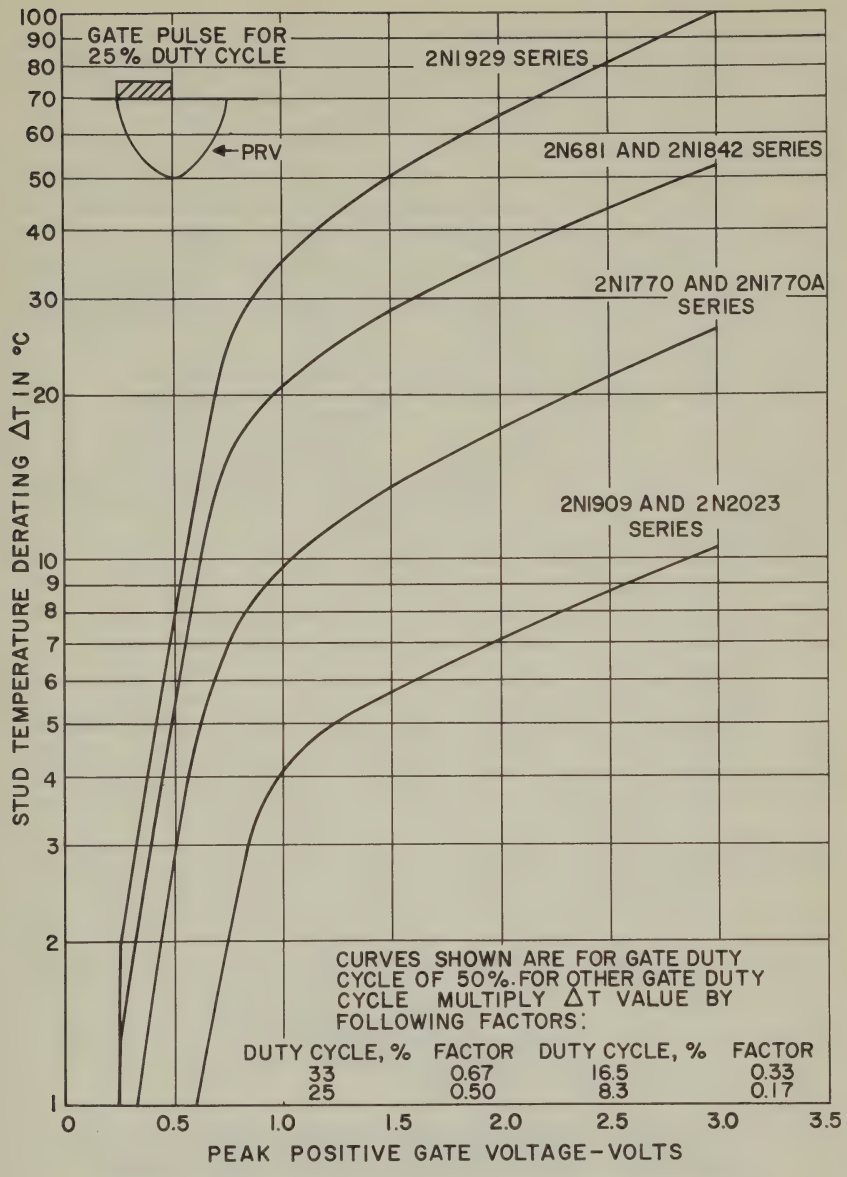
Effect of Gate Bias on Allowable Time Constant of Application of Forward Blocking Voltage
Figure 4.2

4.6 POSITIVE GATE VOLTAGE WHEN ANODE IS NEGATIVE

The presence of positive voltage on the gate when reverse voltage is applied to the anode increases reverse leakage current through the device substantially. As a result, the SCR must dissipate additional power. It is, therefore, necessary either to make provision for this additional loss or to take steps to limit it to a negligible value.

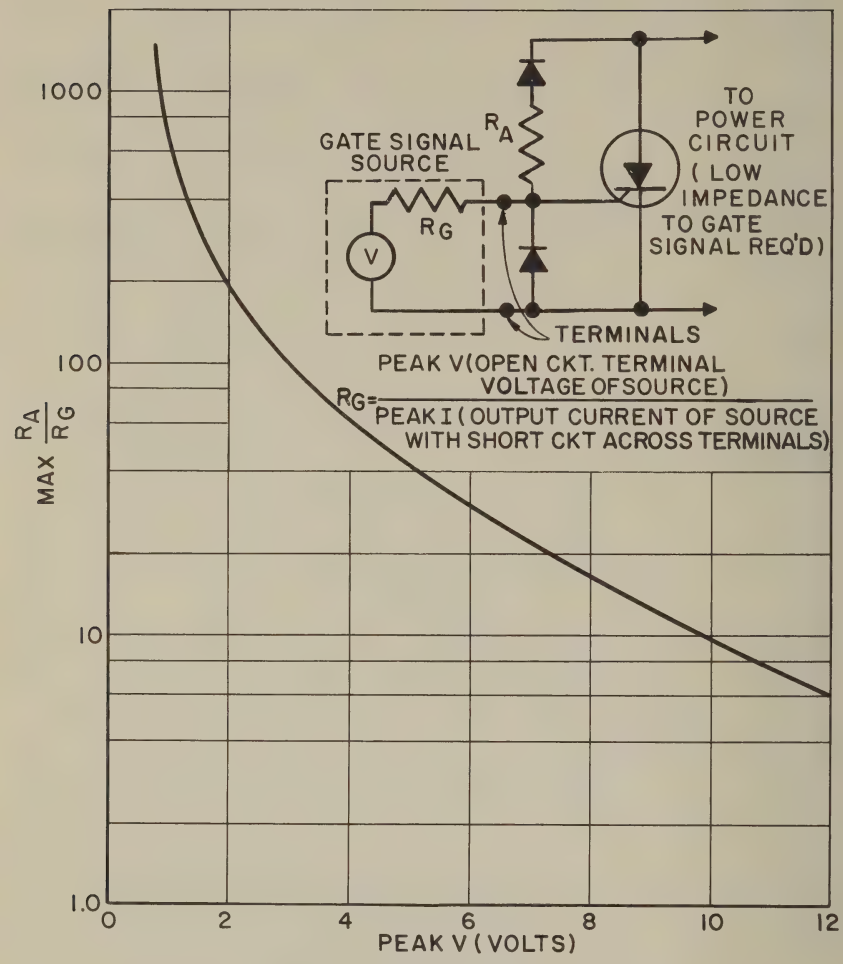
Figure 4.3 gives the temperature derating for different SCR lines at various gate drive duty cycles (per cent of full cycle or 360 electrical degrees) for values of peak positive gate voltage. For proper application this loss must be included in the total device dissipation. The temperature derating, ΔT, found from Figure 4.3, must be subtracted from the maximum allowable stud temperature (found from a curve such as Figure 3.8) for the proper cell type and conduction angle. For lead mounted devices, subtract from the ambient temperature curve. Derating becomes negligible if the gate voltage is less than 0.25 volt or the temperature derating turns out to be 1°C or less.

A means of limiting the additional reverse dissipation to a negligible value is given by a gate clamping circuit of the type shown in Figure 4.4 for low, medium, and high current SCR's (2N1770 through 2N2023 series). Resistor R_A and a diode are connected from gate to anode to attenuate positive gate signals whenever the anode is negative. For a given peak value of open circuit gate source voltage, Figure 4.4 gives the maximum ratio of the value of R_A to R_G that will safely clamp the gate for all values of reverse voltage within the PRV rating of the SCR.


GATE PULSE FOR 25% DUTY CYCLE
PRV
2N1929 SERIES
2N681 AND 2N1842 SERIES
2N1770 AND 2N1770A SERIES
2N1909 AND 2N2023 SERIES
STUD TEMPERATURE DERATING ΔT IN °C
PEAK POSITIVE GATE VOLTAGE-VOLTS
CURVES SHOWN ARE FOR GATE DUTY CYCLE OF 50%. FOR OTHER GATE DUTY CYCLE MULTIPLY ΔT VALUE BY FOLLOWING FACTORS:
DUTY CYCLE, % FACTOR DUTY CYCLE, % FACTOR
33 0.67 16.5 0.33
25 0.50 8.3 0.17

Temperature Derating Curve for Simultaneous Application of Positive Gate Pulse when Anode is Positive
Figure 4.3

An alternate way to limit additional reverse leakage dissipation due to positive gate voltage is to insert in series with the SCR a diode rectifier that has a lower reverse leakage current. In this manner the diode will assume the greater share of the reverse voltage applied to the series string, significantly reducing reverse dissipation in the SCR.



Gate Clamp Circuit for Controlled Rectifier
Figure 4.4

4.7 FIRING CIRCUIT CONSIDERATIONS FOR SERIES AND PARALLEL OPERATION

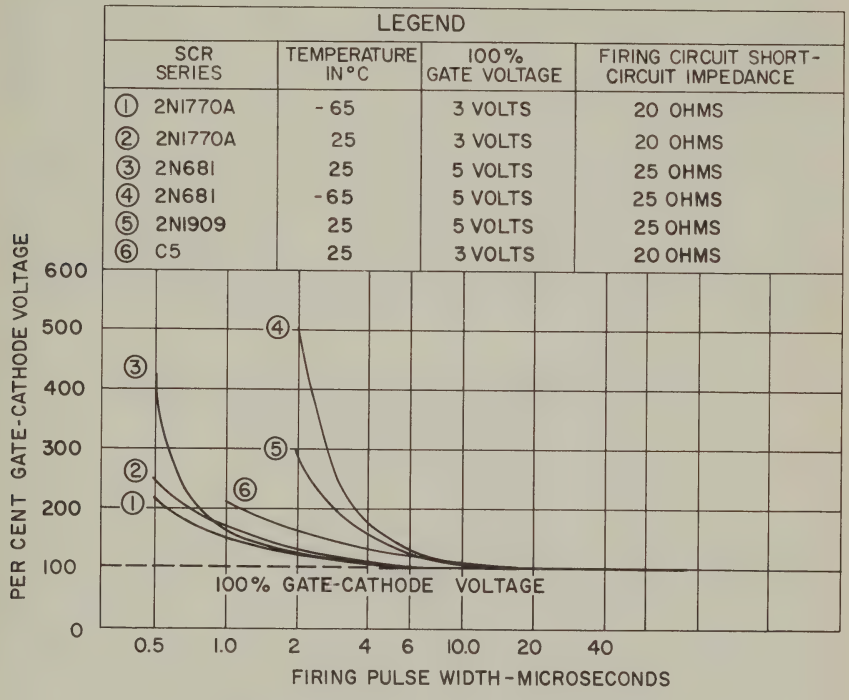
This subject is discussed in Chapter 6. Considerations for firing several SCR's simultaneously from a single unijunction transistor firing circuit are discussed in Section 4.13.5.

4.8.1 PULSE FIRING

The maximum gate signal necessary for firing any SCR under the most adverse conditions (—65°C junction temperature) is given in the specification

sheet in the form shown in Figure 4.1. There, for example, it is seen that for the 2N681 series SCR no more than 80 ma at 3 volts is required to fire every SCR of that specification at −65°C. This requirement assumes either a DC level of this magnitude or a pulse of this magnitude with a minimum pulse width as shown in Figure 4.5 corresponding to the "100% Gate-Cathode Voltage" line. In this figure the per cent increase in gate voltage required to fire is shown for decreasing firing pulse widths.

The data shown in Figure 4.5 are valid only if the anode current is allowed to build up rapidly enough so that the holding current of the SCR is reached before the pulse is terminated. For highly inductive anode circuits it is, therefore, advisable to use a square wave type of firing signal assuring gate drive until holding current has been attained. Also, in certain rectifier and inverter circuits that require refiring, a square wave type of trigger circuit shown in Section 4.14.3 might be considered.



Gate Voltage Required for Short Firing Pulse Duration
Figure 4.5

The DC gate firing characteristics are measured on a 100% basis in production for all SCR's, but the pulse firing characteristics are measured only on a sampling basis. For applications where the pulse firing characteristics are critical, a special specification should be requested so that satisfactory pulse firing will be assured.

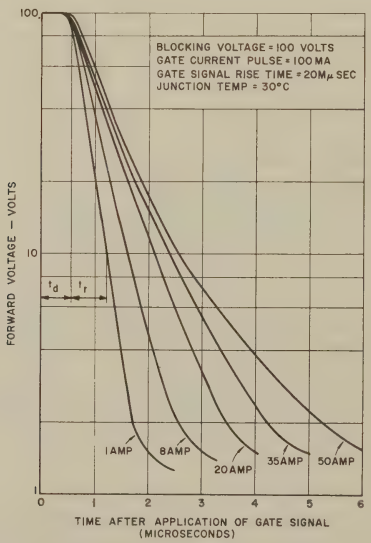
4.8.2 DELAY TIME

After the beginning of a gate current pulse there is a small delay before appreciable increase in the load current occurs. The delay time, t_d, is defined as the time between the leading edge of the gate current pulse and the 10% point of the anode current waveform. The delay time decreases as the amplitude of the gate current pulse is increased, but approaches a minimum value of 0.2 to 0.5 μsec for gate current pulses of 500 ma or more.

4.8.3 RISE TIME

The rise time, t_r, is defined as the time required for the anode current waveform to rise from the 10% to the 90% point. The rise time depends on the nature of the load and to a lesser extent on the initial value of the anode voltage. For non-inductive circuits where the rate of increase of load current is only a function of the switching characteristic of the SCR, the rise time generally decreases as the voltage is increased or as the load current is decreased. Below approximately 100 ma anode current, t_r tends to increase again. At these low current levels, t_r may be minimized by connecting a small capacitor across the SCR from anode to cathode.

Figure 4.6 shows the turn-on characteristic of a typical 2N681 when subjected to a 100 ma gate signal with 20 mμsec rise time and an anode voltage of 100 volts. As the load current during switching is increased, t_r becomes longer. Rise time may be decreased to some degree by substantially overdriving the gate. The delay time and rise time tend to increase with temperature. The total switching time ($t_d + t_r$) increases by about 20-30% between 25°C and 100°C.



Turn-On Characteristics of Typical 2N681 Controlled Rectifier
Figure 4.6

4.8.4 JITTER

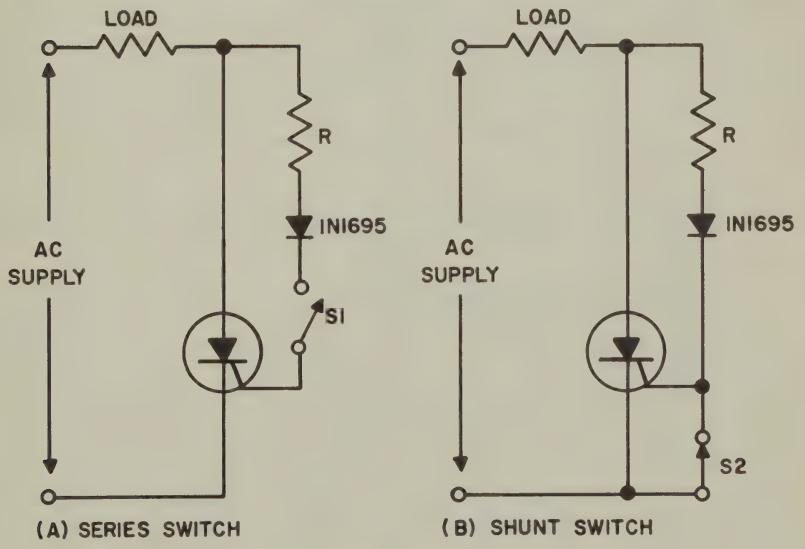
The jitter or variation of switching time from one cycle to the next is less than 2 mμsec at constant temperature if the gate is driven at two to three times the minimum amplitude required for firing.

4.9 DC FIRING

For simple on-off switching of SCR's in DC circuits a continuous DC gate signal is satisfactory, provided that the gate power dissipation is not exceeded. With DC circuits separate means must be provided for turning off the SCR as described in Chapter 5. With AC circuits a continuous DC gate signal can also be used, provided that the considerations of Section 4.6 are taken into account.

4.10 AC FIRING

Figure 4.7 shows a simple method of obtaining gate current for firing the SCR from the main AC supply whenever the anode is positive with respect to the cathode. As soon as the SCR has fired, the anode voltage drops to the conduction value and the gate current decreases to a low value. Resistor R limits the peak gate current and for the 2N681 should be greater than the AC peak voltage divided by two amperes. The diode in the gate circuit is provided to prevent reverse voltage from being applied between cathode and gate during the reverse part of the cycle. If desired, the diode can be connected between gate and cathode rather than in series with R. Conduction is initiated by closing contact S_1 in Figure 4.7(a) or by opening contact S_2 in Figure 4.7(b). Interruption of load current occurs within one-half cycle after opening S_1 or closing S_2.

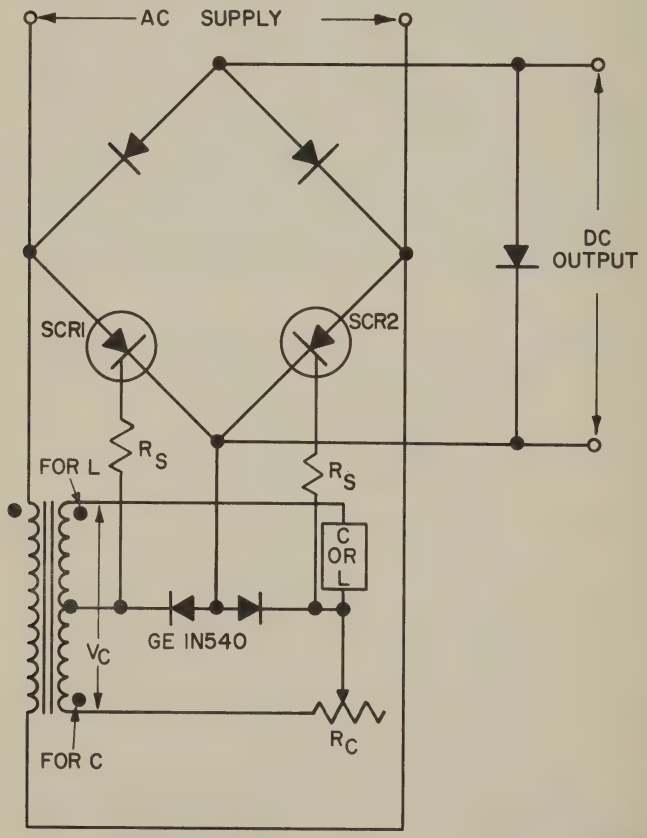


(A) Series Switch (B) Shunt Switch
Half-Wave Static Switch
Figure 4.7

A very promising device for use as the switches S_1 and S_2 in Figure 4.7 is the reed switch. It consists of a set of contacts in a hermetically-sealed glass enclosure which can be actuated by a small magnetic field. Typical commercially available units have pick-up ampere-turns on the order of 50 with drop-out ampere-turns between 15 and 20. Since the reed switch also responds to small permanent magnets, static limit switch type operation can easily be effected.

4.11 AC PHASE SHIFT FIRING CIRCUITS (CONTINUOUS CONTROL)

Figure 4.8 illustrates a full-wave phase controlled rectifier employing an R-C or R-L phase shift network to delay the gate signal with respect to the anode voltage on the SCR's. Many variations of this type of phase shift circuit have been worked out for thyratrons.



R-C or R-L Phase Shift Network Control of Single Phase Bridge Output
Figure 4.8

When using SCR's (2N1929, 2N1770, 2N1770A, 2N681, 2N1842, 2N1909, 2N2023 series), the following criteria should be observed to provide the maximum range of phase shift and positive firing over the particular SCR's temperature range without exceeding the gate voltage and current limitations:

A. The peak value of V_c should be greater than 25 volts.

B. $\frac{1}{2\pi fC}$ or $2\pi fL \leq \frac{V_c}{2} - 9$

where C = capacitance in farads
L = inductance in henries
V_c = peak end-to-end secondary voltage of control transformer
f = frequency of power system

C. $R_s = \frac{V_c - 20}{0.2}$

where R_s = series resistance in ohms

D. $R_c \geq \frac{10}{2\pi fC}$ or $10\ (2\pi fL)$

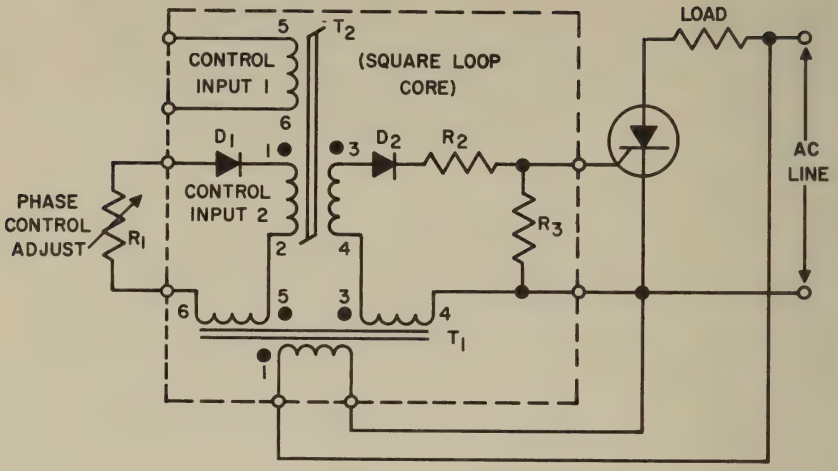
Because of the frequency dependence of this type of phase shift circuit, the selection of adequate L or C components becomes easier at higher operating frequencies.

4.12.1 SATURABLE REACTOR FIRING CIRCUITS

Saturable reactors provide the desirable steep wavefront of gate current with a convenient means of control by a low level DC or AC signal. This type of control is adaptable to feedback systems and provides the additional advantage of multiple, electrically-isolated inputs and outputs for more complex circuits.

4.12.2 CONTINUOUSLY VARIABLE CONTROL

A typical half-wave magnetic firing circuit is shown in Figure 4.9. The gate signal for firing the SCR is obtained from winding 3-4 of transformer T_1. When the core of T_2 is unsaturated, the winding 3-4 of T_2 presents a high impedance to the gate signal so that only a small voltage is developed across R_3. When the core of T_2 saturates, the impedance of winding 3-4 of T_2 decreases by several orders of magnitude so that a large voltage appears at the gate of the SCR, causing it to fire. Resistor R_2 limits the gate current to the rated value (Section 4.2) and resistor R_3 limits the gate voltage produced by the magnetizing current of winding 3-4 of T_2 so that the SCR will not fire before the core of T_2 saturates. Diode D_2 serves the dual purpose of preventing a reverse voltage on the gate of the SCR and preventing any reverse current through winding 3-4 which would produce an undesired reset of the core T_2.



Typical Half-Wave Magnetic Firing Circuit
Figure 4.9

Control signals can be applied to either input 1 or input 2 or both. Input 2 operates in the reset mode by controlling the reset voltage on winding 1-2 of T_2 during the negative half cycle. The setting of the potentiometer R_1 determines the amount of reset of the core during the negative half cycle, which in turn determines the phase angle of the SCR conduction during the positive half cycle. Other control circuits such as a transistor amplifier stage can be used in place of R_1. Since power is furnished by winding 5-6 of T_1, no auxiliary power supply is needed. Input 1 operates in the MMF (magnetomotive force) mode by controlling the current through the winding 5-6 and the core flux level, which in turn determines the firing angle. The current for input 1 must be obtained from an external power supply or from a current generating type of transducer.

Additional output windings can be added to T_2 for firing several SCR's in parallel or in series. Also, additional control windings of the reset or MMF type can be added to T_2. Full wave and multiple phase operation can be achieved by combining two or more half wave circuits.

Commercial Magnetic Firing Circuits

The companies listed below can supply packaged magnetic firing circuits which are designed specifically for operation with SCR's. These units are available in half wave and full wave designs, single phase or three phase, for 60 cps or 400 cps. These companies can generally supply special designs where required and can also furnish more detailed information on the application of magnetic firing circuits.

Avion Division
ACF Industries
11 Park Place
Paramus, New Jersey

Fairfield Engineering
934 Hope Street
Springdale, Connecticut

Control Division
Magnetics, Inc.
Butler, Pennsylvania

Ovitron Corporation
37-04 48th Avenue
Long Island City 1, New York

Vectrol Engineering, Inc.
P.O. Box 1089
Stamford, Connecticut

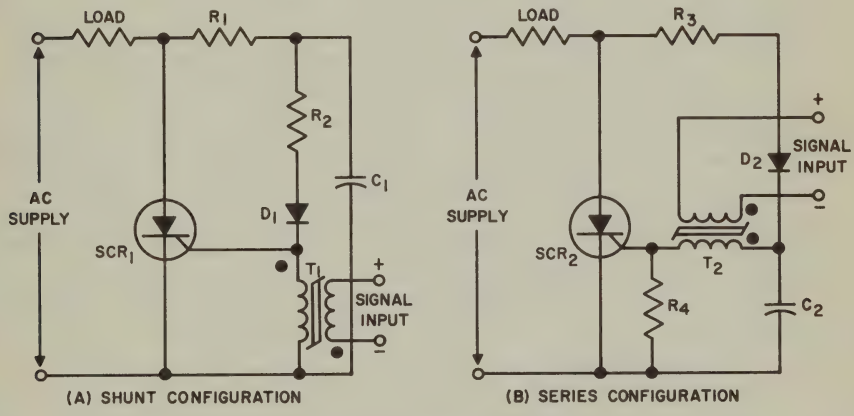
Data Master Corporation
85 Hazel Street
Glen Cove, New York

Dresser Electronics
555 North 5th Street
Garland, Texas

Bergen Laboratories, Inc.
60 Spruce Street
Paterson, New Jersey

4.12.3 ON-OFF MAGNETIC FIRING CIRCUITS

Magnetic firing circuits designed for phase control applications such as the one shown in Figure 4.9 require the use of saturable cores which are large enough to allow the output winding to sustain the gate voltage signal for a full half cycle without saturating. For simple on-off control applications, the magnetic firing circuits shown in Figure 4.10 permit the use of smaller and less expensive cores since the output winding is not required to sustain the gate voltage signal for a full half cycle. In addition, these circuits have the advantage of not requiring the use of an auxiliary supply transformer.



Half-Wave On-Off Magnetic Firing Circuits
Figure 4.10

In Figure 4.10(a) one winding of saturable transformer T_1 is connected in shunt with the gate of SCR_1. If T_1 is unsaturated, the current through R_1, R_2 and D_1 will flow into the gate of SCR_1 during the first part of the positive half cycle and cause SCR_1 to turn on. If T_1 is saturated, the current through R_1, R_2 and D_1 will be diverted from the gate by the low saturated impedance of the winding on T_1. When T_1 is saturated it can be reset and the SCR can be made to fire by a positive voltage on the signal input. Capacitor C_1 provides filtering for the gate signal to prevent undesired firing due to fast transients on the AC supply.

In Figure 4.10(b), one winding of saturable transformer T_2 is connected in series with capacitor C_2 and the gate of SCR_2. If T_2 is unsaturated the current through R_3 and D_2 will charge C_2 during the initial part of the positive half cycle. T_2 will saturate after a few degrees of the positive half cycle and permit a rapid discharge of C_2 into the gate of SCR_2, thus causing SCR_2 to fire. If T_2 is initially saturated at the beginning of the positive half cycle, the winding of T_2 will divert the current from C_2 and prevent C_2 from being charged. Resistor R_4 prevents the voltage at the gate of SCR_2 produced by the current through R_3 from exceeding the minimum gate firing voltage. When T_2 is saturated it can be reset and the SCR can be made to fire by a positive voltage at the signal input.

The circuits of Figure 4.10 permit the SCR to perform the function of an AC contactor with an isolated DC control winding. Modifications of these circuits permit full wave operation with normally open, normally closed or latching operation. An example of a full wave latching type control circuit is described in Chapter 7.

4.13.1 BASIC UNIJUNCTION TRANSISTOR FIRING CIRCUITS

The silicon unijunction transistor (2N1671A and B) is an ideal device for use in SCR firing circuits. It has the advantages of a stable firing voltage, a very low firing current, operation over a temperature range of −55°C to +140°C, and a peak current rating of two amperes. SCR firing circuits using the UJT (unijunction transistor) are simple and compact with low power consumption and a high effective power gain in phase control circuits.

The characteristics of the UJT which are most important in the design of SCR firing circuits are described here. For further information on the UJT, see condensed specifications in the rear of this manual, or consult specification sheets (ECG-516), the UJT application notes (ECG-380), and pages 138-147 of the G-E Transistor Manual, Fifth Edition.

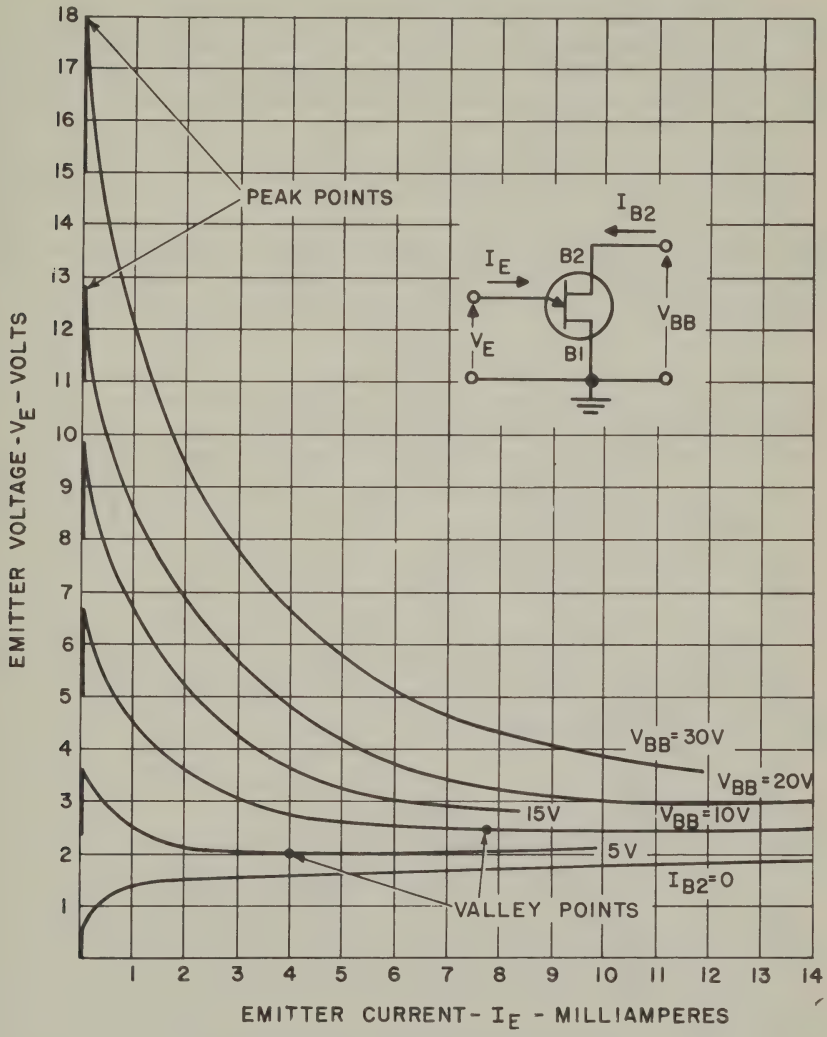
A line of packaged UJT firing circuits is available from the following manufacturer:

Empire Services
RD #3
Skaneateles, New York

4.13.2 UNIJUNCTION TRANSISTOR CHARACTERISTICS

The UJT has three terminals which are called the emitted (E), base-one (B_1), and base-two (B_2). Between B_1 and B_2 the unijunction has the characteristics of an ordinary resistance. This resistance is called the interbase resistance (R_{BB}) and at 25°C has values in the range from 4.7K to 9.1K. The interbase resistance increases linearly with temperature up to about 140°C. The temperature coefficient at 25°C is about +0.8%/°C.

The normal biasing conditions for the UJT are indicated in Figure 4.11. If the emitter voltage, V_E, is less than the emitter peak point voltage, V_P, the emitter will be reverse biased and only a small reverse leakage current, I_{EO}, will flow. When V_E is equal to V_P and the emitter current, I_E, is greater than the peak point current, I_P, the UJT will turn on. In the on condition, the resistance between the emitter and base-one is very low and the emitter current will be limited only by the series resistance of the emitter to base-one circuit. When measured with pulse currents over 30 milliamperes, the AC resistance between emitter and base-one lies in the range from 5 to 20Ω.



Unijunction Transistor Symbol and Emitter Input Characteristics
Figure 4.11

The peak point voltage of the UJT varies in proportion to the interbase voltage, V_{BB}, according to the equation:

$$V_P = \eta V_{BB} + V_O \tag{4.1}$$

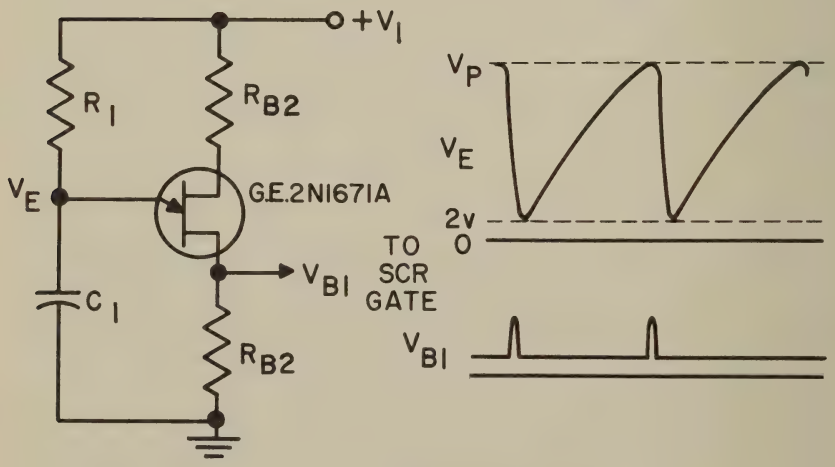
The parameter η is called the intrinsic standoff ratio and is independent of bias conditions and temperature. The value of η lies between 0.47 and 0.75 according to the particular type of UJT. The voltage V_D is the equivalent emitter diode voltage which at 25°C is about 0.70 volts. It is found that V_D decreases with temperature, the temperature coefficient being about −2 mv/°C. Most of the variation of the peak point voltage with temperature may be ascribed to the change in V_D. It is possible to compensate for this temperature change by making use of the positive temperature coefficient of R_{BB}. If a resistor R_2 is used in series with base-two as shown in Figure 4.12 the temperature variation of R_{BB} will cause V_{BB} to increase with temperature. If R_2 is chosen correctly, this increase in V_{BB} will compensate for the decrease in V_D in Equation 4.1. The proper value of R_{B2} is approximately:

$$R_{B2} \cong \frac{0.40\, R_{BB}}{\eta\, V_1} + \frac{(1-\eta)\, R_{B1}}{\eta} \tag{4.2}$$

where the first term represents the compensation for the temperature variation of V_P and the second term represents the resistance needed in base-two to compensate for R_1. If the resistance R_2 satisfies the above equation, the peak point voltage will be

$$V_P = \eta\, V_1 \tag{4.3}$$

4.13.3 BASIC TRIGGER CIRCUIT



Basic Unijunction Transistor Relaxation Oscillator—Trigger Circuit with Typical Waveforms
Figure 4.12

The basic UJT trigger circuit used in applications with the SCR is the simple relaxation oscillator shown in Figure 4.12. In this circuit, the capacitor C_1 is charged through R_1 until the emitter voltage reaches V_P at which time the UJT turns on and discharges C_1 through R_{B1}. When the emitter voltage reaches a value of about 2 volts, the emitter ceases to conduct, the UJT turns off and the cycle is repeated. The period of oscillation, T, is fairly independent of the supply voltage and the temperature and is given by:

$$T = \frac{1}{f} \cong R_1 C_1 \ln \frac{1}{1-\eta} = 2.3 R_1 C_1 \log_{10} \frac{1}{1-\eta} \tag{4.4}$$

The design conditions of the UJT firing circuit are very broad. In general, R_{B1} is limited to a value below 100 ohms although values up to 2 or 3 K are possible in some applications. The resistor R_1 is limited to a value between 3K and 500K. The lower limit on R_1 is set by the requirement that the load line formed by R_1 and V_1 intersect the emitter characteristic curve of Figure 4.11 to the left of the valley point, otherwise the UJT in Figure 4.12 will not turn off. The upper limit on R_1 is set by the requirement that the current flowing into the emitter at the peak point must be greater than I_P for the UJT to turn on. The recommended range of supply voltage V_1 is from 10 volts to 35 volts. This range is determined on the low end by the acceptable values of signal amplitude and at the high end by the allowable power dissipation of the UJT.

If the pulse output (V_{B1}) of the circuit of Figure 4.12 is coupled directly or through series resistors to the gates of the SCR's, the value of R_{B1} should be low enough to prevent the DC voltage at the gate due to interbase current from exceeding the minimum gate firing voltage for the SCR's at the maximum junction temperature at which the SCR's are expected to operate. To meet this criterion, R_{B1} should be chosen in accordance with the following inequality:

$$\frac{R_{B1} V_1}{R_{BB}(\min) + R_{B1} + R_{B2}} < V_{GF}(\min) \tag{4.5}$$

For the 2N681 at a maximum junction temperature of 125°C, V_{GF} (min) is 0.25 volt, hence for a supply voltage of 35 volts or less, R_{B1} should be 50 ohms or less. If the pulse output from the UJT firing circuit is coupled to the gates of the SCR's by means of transformers or capacitors, these limitations do not apply.

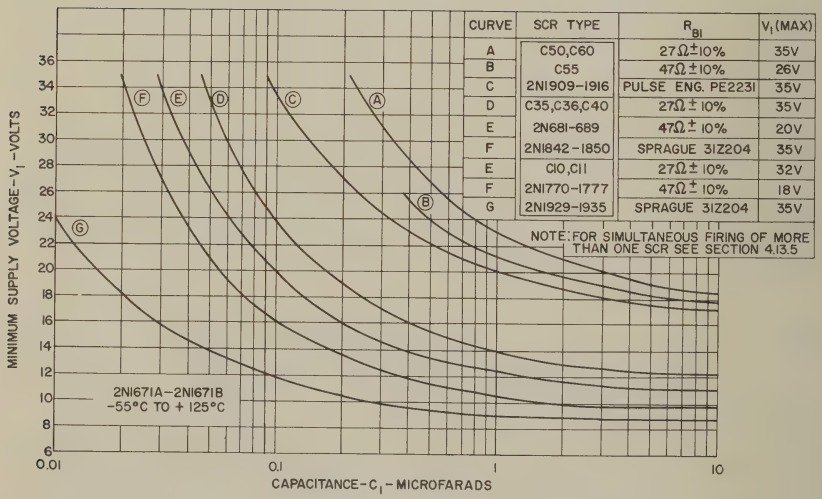
4.13.4 DESIGNING THE UNIJUNCTION TRANSISTOR FIRING CIRCUIT

The type 2N1671A and 2N1671B UJT are specifically characterized for SCR firing circuits and are 100% factory tested to ensure reliable operation with all types of G-E SCR's over their respective temperature ranges. Their specifications are given in Chapter 17. For both the 2N1671A and the 2N1671B a base one peak pulse voltage, V_{OB1}, is specified as 3.0 volts minimum when measured in a circuit similar to Figure 4.12 with $C_1 = 0.20$ μfd, $R_{B1} = 20\ \Omega$, $R_{B2} = 100\ \Omega$, $R_1 \geqq 5$K, and $V_1 = 20$ volts. The 2N1671B in addition has lower

limits on peak point current (I_P = 6 μa max.) and emitter leakage current (I_{EO} = 0.2 μa max.) which make it ideally suited for use in sensitive timing and trigger circuits. Condensed specifications for the 2N1671, 2N1671A, and 2N1671B are given in the specification section of this manual.

The design of a suitable SCR firing circuit can be achieved rapidly and easily by using the design curves given in Figure 4.13. These curves give the minimum supply voltage required to guarantee firing of the various types of SCR's over the temperature range of −55C to +125C as a function of the UJT emitter capacitor, C_1, and the base-one coupling resistor, R_{B1}, or base-one coupling transformer. SCR's can be fired at higher temperatures than 125°C consistent with their ratings using the curves given in Figure 4.13 provided that direct coupling to the gates is not used (i.e., capacitor or pulse transformer coupling must be used). The value of the resistor R_1 is not important for the purposes of the design provided that it is within the limits required for the UJT to oscillate. The value of R_{B2} is not important provided that it is equal to or less than 100 Ω. If R_{B2} is significantly greater than 100 Ω the minimum supply voltage which is assumed (V_1') should be calculated from the minimum supply voltage (V_1) given by Figure 4.13 using the equation:

$$V_1' = \frac{(2200 + R_{B2})\, V_1}{2300} \tag{4.6}$$



CURVE	SCR TYPE	R_{B1}	V_1 (MAX)
A	C50,C60	27Ω±10%	35V
B	C55	47Ω±10%	26V
C	2N1909-1916	PULSE ENG. PE2231	35V
D	C35,C36,C40	27Ω±10%	35V
E	2N681-689	47Ω±10%	20V
F	2N1842-1850	SPRAGUE 31Z204	35V
E	C10,C11	27Ω±10%	32V
F	2N1770-1777	47Ω±10%	18V
G	2N1929-1935	SPRAGUE 31Z204	35V

NOTE: FOR SIMULTANEOUS FIRING OF MORE THAN ONE SCR SEE SECTION 4.13.5

SCR/UJT Firing Circuit Design Curves
Figure 4.13

It is recommended in all cases that series resistance of 100 Ω or greater be used in series with either base-two or in series with the power supply to protect the UJT from possible thermal runaway. This is particularly important when operating at high ambient temperatures, at high supply voltages, or with large values of emitter capacitance.

As an example of the use of Figure 4.13 in the practical design of an SCR firing circuit, consider the following problem:

Example: A circuit is required to fire a type 2N1773 SCR at the lowest possible supply voltage. Assume that the value of capacitance, chosen on the basis of operating frequency, is 0.2 μf and that the value of the base-two resistor, chosen for temperature compensation, is 180 Ω.

Solution: From Figure 4.13 it is seen that a minimum supply voltage is obtained with a 47 Ω resistor (i.e., curve F lies below curve E). On curve F it is seen that the minimum voltage for $C_1 = 0.2$ μf is 13.6 volts. Correcting this value to take into account the value of R_{B2}, Equation 4.6 gives $V_1' = (1.03)(13.6) = 14$ volts. From the chart given on Figure 4.13 it is seen that the maximum allowable supply voltage is 18 volts (if the supply voltage is greater than 18 volts the SCR may be fired by the DC voltage across R_{B1} at an elevated temperature). Thus a suitable design for the firing circuit of the example would be $C_1 = 0.2$ μf, $R_{B2} = 180$ Ω, $R_{B1} = 47$ Ω ±10%, $V_1 = 16$ volts ±2 volts.

4.13.5 PARALLEL FIRING

If two or more SCR's must be fired in parallel by a single UJT the design of the firing circuit must take into consideration the possibility that an SCR with a low gate resistance may be paralleled with an SCR having a high gate resistance, thus loading down the output pulse sufficiently to prevent the second SCR from being fired. To reduce this possibility it is recommended that the trigger pulse be coupled by means of a separate capacitor to each SCR gate. These capacitors act to equalize the charge coupled to each gate during the trigger pulse and thus tend to reduce the effects of unequal loading. The optimum value of capacitor for this purpose has been found to be 0.1 μf. In addition to this capacitor, a resistor having a value of 220 Ω to 1K should be connected between gate and cathode of each SCR.

Using this approach of equalizing capacitors the design curves of Figure 4.13 can be used for parallel firing of SCR's provided that the minimum supply voltage is multiplied by a factor of 1.50 if two SCR's are to be fired in parallel and by a factor of 1.80 if three SCR's are to be fired in parallel. Since the gates are not direct coupled, the maximum supply voltage allowed is limited only by the 35 volt rating of the UJT.

Alternatively, a larger value of base-one resistance, R_{B1}, can be used to reduce the otherwise required increase in value of supply voltage for parallel filing. For example, if $R_{B1} = 100$ Ω, and using equalizing capacitors, the curves for $R_{B1} = 27$ Ω apply for firing two SCR's in parallel with no increase in supply voltage. For firing three SCR's in parallel under this condition the supply voltages given by these curves should be increased by a factor of 1.25.

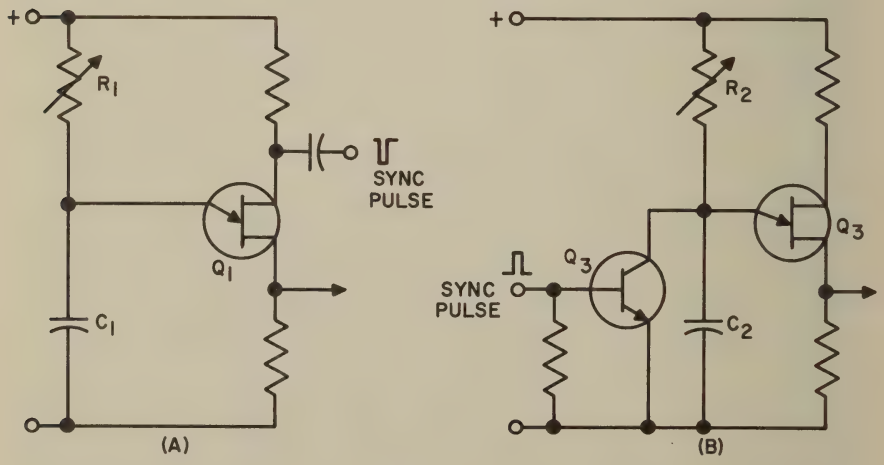
4.13.6 TRANSFORMER COUPLING

If DC isolation is required between the trigger circuit and the SCR's, transformer coupling can be used. Generally small pulse transformers are adequate for this purpose. The optimum turns ratio is about 1:1 and the primary inductance should be 6 millihenries or more. The Sprague type 31Z204 or equivalent (1:1) performs satisfactorily for this purpose, giving an output pulse which has a voltage only 10% less than the direct-coupled case. If two isolated outputs are desired a similar transformer with three windings can be used, such as the Sprague 31Z286 or equivalent (1:1:1).

4.13.7 SYNCHRONIZATION METHODS

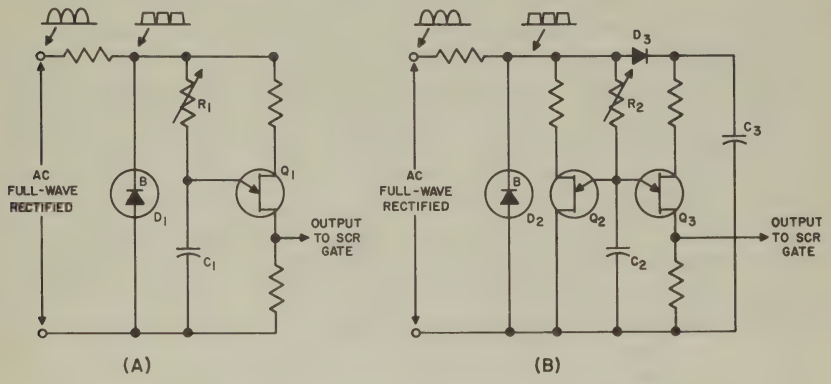
In the basic trigger circuit of Figure 4.12, the UJT can be fired at any intermediate part of the cycle by reducing either the interbase voltage or the supply voltage, V_1. This results in an equivalent decrease in V_P in accordance with Equation 4.3 and causes the UJT to fire if V_P drops below the instantaneous value of V_E. Thus the base-two terminal or the main supply voltage can be used to synchronize the basic trigger circuit. Figure 4.14(A) illustrates the use of a negative synchronizing pulse at base-two.

Another synchronization method is illustrated in Figure 4.14(B). An NPN transistor, Q_2, is used in shunt with the emitter capacitor, C_2. A positive current pulse at the base of Q_2 will discharge C_2 and delay the firing of the UJT. This circuit can also be used for clamping the voltage at the emitter of the UJT. As long as a positive current is maintained into the base of Q_2, no voltage will be developed across C_2. When the base current is removed, the voltage across C_2 will rise and the UJT will fire at the end of the time interval determined by the values of R_2 and C_2.



Circuits for Pulse Synchronization of UJT Relaxation Oscillator
Figure 4.14

Two methods of achieving synchronization with the AC line are illustrated in Figure 4.15. A full wave rectified signal obtained from a rectifier bridge or similar source is used to supply both power and synchronizing signal to the firing circuit. The zener diodes, D_1 and D_2, are used to clip and regulate the peaks of the AC as indicated in Figure 4.15.



Circuits for Synchronization to AC Line
Figure 4.15

At the end of each half cycle the voltage at base-two of Q_1 and Q_2 will drop to zero, causing Q_1 and Q_2 to fire. The capacitors are thus discharged at the beginning of each half cycle and the firing circuits are thus synchronized with the line. In Figure 4.15(A) a pulse is produced at the output at the end of each half cycle which can cause the SCR to fire and produce a small current in the load. If this is undesirable, a second UJT can be used for discharging the capacitor at the end of the half cycle as illustrated in Figure 4.15(b). Diode D_3 and capacitor C_3 are used to supply a constant DC voltage to Q_3. The voltage across Q_2 will drop to zero each half cycle causing C_2 to be discharged through Q_2. The UJT's should be chosen so that Q_2 has a higher standoff ratio than Q_3.

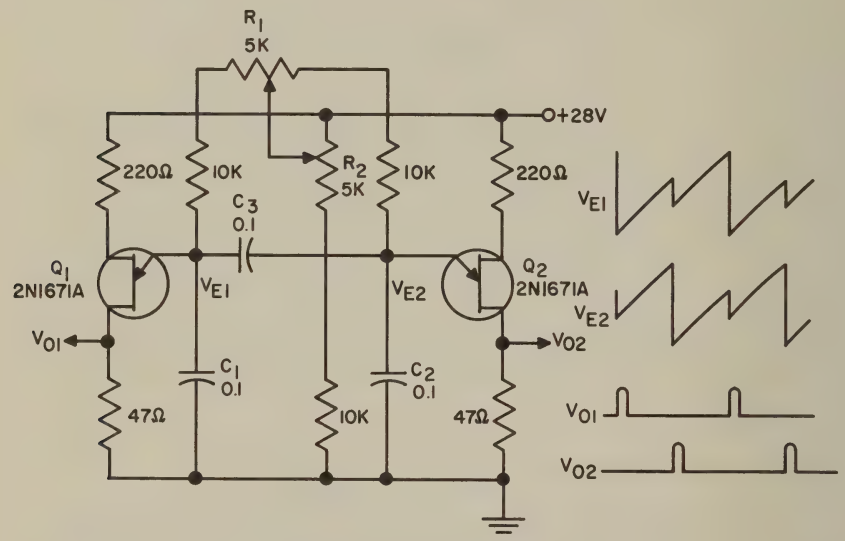
4.14.1 INVERTER FIRING CIRCUITS

For triggering some types of SCR parallel inverter circuits, a generator is desired which will produce trigger signals alternately at two outputs. The trigger signals can be either square waves or pulses depending on the circuit requirements. A pulse signal is generally preferable since it requires a minimum of power from the trigger circuit. A square wave signal is required for some types of parallel inverters operating with inductive loads.

4.14.2 UJT CIRCUIT FOR GENERATING ALTERNATE PULSES

Figure 4.16 shows a versatile UJT circuit which can be used for the generation of alternate pulses. This circuit consists of two UJT relaxation oscillator

circuits which are synchronized by the capacitor C_3. Each time one UJT fires a negative voltage step is coupled to the emitter of opposite UJT through the capacitive voltage divider formed by C_3 and C_1 or C_3 and C_2. If this negative voltage step occurs when the emitter voltage is low the delay in the firing of the UJT will be less than if the step occurs when the emitter voltage is high, owing to the non-linear charging characteristic of the capacitor. This effect produces the synchronization between the two oscillators. The frequency of oscillation and the relative spacing between the pulses from the two outputs are controlled independently by potentiometers R_2 and R_1, respectively. For the circuit shown, the frequency can be adjusted between 200 cps and 800 cps and the relative pulse spacing can be varied from 35% to 65%. The range of control of pulse spacing can be increased by reducing the size of C_3 relative to C_1 and C_2. The size of C_3 relative to C_1 and C_2 also determines the initial timing of the pulses when the power is first applied. If C_3 is the same size as C_1 and C_2, the circuit will start with the same timing sequence that it has under steady state conditions (50% pulse spacing). This characteristic is very important for the reliable starting of parallel inverters.

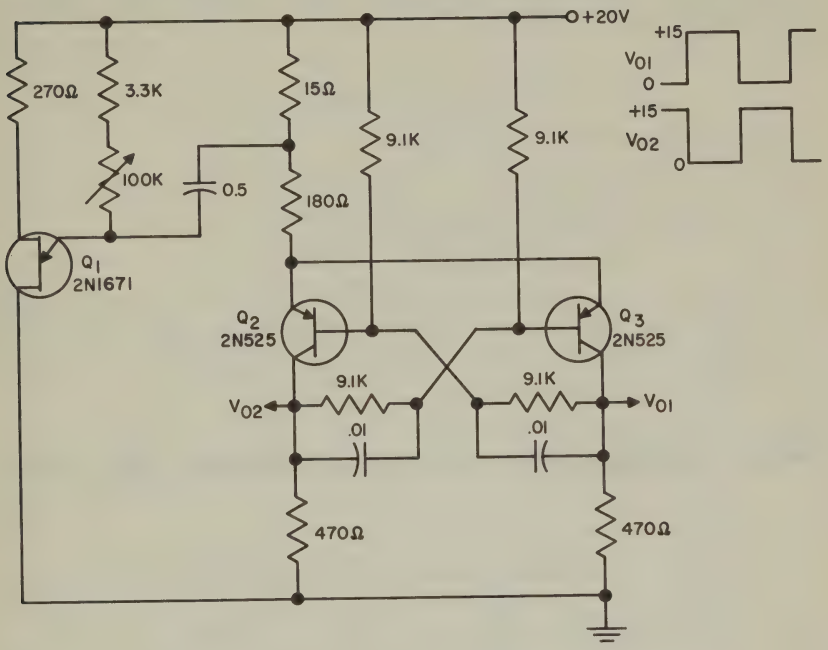


UJT Circuit for Generating Alternate Pulses
Figure 4.16

4.14.3 HYBRID SQUARE WAVE MULTIVIBRATOR

Figure 4.17 shows a circuit for generating a square wave from two outputs. This circuit is an example of the hybrid multivibrator which is described fully in the UJT application notes (ECG-380). Transistors Q_2 and Q_3 form a simple flip-flop which is triggered by the UJT operating as a relaxation oscillator. Negative trigger pulses are generated across the 15 Ω resistor each time the

UJT fires. The frequency of oscillation can be varied by the 100K potentiometer from approximately 20 cps to 600 cps. The waveform remains perfectly symmetrical over the full frequency range. The circuit will operate up to a temperature of 75°C. Higher temperatures are possible if silicon transistors are used for Q_2 and Q_3.



Hybrid Multivibrator for Generating Square Waves
Figure 4.17

If transformer coupling to the gates is desired, the primary of the transformer can be connected in place of the collector resistors.

4.15.1 PHASE CONTROL FIRING CIRCUITS

Simple phase control circuits can be obtained by using a PNP or NPN transistor in series or in shunt with the emitter capacitor of the UJT firing circuit. The amount of current in the base of the transistor will control the effective charging current to the capacitor and hence will control the firing angle of the UJT and SCR. Several examples of this type of circuit are described in Chapter 8.

4.15.2 SHUNT TRANSISTOR CONTROL OF UJT

Referring to the circuit of Figure 8.2 in Chapter 8, it is seen that NPN transistor Q_2 shunts some of the charging current supplied to capacitor C_1 by

resistor R_2 in an amount dependent on the base drive of Q_2. The more Q_2 is turned on, the later UJT will fire, and the lower the output of the SCR's will be.

By fixing the value of R_2 at approximately 2500 Ω, base current i_B will then control the diversion of charging current from C_1 and retard or advance the firing angle accordingly. The UJT will be prevented from firing, and essentially zero output will occur across the load if i_B in amperes is increased to approximately the following value:

$$i_B \geqq \frac{V_1}{(\beta)(R_2)}(1-\eta) \quad \text{if} \quad \frac{1}{2f(R_2)(C_1)} > 4$$

where V_1 = avalanche voltage of CR_5

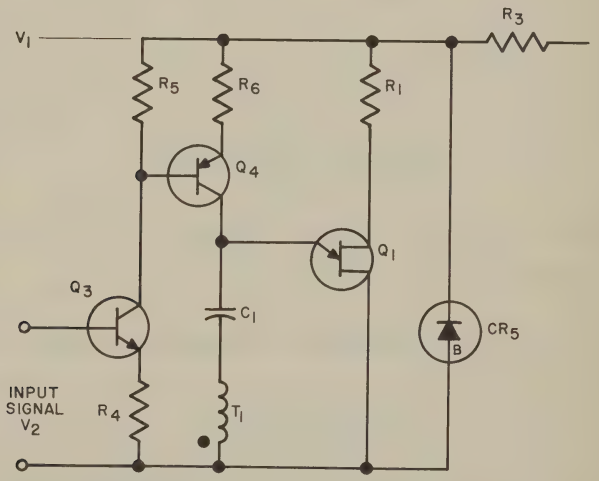
β = common emitter current gain of Q_2

η = intrinsic standoff ratio of Q_1

C_1 = UJT capacitor, farads

For values of i_B less than this value, the SCR output increases rapidly. This type of shunt transistor control of the UJT and SCR firing angles is characterized by very high gain. Power gain between the base drive of Q_2 and the load on the order of 10^8 is readily attainable.

4.15.3 SERIES TRANISTOR CONTROL OF UJT



Q_3 – G–E 2N167
Q_4 – G–E 2N524
R_4 – 2500 OHMS
R_5 – 200 OHMS
R_6 – 1000 OHMS

OTHER VALUES SAME AS IN FIGURE 8.2 IN CHAPTER 8

Series Transistor Control of UJT Firing Angle
Figure 4.18

For a more linear transfer characteristic at the expense of power gain, a transistor in series with C_1 instead of in shunt with it can be used to regulate the charging rate of this capacitor and thereby control the firing angle. Such a firing circuit is shown in Figure 4.18. An additional NPN transistor Q_3 is required if it is desired to keep one side of the input signal at the potential of the lower line. If the resistors in this circuit are selected so that both Q_3 and Q_4 operate as emitter follower stages, the transfer characteristic can be approximated as follows:

$$\frac{e_o}{e_{max}} = \frac{1}{2} + \frac{1}{2}\cos\frac{2\pi f\eta(V_1)(C_1)(R_6)(R_4)}{(R_5)(V_2)}$$

where e_o = average value of voltage across load

e_{max} = maximum theoretical average value of voltage across load when no firing angle delay occurs

f = supply frequency, cps

Zero output voltage across the load will occur when:

$$V_2 = \frac{2f\eta(V_1)(C_1)(R_6)(R_4)}{(R_5)}$$

These types of firing angle control using the UJT can be used to regulate the output of SCR's in many other phase-controlled circuits, examples of which are shown in Chapter 8.

4.16.1 DIFFERENTIAL AMPLIFIERS

Differential amplifiers offer advantages in some types of phase control circuits. Some of the practical benefits which might be expected from the use of differential amplifiers would include:

(1) In circuits where the amplifier must work from a source having a low output impedance (1K or less) the differential amplifier offers considerably more stability with respect to changes in temperature than the simple direct-coupled amplifier. This occurs since the base to emitter voltage change with temperature is compensated for in the differential amplifier configuration.

(2) The control threshold of the differential amplifier may be adjusted as desired and will remain independent of ambient temperature. This means, for example, that the input voltage to a differential amplifier using silicon transistors may initiate control action of 0.10 volts or less rather than a 0.70 volt as required for the conventional direct-coupled circuit.

(3) A simple reversing type control can be made using the differential amplifier which may be operated from an electrical signal at a single input and which has a precisely determined deadband.

(4) Simple and sensitive reversing type phase detector controls can be made using the differential amplifier.

(5) Either linear type controls or full on-full off type controls can be made using the differential amplifier.

The basic differential amplifier circuit is shown in Figure 4.19 below.

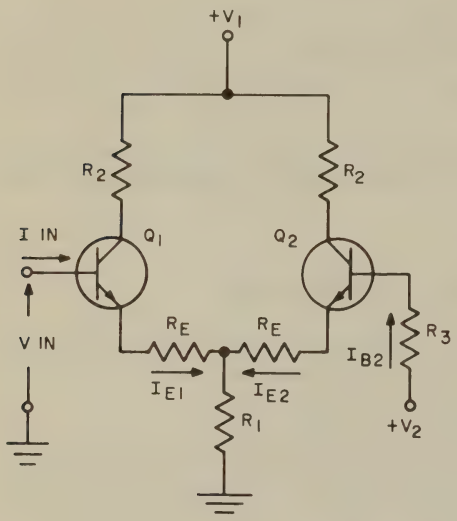
An exact analysis of this circuit is generally too complex to be of practical value. Several simplifying assumptions can be made which do not seriously affect the accuracy of the analysis for the type of application considered here. The assumptions which are made are:

(1) The common base input characteristic of the transistor is used in the analysis. This characteristic is generally quite uniform for different transistors of the same type. This input characteristic is assumed to be linear as indicated in Figure 4.20 and is assumed to be independent of the collector voltage. The slope of the characteristic is R_E and the intercept of the V_{BE} axis is V_{BO}.

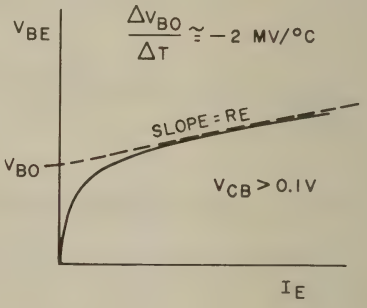
(2) The value of R_E and V_{BO} is assumed to be the same for both transistors.

(3) The current gain of the two transistors is assumed to be independent of emitter current and collector voltage ($\because \alpha \equiv h_{fb} = f_{FB}$).

(4) For both transistors h_{oe} (output admittance) is assumed to be zero and h_{re} (reverse voltage transfer ratio) is assumed to be zero.



Basic Differential Amplifier Circuit Figure 4.19



Common Base Input Characteristics (Actual and Assumed) Figure 4.20

As indicated in Figure 4.19 the input resistance R_E is included in the circuit external to the transistors. Any additional circuit resistance in series with the emitters can be included with R_E.

The ratio of input voltage to emitter current is given by:

$$R'_{in} = \frac{\Delta V_{in}}{\Delta I_{E1}} = R_1 \frac{(R_E + (1 - \alpha_2) R_3)}{(R_1 + R_E + (1 - \alpha_2) R_3)} + R_E \qquad (4.6)$$

where: $R_A = R_1 + R_E + (1 - \alpha_2) R_3$

For the case where $R_1 >> R_E + (1 - \alpha_2) R_3$ then:

$$V_{in} = V_2 + R_3 I_{CO} + [2 R_E + (1 - \alpha_2) R_3] I_E \qquad (4.7)$$

$$R'_{in} = \frac{\Delta V_{in}}{\Delta I_{E1}} = 2\,R_E + (1 - \alpha_2)\,R_3 = -\frac{\Delta V_{in}}{\Delta I_{E2}} \tag{4.8}$$

The input impedance of the circuit is given by:

$$R_{in} = \frac{\Delta V_{in}}{\Delta I_{in}} = \frac{\Delta V_{in}}{\Delta I_{E1}} \frac{\Delta I_{E1}}{\Delta I_{in}} = \frac{R'_{in}}{1 - \alpha_1} \tag{4.9}$$

Which for the case where $R_1 >> R_E + (1 - \alpha_2)\,R_3$ gives:

$$R_{in} = \frac{2\,R_E}{1 - \alpha_1} + \frac{(1 - \alpha_2)}{(1 - \alpha_1)}\,R_3 \tag{4.10}$$

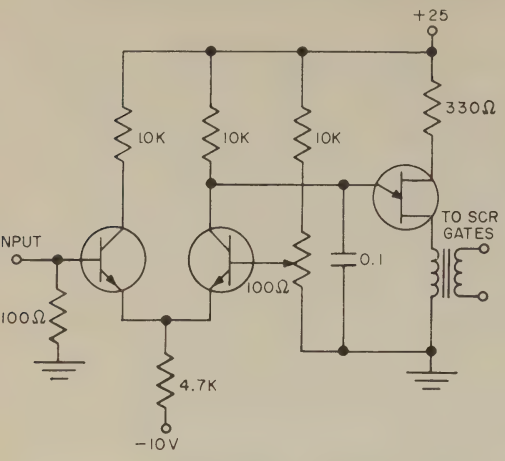
4.16.2 BASIC PHASE CONTROL CIRCUIT WITH THE DIFFERENTIAL AMPLIFIER

In the types of applications considered in this section, it is helpful to consider the differential amplifier from the following viewpoint: over the normal range of operation resistor R_1 is considered as a source of constant current to the emitters of the two transistors. The value of current is given by $(V_2 - V_{BO})/(R_1 + \frac{1}{2} R_E) = I_1$. The input voltage, V_{in}, serves to control the portion of I_1 flowing in each collector. When V_{in} reaches a value high enough to cause all of I_1 to flow in the collector of Q_1, the input resistance of the circuit will increase from the value given by Equation 4.9 to a value of approximately $R_1/(1 - \alpha_1)$. In the normal range of operation the characteristic of the circuit is given by Equation 4.6 or Equation 4.8 and the input resistance of the circuit is given by Equation 4.9 or Equation 4.10.

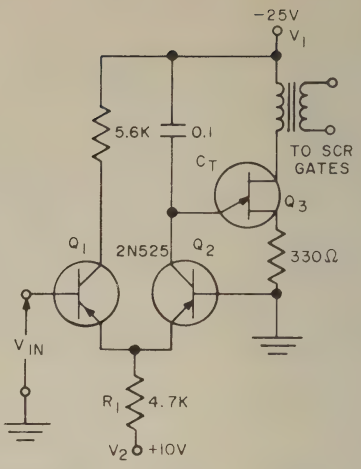
A simple phase control circuit using NPN transistors in a differential amplifier circuit is shown in Figure 4.21. This circuit uses a 100 ohm pot for adjusting the voltage level of the control circuit. With the circuit as shown, an increase in the input voltage level will cause a decrease in the firing angle of the UJT and the SCR's. Note that the opposite effect can be obtained by interchanging the connections to the collectors of the two transistors. The circuitry required for synchronizing the control circuit to the line is not shown in Figure 4.21 or 4.22, but this circuitry can be similar to that described in the section on synchronization methods.

Figure 4.22 illustrates the use of PNP transistors in control circuits. The control voltage of this circuit is zero since the base of Q_2 is connected to ground. This circuit is superior to the NPN circuit of Figure 4.21 since the control is more linear. This occurs because the capacitor in Figure 4.22 is charged from a current source (i.e., the output impedance of the transistor Q_2 is very high.) For this circuit, the period is given by:

$$\tau = \frac{\eta\,V_1 C_T}{I_{E2}} \cong \eta\,V_1 C_T \left[\frac{V_{in}}{R_{in}} + \frac{V_2}{2R_1}\right]^{-1} \tag{4.11}$$



Basic Differential Amplifier Circuit Using NPN Transistors
Figure 4.21

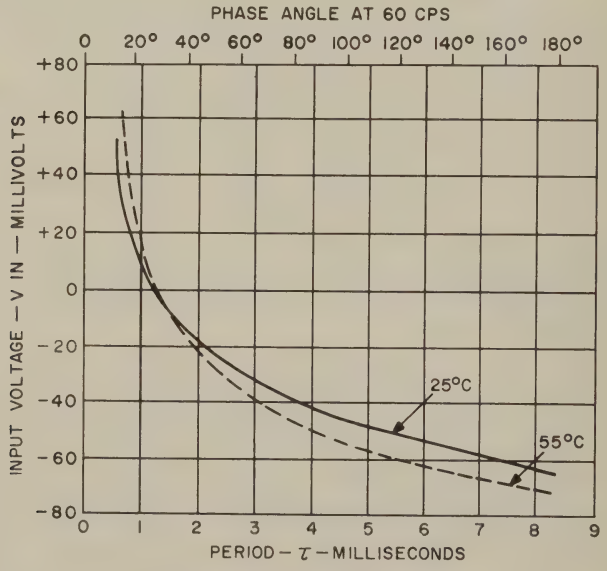


Basic Differential Amplifier Circuit Using PNP Transistors
Figure 4.22

and the minimum period is given by:

$$\tau\,(\min) = \frac{\eta\, V_1 R_1 C_T}{V_2} \tag{4.12}$$

The variation of period with input voltage for the circuit of Figure 4.22 is shown in Figure 4.23 at ambient temperatures of 25°C and 55°C.

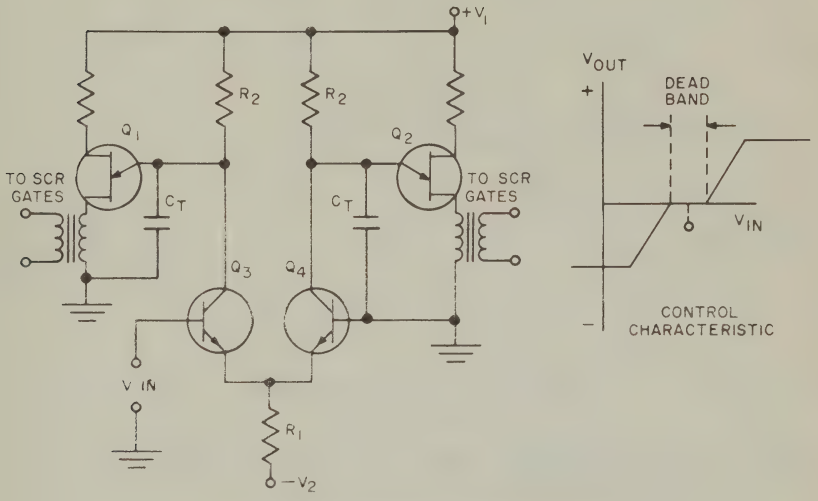


Control Characteristics of Circuit Shown in Figure 4.22
Figure 4.23

4.16.3 REVERSING TYPE CONTROL CIRCUIT

A basic circuit for a reversing type control is shown in Figure 4.24. This circuit shows the voltage reference as ground, but a variable reference voltage may also be used. This circuit can also use the PNP differential amplifier if desired.

The circuit is designed in such a way that for any value of input voltage only one of the UJT's can fire during a half cycle. If the SCR's are used in a full-wave bridge, the UJT which fires will determine the phase angle and the direction of current flow through the load. If the input voltage is reversed in polarity, the opposite UJT will fire and the current will flow through the load in the opposite direction.



Basic Control Circuit for Reversing Type Applications
Figure 4.24

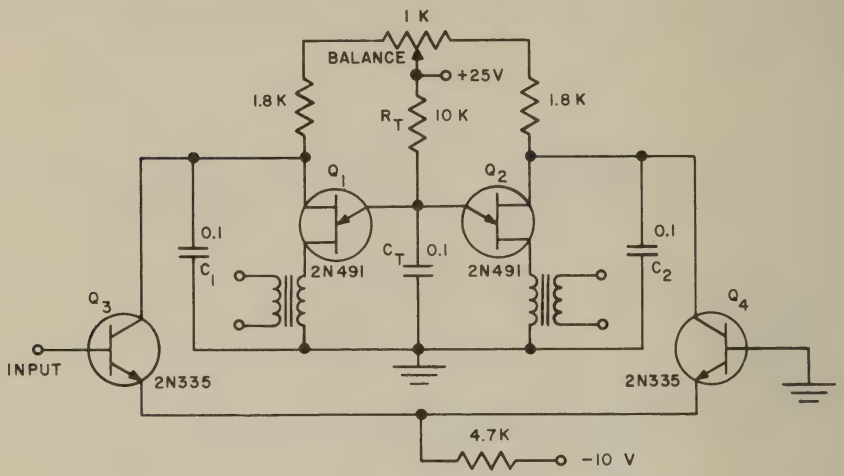
For suitably small values of input voltage, the output from the circuit will be zero since the firing of both UJT's will be delayed for more than a half cycle. The width of this "dead band" can be chosen as desired by means of the component values in Figure 4.24. For example, the dead band can be varied by means of R_1, increasing R_1 will increase the width of the dead band.

4.16.4 ON-OFF TYPE CONTROL CIRCUITS

In some types of applications, an on-off type of control is required rather than a linear control. A circuit which gives this characteristic is shown in Figure 4.25. As the capacitor C_T is charged, either UTJ Q_1 or Q_2 will fire, depending on which one has the lower peak point voltage. The peak point voltage of the two units is varied by controlling the interbase voltages with the differential

amplifier as shown. For the circuit shown in Figure 4.25, the UJT which fired could be controlled by an input voltage change of 4 millivolts. The temperature stability is very good since the circuit is completely symmetrical.

The capacitors C_1 and C_2 are required to prevent one UJT from triggering the other with the pulses developed across the power supply impedance. If these capacitors are eliminated, both UJT's can fire at the same time and as the input voltage is varied the pulse amplitude for one UJT will increase as the pulse amplitude for the other UJT decreases. This would be a serious problem if a reversing type control was used.



On-Off Type Control Circuits
Figure 4.25

4.17.1 R-C-DIODE FIRING CIRCUITS (CONTINUOUS CONTROL)

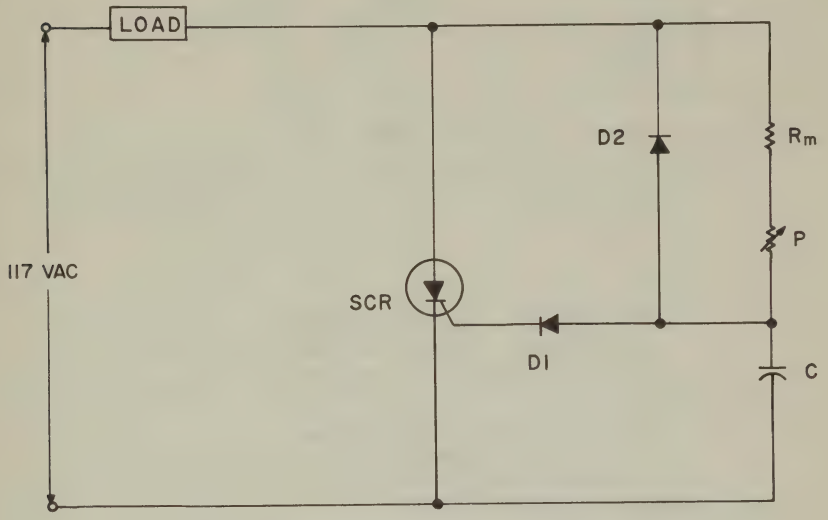
It is sometimes required to find the simplest and most economical means for firing an SCR when some performance compromise can be made, particularly with regard to repeatibility over a temperature range. Simple resistor-capacitor-diode combinations will fire and control SCR's over the full 180 electrical degree range, giving very good performance at commercial temperatures.

Since in a scheme of this type a resistor will usually have to supply all of the gate drive required to turn on the SCR, these types of circuits operate most satisfactorily with SCR's having fairly good gate sensitivities. The less sensitive the gate, the lower resistance must be the resistor, and the greater will have to be its wattage rating.

4.17.2 HALF-WAVE R-C-DIODE CIRCUIT

Figure 4.26 shows an R-C-Diode circuit giving full half-cycle control (180 electrical degrees).

On the positive half-cycle of SCR anode voltage the capacitor will charge to the firing point of the SCR in a time determined by the RC time constant and the rising anode voltage. On the negative half-cycle, the top plate of the capacitor charges to the peak of the negative voltage cycle, thus resetting it for the next charging cycle.



SCR : GE 2N1774 — R_m: 470Ω

D1 : GE 1N678 — P : 40KΩ

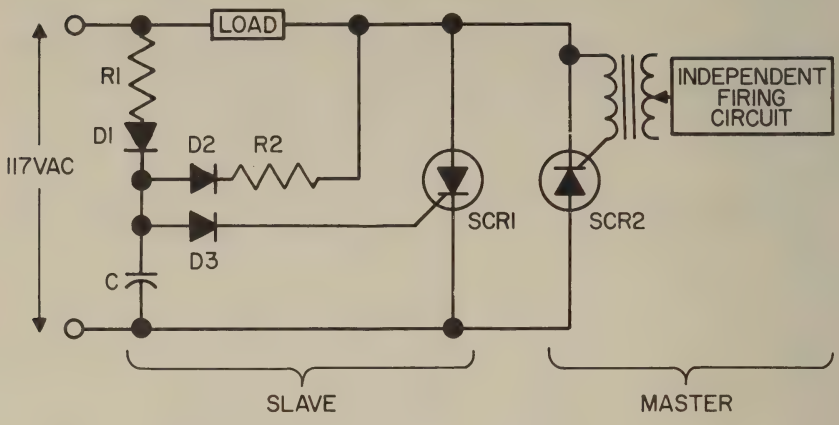
D2 : GE 1N681 — C : .25 MFD

Half-Wave R-C-Diode Circuit
Figure 4.26

4.17.3 RC DIODE SLAVING CIRCUIT

Figure 4.27 illustrates a slave circuit arrangement in which an independent half-wave circuit (SCR_2) is fired on one half-cycle at a predetermined phase angle. On the following half-cycle the slave circuit will fire SCR_1 at the same phase angle relative to that half-cycle.

When SCR_2 does not fire, capacitor C will charge and discharge to the same voltage at the same time constant. The voltage across C will not be sufficient to fire SCR_1. As SCR_2 is fired, capacitor C on discharging sees a time integral of line voltage that is different from the one on charging by the time integral of voltage appearing across the load. This action resets the capacitor to a voltage level related to the firing delay angle of SCR_2. On the next half-cycle, when the anode of SCR_1 swings positive, it will fire at the end of this delay angle.



R1 : 15K D1, D2 : GE IN678
R2 : 15K SCR1,2 : GE 2N1774
C : 5 MFD D3 : GE IN676

R-C-Diode Slaving Circuit
Figure 4.27

4.17.4 SIMPLIFIED UJT FIRING CIRCUIT (HALF-WAVE)

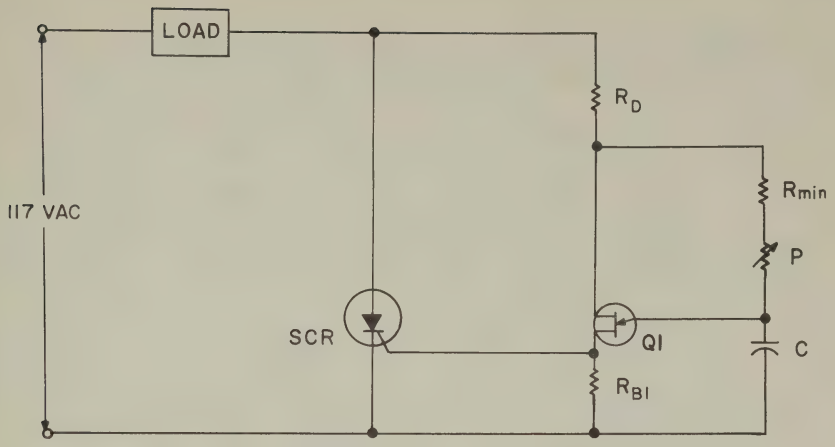
The basic unijunction transistor firing circuit was discussed in Section 4.13. A simplified type of firing circuit results if base two and the emitter timing circuit of the UJT are supplied directly from the line by way of a dropping resistor, R_D, which keeps the peak voltage on the UJT within its specifications.

Figure 4.28 shows this circuit with values given for operation from a 117 VAC supply. The voltage across capacitor C will rise to a value determined by the time constant of the circuit. When it reaches the peak point voltage the UJT will fire and in turn trigger the SCR.

4.17.5 SIMPLIFIED FULL-WAVE UJT FIRING CIRCUITS

The circuit of Figure 4.28 can be extended to full-wave operation by the addition of another SCR and its own UJT trigger (Figure 4.29) or by the addition of a diode rectifier and a switch (Figure 4.30).

In Figure 4.29 two of the basic circuits of Figure 4.28 have been placed back-to-back. The emitters of the two UJT's have been cross-coupled with a network that exerts full cycle phase control over both SCR's. Where only manual control is required, this circuit trades off a pulse transformer and an avalanche diode for an additional low cost UJT compared to the basic full-wave UJT circuit discussed earlier.



SCR : GE2N1774
Q1 : GE2N1671A
R_D : 33 KΩ

R_{min} : 3.3KΩ
P : 50KΩ
C : 0.1 MFD
R_{B1} : 47Ω

Simplified Unijunction Transistor Firing Circuit
Figure 4.28

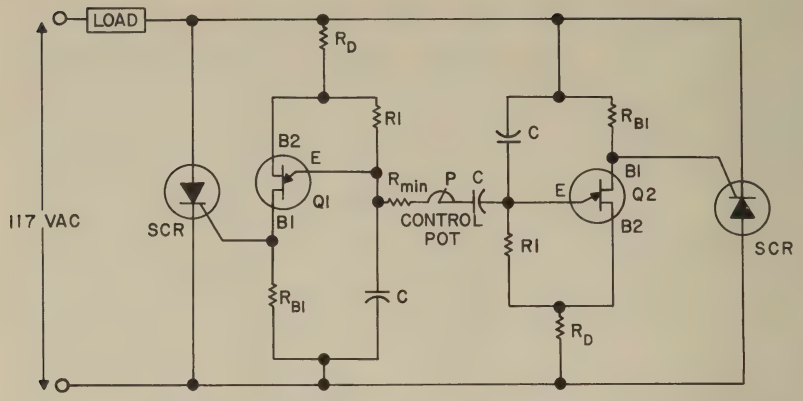
Figure 4.29 gives a lower cost version of a full-wave UJT circuit with only one UJT but requiring a center-tapped potentiometer, P, and a double-pole-double-throw switch, DPDT.

With DPDT in the "dotted" position, potentiometer P can be turned up to lower resistance values until the SCR fires for a full half-cycle. Diode D_1 resets the voltage on capacitor C to essentially zero. Continuing the travel of the potentiometer arm throws DPDT into the "solid" position and simultaneously inserts sufficient resistance in the UJT emitter circuit to cut off the SCR. Diode D_1 now bypasses all negative half-cycles to the load and also continues to reset the voltage on the capacitor to the same value as before. The SCR has full control over the positive half-cycles to the point at which full wave power is applied to the load.

This type of operation introduces a DC component into the supply lines inherent in all half-wave operation. It will generally not be objectionable whenever the total connected load of this nature is small compared to the normal capacity of the supply line.

4.18 SCR's AS GATE SIGNAL AMPLIFIERS

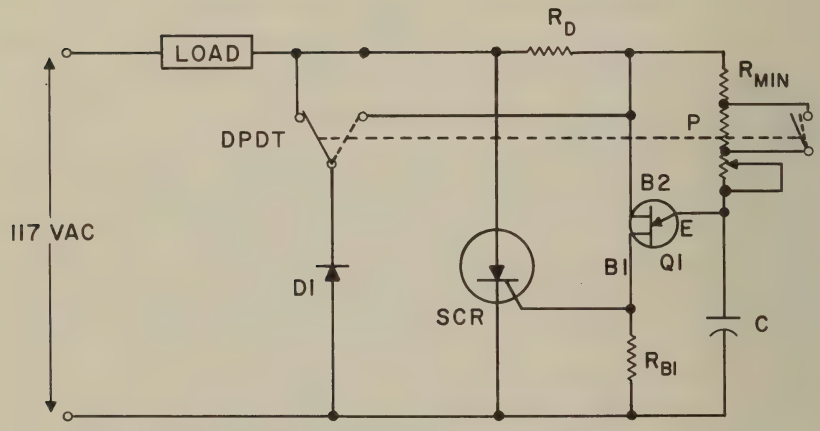
The availability of SCR's with highly sensitive gates permits use of these devices to trigger higher rated SCR's as shown in Figure 4.31. Here a C5B as



SCR: GE 2N1774 (2)
Q1: GE 2N1671A (2)
R_D: 33 KΩ (2)
R_{BI}: 47Ω(2)

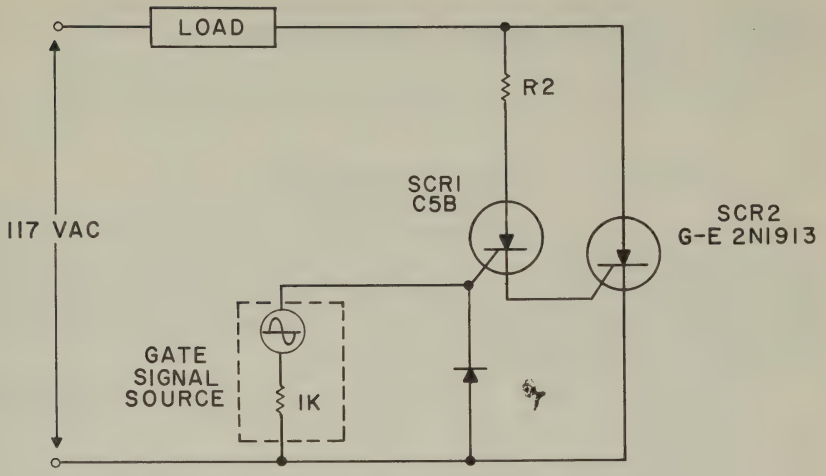
RI: 100KΩ(2)
C: 0.1 MFD (3)
R_{min}: 22 KΩ
P: 500 K Ω

Simplified Full-Wave UJT Firing Circuit
Figure 4.29



SCR	GE 2N1774	C	0.1MFD
Q1	GE 2N1671A	R_{MIN}	3.3KΩ
D1	GE 1N1344A	P	550KΩ (CENTER-TAPPED)
R_D	33KΩ/2W	R_{BI}	47Ω

Simplified UJT Circuit with Auxiliary Diode and Switch for Full-Wave Operation
Figure 4.30



Use of C5 as a Gate Signal Amplifier
Figure 4.31

SCR_1 requires less than 200 microamperes of gate signal to fire. Load current then flows through R_2, SCR_1, and into the gate of SCR_2. When load current reaches the firing requirements of SCR_2, this device turns on and shunts the main power away from SCR_1. In addition to providing a means of triggering high current SCR's by low level signals from high impedance sources, this type of firing yields positive firing from pulsed gate signals even with highly inductive loads due to the much lower holding current requirements of the C5 in comparison with the higher rated SCR's.

R_2 limits current through SCR_1 within its rating. SCR_1 must meet the same voltage requirements as SCR_2. However, its current duty is generally of a pulsed nature, and hence negligible.

REFERENCE

1. "An All-Solid-State Phase Controlled Rectifier System," F. W. Gutzwiller, AIEE Paper CP 59-217, American Institute of Electrical Engineers, New York, N. Y., 1959.

CHAPTER 5

TURN-OFF CHARACTERISTICS AND METHODS

5.1 GENERAL CONSIDERATIONS

SCR circuits that operate from a DC supply have a fundamental difference from those that operate from an AC supply. In AC operation the supply itself turns off the SCR during the negative half-cycle, whereas with a DC supply special turn-off circuitry is required. This turn-off circuitry usually involves a capacitor for storing the required turn-off energy.

The SCR may be turned off by just reducing the current below the holding value, but the turn-off time may then be as long as 100 μsec. The gate will regain control in a shorter time if the SCR is reverse biased with a low impedance external circuit that will permit a reverse current to flow. This permits recovery of the two end junctions in about 2 μsec. Since the center junction is not reverse biased, its recovery is a result of natural recombination of the stored charges. Section 1.4 describes in more detail the physical mechanism by which an SCR turns off and recovers its ability to block forward voltage.

The time t_o, necessary for an SCR to turn off and recover its blocking ability, is a function of the following general environmental and circuitry considerations:

1. Junction temperature (as T_J increases, t_o increases).
2. Level of forward current immediately prior to turn-off and its rate of decay (as I_F and its rate of decay increase, t_o increases). The rate of decay of forward current affects turn-off time because it affects the amount of charge stored within the device when reverse voltage is applied. Rapid decay of forward current results in higher amounts of stored charge which tends to make turn-off time increase. If the decay of forward current is at a rate slower than that at which stored charge can naturally reach equilibrium, then the magnitude of peak forward current has less effect on the turn-off time.
3. Reverse voltage and its rate of rise (as V_R and its rate of rise increase, t_o decreases).
4. Amplitude and rate of rise of forward voltage applied after reverse voltage (as reapplied forward voltage and its rate of rise increase, t_o increases).
5. Turn-off time is also dependent on gate bias conditions. The curve of Figure 5.1 shows the typical effect of gate bias on turn-off time for the C40B SCR. At maximum rated junction temperature of +125°C. the C40 is rated to withstand a positive gate to cathode voltage of 0.25 volts without firing, which dictates one extreme of the curve of Figure 5.1. Although the C40 is rated to withstand negative gate to cathode voltage

of 5.0 volts, little decrease in turn-off time results for negative voltages of more than 2.0 volts.

Negative gate to cathode voltage also increases the capability of the device to withstand rates of rise of reapplied forward blocking voltage higher than the factory tested value of 20 volts per microsecond.

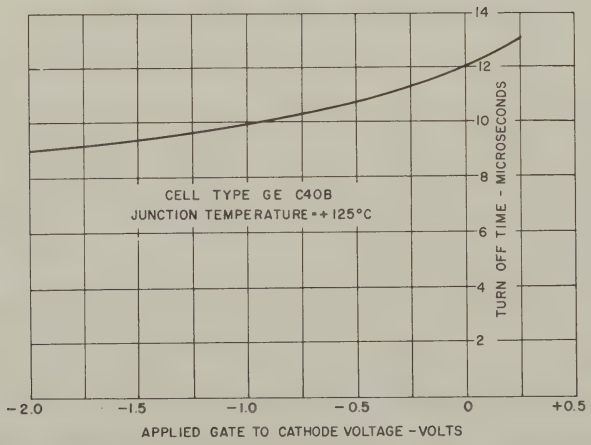
5.2 INVERTER TYPE SCR'S WITH SPECIFIED TURN-OFF TIME LIMITS

Turn-off time (t_o), is defined on the Inverter Type specification sheets as the time measured from the point where the forward current reaches zero to the time of reapplication of forward voltage. A guaranteed maximum t_o permits the circuit designer to design with confidence for maximum efficiency and minimum physical size of the circuit.

G.E.'s FULL LINE OF INVERTER TYPE SCR's

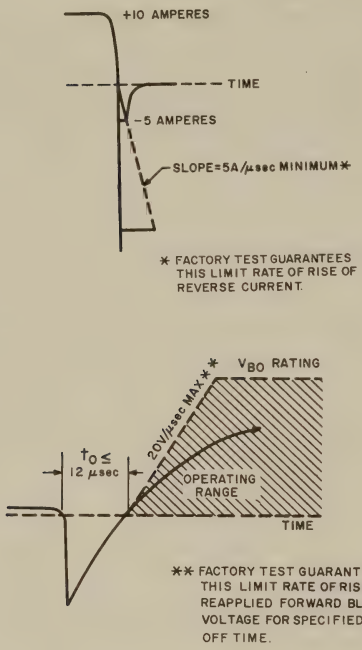
Inverter Type	Maximum Average Current Per SCR (In Inverter Service)	Voltage Ratings Available	Maximum Turn-Off Time*
C9	0.8 Amperes	25 to 300 volts	12 μsec
C12	4.7 Amperes	25 to 300 volts	12 μsec
C40	16 Amperes	25 to 300 volts	12 μsec
C55	70 Amperes	25 to 300 volts	20 μsec

* Under conditions indicated on G-E specification sheets (condensed in "Inverter Type SCR's" section of Chapter 17).



Effect of Gate Bias Condition on Turn-Off Time
Figure 5.1

In addition to all the other tests to which G-E SCR's are subjected, all inverter type SCR's must pass a special turn-off time test. With its junction temperature at the maximum rated value (125°C.), an inverter type SCR must turn off its load current within the specified turn-off time and then block forward voltage reapplied at the rate of 20 volts per μsec. See Fig. 5.2.

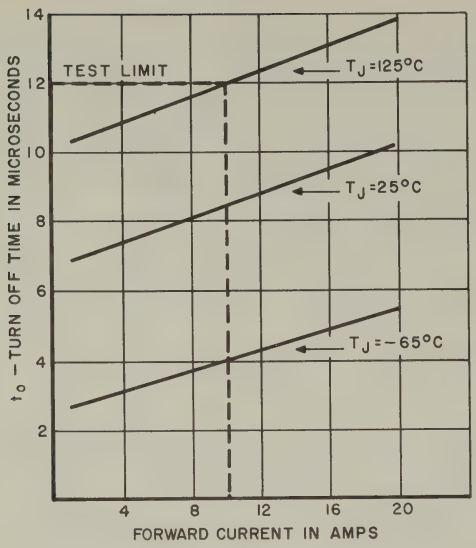

+10 AMPERES
TIME
−5 AMPERES
SLOPE=5A/μsec MINIMUM*
* FACTORY TEST GUARANTEES THIS LIMIT RATE OF RISE OF REVERSE CURRENT.
Current Waveform through SCR
* V_{BO} RATING
20V/μsec MAX.*
$t_o \leq$ 12 μsec
OPERATING RANGE
TIME
** FACTORY TEST GUARANTEES THIS LIMIT RATE OF RISE OF REAPPLIED FORWARD BLOCKING VOLTAGE FOR SPECIFIED TURN-OFF TIME.
Voltage Waveform Across SCR

C40 Turn-Off Time Test Conditions
Figure 5.2

To attain the fastest turn-off time for the inverter type SCR's in equipment design, the peak reverse current during turn-off must be high enough to minimize the reverse recovery time of the SCR. Following the reverse recovery period, the reverse voltage level affects both turn-off time and reapplied voltage rate of rise capability. The factory test condition of −2 volts maximum reverse voltage during this interval assures conservative application where higher reverse voltages may be present as illustrated in Figure 5.2.

The typical variation of turn-off time with junction temperature and forward current is shown by Figure 5.3 for the C40 series.

Figure 5.3 indicates the improvement in turn-off time that can be realized by using the most effective heatsink that is practical for a particular application. For equipment design it is important that the highest forward current value to be turned off and the highest expected operating junction temperature be considered.



Typical Turn-Off Time Vs. Forward Current (C40 Series) Figure 5.3

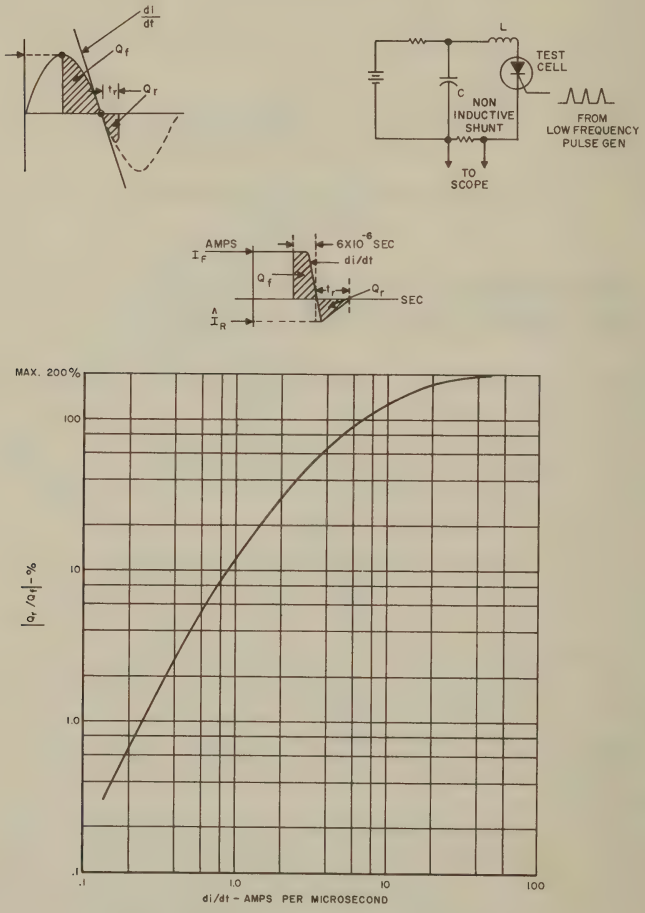
5.3 RECOVERY CURRENT AND REVERSE RECOVERY TIME

Because current carriers in an SCR have a finite lifetime, which may be in the order of a few microseconds, there is always a certain amount of charge stored in transit while the device is conducting forward current. In high frequency AC circuits, where forward current is rapidly commutated to zero at the end of each conducting half cycle, a fraction of this charge remains stored in the vicinity of the SCR end junctions at the instant of zero forward current. Ref. (1) The amount of charge stored (for a given device) is a function of forward current and rate of change of forward current just prior to commutation. Until this charge is swept out, the SCR is unable to block *reverse* voltage, and a reverse (recovery) current will flow which is initially limited only by the commutating circuit impedance and applied voltage. Reverse recovery current and the time for which it flows should not be confused with turn-off time described previously, which is the time necessary for the SCR to block reapplied *forward* voltage. The reverse recovery phenomenon is also common to ordinary junction rectifiers.

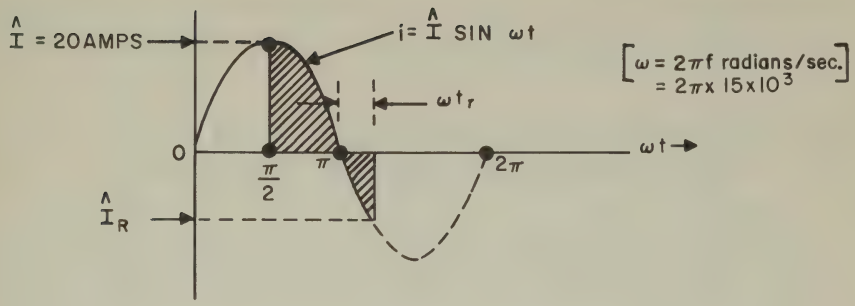
In high frequency sinusoidal circuits ($f > 1$ KC/S) typical reverse recovery time can be calculated by using the curve of Figure 5.4A. This relates the integral of amp-seconds for the latter half of the forward current cycle, (designated Q_f), to the reverse amp-second integral (Q_r) before reverse current flow ceases, as a function of $\frac{di}{dt}$. In square wave circuits the same curve may be used to approximate reverse recovery times by taking Q_r as the amp-second integral for the last 6 microseconds of forward current conduction.

and Q_r as the amp-second integral of a triangular current waveform (Figure 5.4B) with peak value $\hat{I}_R \cong \frac{V_R}{R}$ amps, where V_R equals peak negative commutating voltage and R equals commutating circuit impedance. It should be emphasized that in either case (sinusoidal or square wave), Q_f, as defined, merely provides a convenient reference quantity which is a function of both forward current and di/dt; it is not a true measure of actual charge stored in the SCR at the instant of commutation.

As an example of the use of Figure 5.4A, consider a 2N681 SCR operating in a 15 KC/S sinusoidal circuit with a peak forward current of 20 amps as sketched in Figure 5.5.



Test Circuit and Current Waveform
(a) Controlled Rectifier Reverse Recovery Characteristics (All Medium & Low Current SCR's Except TO-5 Package Types).
Q_r and Q_f in Square Wave Circuits
Figure 5.4



Current Through 2N681 SCR in 15 kc/s Circuit
Figure 5.5

$$i = \hat{I} \sin \omega t$$

at $\omega t = \pi$, di/dt is given by:

$$di/dt = \omega.\hat{I} = (6.28 \times 15 \times 10^3 \times 20) = 1.885 \text{ amps}/\mu\text{second}$$

From Figure 5.4A $\left|\frac{Q_r}{Q_f}\right| = 0.30$ @ di/dt = 1.885 amps/μsecond

From Figure 5.5 $Q_f = \frac{1}{\omega}\int_{\pi/2}^{\pi} \hat{I}.\sin \omega t.\, d\omega t = \frac{\hat{I}}{\omega}$

and $Q_r = \frac{1}{\omega}\int_{\pi}^{(\omega t_r + \pi)} \hat{I} \sin \omega t,\, d\omega t. = -\frac{\hat{I}}{\omega}[1 - \cos \omega t_r]$

Since $\left|\frac{Q_r}{Q_f}\right| = 0.30,\ \frac{\hat{I}}{\omega}[1 - \cos \omega t_r] = 0.30\frac{\hat{I}}{\omega}$

Cancelling common terms, rearranging, and solving for ωt_r:

$$(1 - \cos \omega t_r) = 0.30$$

$$\cos \omega t_r = 0.70$$

or $\quad \omega t_r = 45°34' = .795$ radians

The recovery time t_r is given by:

$$t_r = \frac{\omega t_r}{\omega} = \frac{.795}{6.28 \times 15 \times 10^3} = (8.43 \times 10^{-6}) \text{ sec.}$$

and peak recovery current $\hat{I}_R$ is given by:

$$\hat{I}_R = \hat{I} \sin (\omega t_r + \pi)$$

$$= -20 \sin 45°34'$$

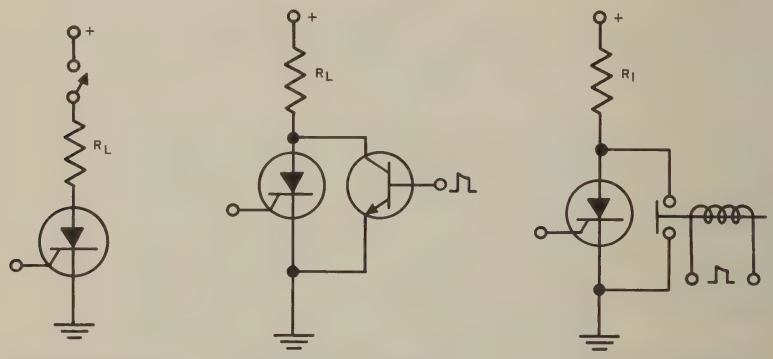
$$= -14.28 \text{ amps}$$

In full wave rectifier circuits employing SCR's as the rectifying elements, this reverse recovery current, which can be appreciable, has to be carried in

the forward direction by the complementary SCR(s). The sudden cessation of reverse current may also produce commutating voltage transients which can be suppressed with suitable R-C filters if excessive.

5.4 CURRENT INTERRUPTION AND A-C CURRENT TURN-OFF CIRCUITS

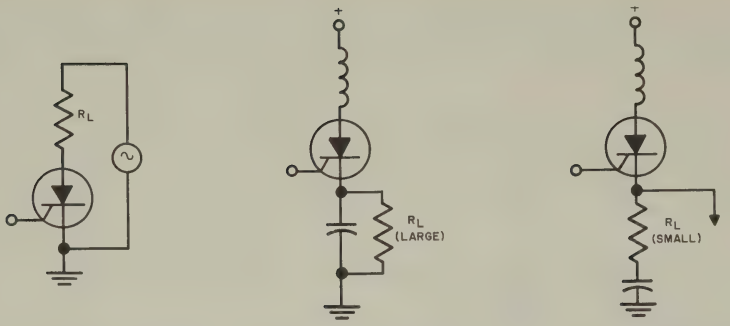
There are numerous circuits that can be used to turn-off an SCR after it has been triggered into its high conduction mode. Interrupting the load current with a switch as shown in Figure 5.6(A) is satisfactory provided the switch is opened for approximately 100 μsec. The circuits of Figures 5.6(B) and 5.6(C) accomplish turn-off by shunting the load current around the SCR. The transistor in Figure 5.6(B) must have a collector to emitter voltage drop (when carrying full load current) less than the forward drop of the SCR otherwise some load current will flow in the SCR and it may not turn-off. The use of an SCR to carry the main current and a relay to turn-off the SCR as in 5.6(C) may be desirable where it is necessary that a circuit remain energized under conditions of shock or vibration that cause a relay to chatter. The turn-off methods of Figure 5.6(B) and Figure 5.6(C) will permit some reverse current flow, depending on how low the shunting voltage and impedance. These methods offer some improvement in turn-off time over Figure 5.6(A).



(A) Reset Switch-Line Interruption **(B) Shunt Transistor** **(C) Shunt Relay**

Turn-Off by Current Interruption
Figure 5.6

If a sinusoidal voltage is applied to an SCR, it can be triggered on during the positive half cycle and will turn-off during the negative half cycle. Current will flow for a few microseconds in the reverse direction as described previously in Section 5.3. The circuits of Figure 5.7 all turn-off by this action. Figure 5.7(A) indicates operation from an a-c source voltage and 5.7(B) and (C) are oscillatory circuits that form the basis of some types of d-c to a-c inverters. In 5.7(B), when the SCR is triggered "on," the current attempts to go into a damped oscillation but the SCR will turn-off when the current reverses. At the time of current reversal, the voltage on the capacitor will be above line voltage so a back bias is applied to the SCR. More detailed information on these circuits will be found in Chapter 9.



(A) AC Source—Phase Commutation

(B) Underdamped R-L-C Circuit—Shunt Load

(C) Underdamped R-L-C Circuit Series Load

A-C Current Turn-Off
Figure 5.7

5.5 CAPACITOR TURN-OFF CIRCUITS

A common method of turning off an SCR that is conducting from a DC supply is to connect a charged capacitor across the SCR so that the cathode is driven positive with respect to the anode. A charged capacitor represents a very low impedance source of negative voltage so that sufficient reverse current can flow and thus permit the SCR to turn off in the minimum amount of time.

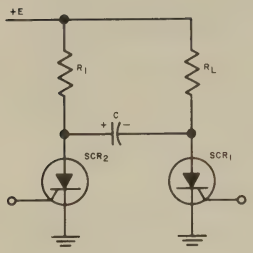
Figure 5.8 shows several methods of charging a capacitor to the proper voltage and then connecting it across the SCR when turn-off is desired.

In Figure 5.8(A) when SCR_1 is turned "on," the capacitor will charge through R_1 to the polarity as shown. Firing SCR_2 will connect the left side of C to ground thus making the anode of SCR_1 instantaneously E volts below ground potential. If the R_LC time constant is long enough, SCR_1 will remain back biased until it recovers its ability to block forward voltage.

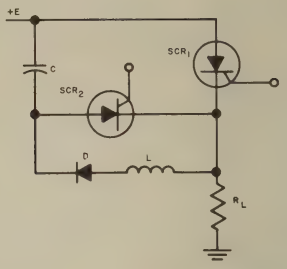
In Figure 5.8(B), SCR_2 should be triggered first to assure that the lower plate of C is near ground potential before SCR_1 is triggered. Then when SCR_1 is turned on, the supply voltage will appear across R_L; the lower plate of capacitor C then charges up to approximately 2E through the resonant charging circuit of L, C, and D. Now when SCR_2 is triggered again, the cathode of SCR_1 will rise to 2E. This turns off SCR_1 due to the reverse voltage of approximately E.

Figure 5.8(C) functions in a manner very similar to 5.8(B) except that it has the desirable property of auto-transformer action in the choke, which tends to charge the lower plate of capacitor C to higher than twice the line voltage when the load current is heavy. This means additional turn-off energy is stored in the capacitor for high load currents where the SCR turn-off time will be longer.

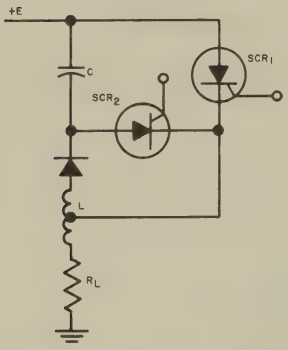
Figure 5.8(D), known as the Morgan circuit, uses a saturable reactor to function both as an auto-transformer and switch. When SCR_1 is turned on, the full line voltage will appear across N_S, which causes the core to saturate and charge the bottom plate of C up to line voltage. The load current flowing



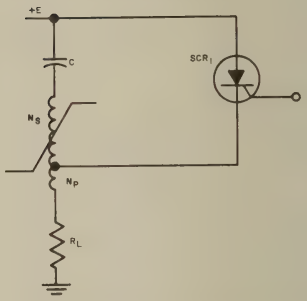
(A) SCR Flip-Flop Circuit



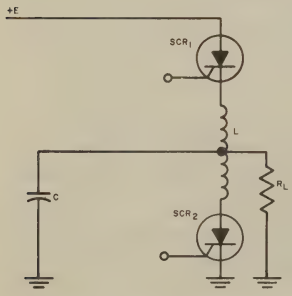
(B) Cathode-Pulse Turn-Off



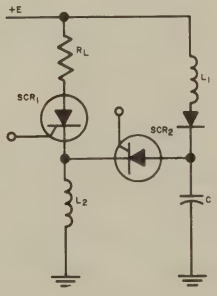
(C) Load Sensitive Cathode Pulse Turn-Off



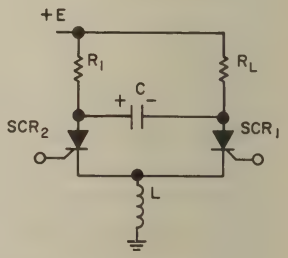
(D) Morgan Circuit



(E) Center-Tapped Choke Turn-Off



(F) Resonant Cathode Pulse Turn-Off



(G) Flip-Flop with Resonant Cathode Pulse Turn-Off

Capacitor Turn-Off Circuits
Figure 5.8

through N_P will reverse the mmf on the core and charges capacitor C above line voltage by auto-transformer action. The load current will cause the core to saturate again (in the opposite direction, however) and the charged capacitor is effectively connected across the SCR.

If the load resistance in Figure 5.8(E) is small enough, the R_L-L-C circuit is underdamped and current will flow continuously through R_L when SCR_1 is fired. Capacitor C will then charge up to line voltage. When SCR_2 is fired, the cathode of SCR_1 will be driven above line voltage by auto-transformer action to effect turn-off.

In Figure 5.8(F) the capacitor is charged to approximately 2E through choke L_1 which has an inductance in the order of 1 mh. Choke L_2 is small (50 μh) so when SCR_1 is fired the current builds up quickly through R_L. When SCR_2 is fired, capacitor C discharges through L_2 and the cathode of SCR_1 is driven more positive than line voltage, thus shutting off SCR_1. SCR_2 turns off when the current in the SCR_2-L_2-C circuit tries to reverse. This circuit must be designed so that C has always been discharged before firing SCR_1.

The circuit of Figure 5.8(G) is similar to that of Figure 5.8(A) except that L assists the capacitor C in turning off the SCR's. A resonant turn-off pulse is developed across the SCR cathode inductance similar to that of Figure 5.8(F). Capacitor C can be eliminated in Figure 5.8(G) if an external pulse generator is coupled to the inductor L to provide the commutating energy.

Complete circuits using some of the above turn-off principles will be found in Chapters 9 and 10. It should be noted that SCR_2 in all these circuits can generally have a lower average current rating than SCR_1, since SCR_2 only conducts for a few microseconds to turn off SCR_1.

5.6 CAPACITORS FOR INVERTER TYPE CIRCUITS

The commutating capacitor has stringent requirements placed upon it to deliver the peak reverse current to the SCR in about 1 μsec. The following should be considered when selecting a capacitor for commutating duty in SCR applications:

1. Capacitance and tolerance.
2. Operating ambient temperature range.
3. Peak voltage and current requirements with repetition rate (wave shapes).
4. RMS current (wave shapes).
5. Provisions for cooling.

The commutating capacitor should have extended foil construction with low impedance at high frequency and a minimum of losses. The high peak value of the charging and discharging currents requires a capacitor with good dielectric efficiency at higher operating frequencies.

The Capacitor Department of the General Electric Company has engineered a family of specially designed units for this type of application. (Ref. 2) A bulletin, "Capacitors for SCR Commutation Applications," GEZ-3279, is

available from Electronic Capacitor Section, General Electric Company, Hudson Falls, N. Y. Several of the inverter and chopper circuits in Chapter 9 specify capacitors of this type.

REFERENCES

1. "Turn-Off Time Characterization and Measurement of Silicon Controlled Rectifiers," R. F. Dyer and G. K. Houghton, AIEE CP 61-301.
2. "Capacitor Selection for Controlled Rectifier Circuits," R. L. Watts and J. D. Harnden, Jr., 1960 AIEE Summer General Meeting, CP 60-926.

CHAPTER 6

SERIES AND PARALLEL OPERATION OF SCR'S

6.1 SERIES OPERATION

The SCR can be used in circuits where total forward (or reverse) voltage is higher than the capability of a single cell by connecting additional SCR's in series. When SCR's are used in this manner, however, some form of forced voltage sharing becomes mandatory. Because the slope of an SCR's E-I characteristic below forward breakover is such that small changes in cell leakage current result in large changes in forward voltage, a cell with low inherent leakage (as measured at rated voltage) will tend to support a much larger share of total voltage than one with high inherent leakage, when both are forced to carry the same leakage current in a series string. If peak voltage impressed across the string is high enough, one cell may even break over, allowing the remainder to follow suit. One way of avoiding this possibility is to shunt each SCR with a voltage-equalizing resistor R. For non-selected SCR's of the same type, the maximum value of R can be determined from the following equation:

$$R = \frac{n V_{BO} - V_{PK}}{(n - 1) \cdot I_M}$$

where V_{BO} = minimum forward breakover voltage per cell (volts)

V_{PK} = maximum peak forward voltage impressed across the string (volts)

n = number of SCR's in series

I_M = maximum forward leakage current per cell (amps)

Both V_{BO} and I_M can be established directly from the appropriate SCR specification sheet. Thus for a 2N685 (C35B) SCR:

$$V_{BO} = 200 \text{ volts}; \quad I_M = 12 \text{ mA}$$

While the above technique will ensure satisfactory voltage sharing under steady state blocking conditions, further precautions must be taken to protect the SCR's against transient effects. When a series string is subjected to high frequency voltage transients, or is called upon to block voltages with steep wavefronts, voltage division is inversely proportional to cell junction-capacitance. Individual differences in junction capacitance can be effectively swamped out by paralleling each series equalizing resistor with a small capacitor. If selected correctly, these parallel capacitors also prevent excessive voltage from appearing across slow cells during "turn-on," and as a corollary, assure even distribution of reverse recovery transients during commutation (Section 12.3).

In applications where reverse-recovery effects are non-critical, .01 to .05 μf

across each element should be sufficient. Otherwise the maximum size of capacitor required can be determined from the following equation:

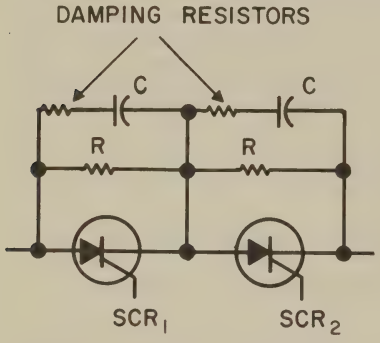
$$C = \frac{10.\ I_F}{V}$$

where: C = Maximum capacitance to distribute reverse recovery transient within cell PRV rating (μf)

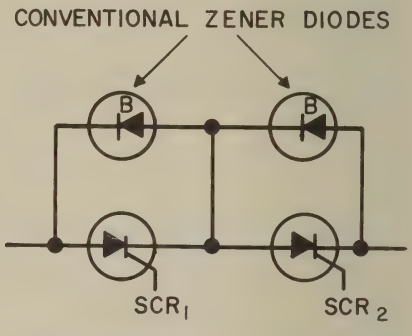
I_F = Current flowing through cell immediately preceding commutation (amps)

V = maximum repetitive cell PRV rating (volts)

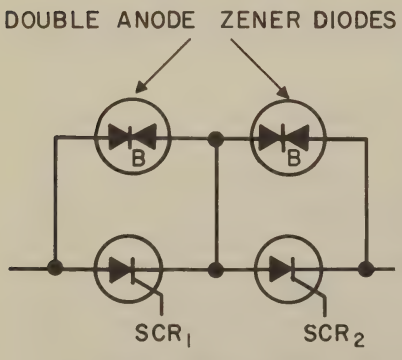
The value of C derived from the above expression is conservative and can often be reduced by experimental optimization. Since these capacitors discharge through the SCR's during turn-on, it is recommended that resultant switching currents be limited within the SCR rating by adding a small resistor



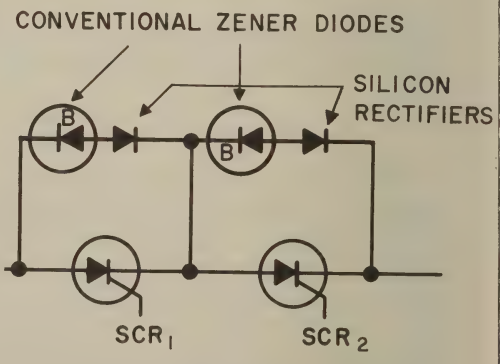
(a) Voltage Sharing Under Both Forward and Reverse Blocking. Increased Leakage.



(b) Voltage Sharing Under Forward Blocking. No Reverse Blocking Capability. Low Leakage.



(c) Voltage Sharing Under Both Forward and Reverse Blocking. Low Leakage.



(d) Voltage Sharing Under Forward Blocking; Reverse Blocking but No Provision for Sharing. Low Leakage.

Series Equalizing Arrangements
Figure 6.1

in series with each capacitor whenever C exceeds 0.1 μf. Series resistors also prevent high frequency oscillations developing due to interaction between lumped or distributed circuit inductance and the parallel capacitance. Generally speaking, 5-50 Ω will be sufficient.

In applications where increase in total forward leakage current due to equalizing resistors must be avoided at all cost, as in SCR radar modulators, voltage sharing may be successfully accomplished by replacing each series equalizing resistor with a silicon zener diode. When zener voltage is chosen correctly, total leakage current through the series string need be only slightly higher than the maximum leakage current of the poorest SCR. Zener voltage should be equal to, or slightly below, specified SCR forward breakover voltage, when measured at the zener's rated maximum temperature and with a zener current of twice maximum SCR leakage current. Where a series string has to block appreciable reverse as well as forward voltage, double-ended zener diodes may be substituted for the conventional single anode type. In cases where reverse blocking requirements are not so severe, some reverse blocking ability can be obtained using conventional zeners and silicon rectifiers arranged as in Figure 6.1 (d).

6.2 GATE ISOLATION OF SERIES SCR'S

Series operation also requires that the gate signal for each series connected cell be electrically isolated from all others. For AC and pulse type firing signals, this can be accomplished by means of small transformers with multiple secondaries. Multiple gate windings in saturable reactor firing circuits are particularly adapted for this purpose. Particular attention should be given to the insulation between the various windings. It usually must be capable of withstanding the peak line voltages in the circuit. A small resistor or capacitor should be added in series with each gate to prevent a cell with low impedance gate characteristic shunting the triggering signal away from cells with higher gate impedance. This requirement is discussed fully in Section 6.6 under "Gate Requirements for Parallel SCR's."

6.3 SLAVE FIRING OF SERIES SCR'S

Figure 6.2 illustrates an alternative method for accomplishing gate isolation without the use of an isolating transformer. Two voltage equalizing resistors, R_2 and R_3, are connected across the respective cells. Only SCR_1 is directly triggered by the signal source, in this case a unijunction transistor UJT. The gate of SCR_2 is triggered by the surge of current charging capacitor C_1 when the voltage across SCR_1 abruptly decreases from a high value to a low value as it switches into conduction. When used in an AC circuit, the size of capacitor C_1 must be selected so that it discriminates between the normal cyclical variations in line voltage and the turn-on transient. The former must not fire the SCR under any conditions. The latter must turn SCR_2 on. Optimum value of C_1 in sinusoidal voltage circuits can be determined as follows:

$$\frac{1}{8\pi f R_1 V_{max}} \gtrsim C_1 \gtrsim \frac{I_{GF}}{10^7}$$

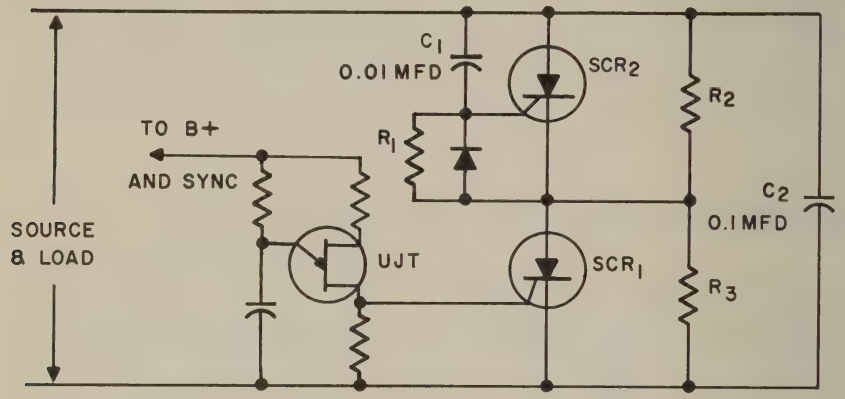
where f = frequency of supply, cps

V_{max} = peak anode voltage applied to each SCR, volts

C_1 = triggering capacitor in farads

I_{GF} = maximum gate current required to fire SCR_2 (amperes)

C_2 is connected across both SCR's to provide a stiff source of voltage for the few microseconds required to fire the second SCR_2, and to reduce the effect of line transients on the triggering circuit.



Series Operation of SCR's (2N681 Series)
Using Slave Gating
Figure 6.2

6.4 USE OF PARALLEL MATCHED SCR'S

SCR's with factory matched forward conduction characteristics will share load current if connected directly in parallel. Matched cells of this type are available from General Electric Company on special order. In order to assure satisfactory current sharing at both normal load and under fault conditions, the forward voltage drops of these special selections are matched at two levels of current. For example, the forward voltage drops of matched 2N681 series medium current SCR's are selected to be within .015 volt of each other at 500 mA and within .04 volt of each other at 50 amps, while comparable figures for the 2N1909 (C50) high current line are .05 volts at both 10 and 500 amps. Based on these figures, the maximum allowable total load current I_{total} through a parallel group of n cells can be expressed as follows:

2N681 series: $I_{total} = (0.8\ n + 0.2)\ I_{cell}$

2N1909 series: $I_{total} = (0.6\ n + 0.4)\ I_{cell}$

where I_{cell} is the rated current for a cell operating alone. Thus, two matched

2N1909 cells, each capable of handling 70 amperes continuously when operated alone, will carry up to

$$(0.6 \times 2 + 0.4) \times 70 = 112 \text{ amperes total}$$

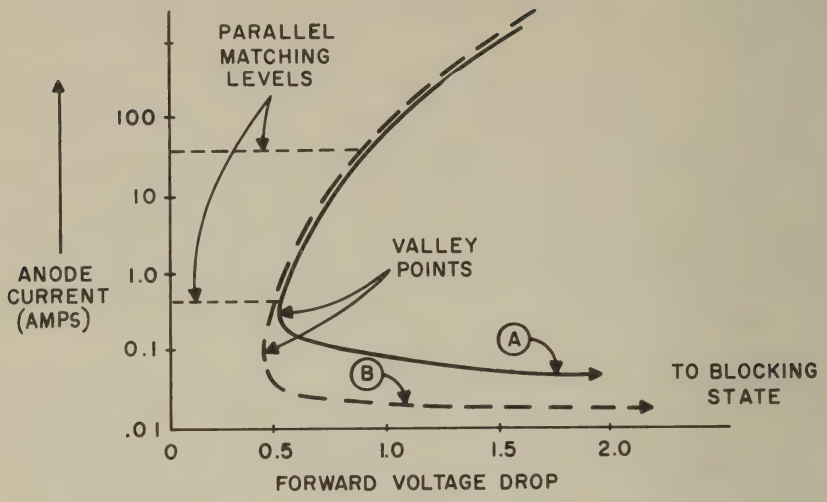
when operated in parallel with each other.

At normal load current levels the forward voltage drop of an SCR decreases as junction temperature increases. This phenomenon would tend to cause the hotter of two parallel cells to carry more than its share of the total, thereby causing it to heat up still more and ultimately draw enough current to cause serious damage to the cell. To avoid this possibility, it is recommended that cells operated in parallel be mounted on a common heatsink so that variations in cooling conditions will affect all paralleled cells equally.

When parallel matched SCR characteristics are relied on for current sharing, particular care must be taken to assure that resistance in series with each individual parallel path is maintained as nearly equal as possible. Wiring and connections should be uniform in all respects. The tendency for current to crowd to the outer branches or paths of a parallel network due to reactive effects is of particular significance at higher frequencies, and during the switching interval at the beginning and end of each conduction period. Inductance in series with each parallel path should be equalized where this phenomenon poses a problem. Conceivably this may also be of concern on phase controlled 60 cps circuits when three or more SCR's are connected in parallel without some external means of forced current sharing, although no difficulties have been observed up to this writing.

At low values of anode current the forward voltage-current characteristic changes from a positive to a negative resistance as it is reduced towards the minimum holding current. Below this value, the SCR will turn off by reverting to the forward blocking state. This transition point between positive and negative resistance is represented by the valley indicated in Figure 6.3, i.e., the current at which minimum forward voltage drop occurs. It is very difficult to match SCR's satisfactorily for identical characteristics in this region, particularly over wide ranges of temperature. This poses no problem when the gate signal is supplied to the parallel SCR's throughout the anode conduction period, since any instability in current-sharing or a tendency of one SCR to turn off will not overheat the other device(s) in parallel because of the low current level in the region of the valley. As long as gate current is maintained, an SCR with a tendency to turn off at low anode current levels will switch into conduction again as soon as the total load current moves out of this valley area. It will thus assume its share of the load before overloading on its partner can occur.

When a pulse type of gate signal is employed for firing paralleled SCR's, instability may be encountered at low anode current levels which may have serious consequences if high levels of current follow. Pulsed gate signals are typical of unijunction transistor firing circuits and some types of saturable reactor firing schemes. Unless the total load current has reached a sufficiently high level to keep all of the parallel cells above the valley point by the time the gate pulse is removed, a cell such as A in Figure 6.3 will turn off. In the absence



Anode Voltage-Current Relationship of SCR's with Matched Forward Characteristics
Figure 6.3

of any further gate signal, it will remain in the non-conducting state through the remainder of that cycle, thus failing to carry its share of the load.

This phenomenon is likely to occur when operating at very short firing angle delays in phase controlled AC circuits and when firing from reactive lines or into inductive loads where the buildup of load current to normal levels is restrained by the inductive effect.

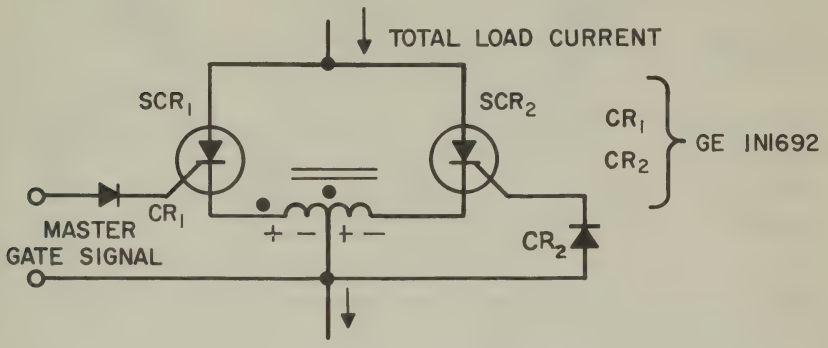
For a pair of factory matched SCR's, the total anode current required to ensure continuity of conduction after the gate signal is removed as follows:

Junction Temperature	Minimum Instantaneous Anode Current for Positive Hold-In (Total for Two Parallel Cells)	
	2N681 (C35)	2N1909 (C50)
+125°C	0.9 Amps	——
+ 25°C	1.5 Amps	1.5 Amps
— 65°C	6.5 Amps	4.0 Amps

When more than two cells are paralleled, total anode current should be increased proportionately. For example, when three matched 2N681 SCR's are operating at 125°C junction temperature, the total anode current should reach $(0.9 \times 3/2) = 1.35$ amps before the gate signal is removed.

This situation may be alleviated to a great extent by introducing a paral-

leling reactor, which is effective in forcing current sharing until total anode current reaches a value high enough to maintain all cells in conduction. Once the cells are in full conduction, the reactor may saturate and become ineffective for the remainder of that particular cycle. A paralleling reactor circuit of this type is shown in Figure 6.4. (Ref. 1)



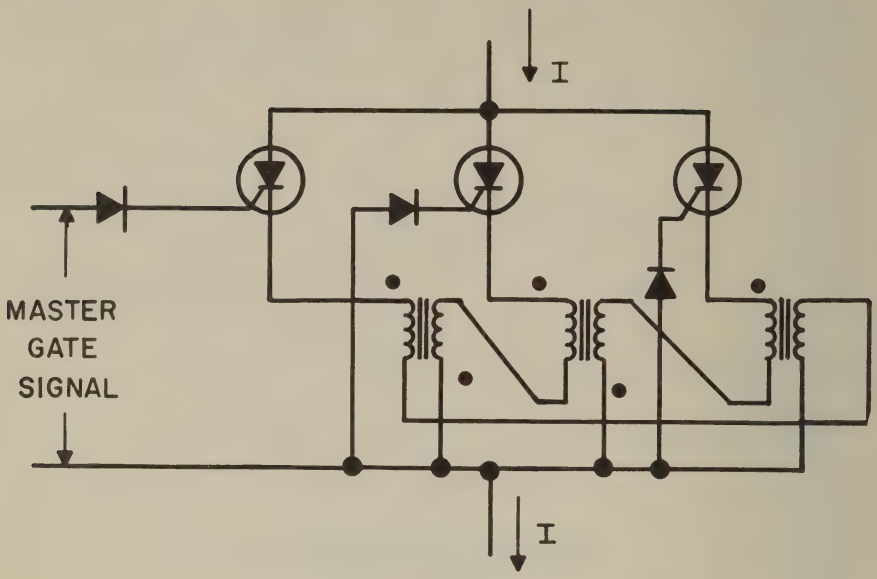
Use of Paralleling Reactor
Figure 6.4

When SCR_1 is fired (from a pulse source), voltage is developed across the reactor as shown. This voltage provides both gate voltage and additional anode voltage to help turn on SCR_2. In practice, as SCR_1 starts to turn on, SCR_2 will follow with but a slight time lag, so that the gate voltage on SCR_2 can never rise excessively. The advantage of this circuit is that if either SCR starts to turn off early in the cycle, as the gate signal is removed, the paralleling reactor develops both gate and anode voltage to keep it turned on.

The most important magnetic requirements for such a reactor are high saturation flux density and low residual flux density in order to provide as great a change in total flux ($\Delta\phi$) per cycle as possible. Powdered molybdenum-permalloy cores such as the Arnold type A438281 have been found suitable. CR_1 and CR_2 prevent flow of negative gate current in the SCR gate-cathode circuits.

Figure 6.5 illustrates how three of these cores can be used in paralleling three SCR's. Using a three core closed loop arrangement, any one of the three parallel paths could be opened and the two remaining cells would operate satisfactorily, sharing the total load equally between themselves. This approach may have significance in high reliability circuits where continuity of operation is essential, even after removal of a faulty cell from the circuit by a fuse or circuit breaker.

Because there is a small but finite delay between one SCR firing and the next in these slave-gated parallel arrays, slave gating should not be used in applications where high switching currents are generated, as when paralleled SCR's operate into capacitive or very large resistive loads. In such cases each SCR must be fired independently and simultaneously to prevent any one cell from instantaneously carrying the full switching current.



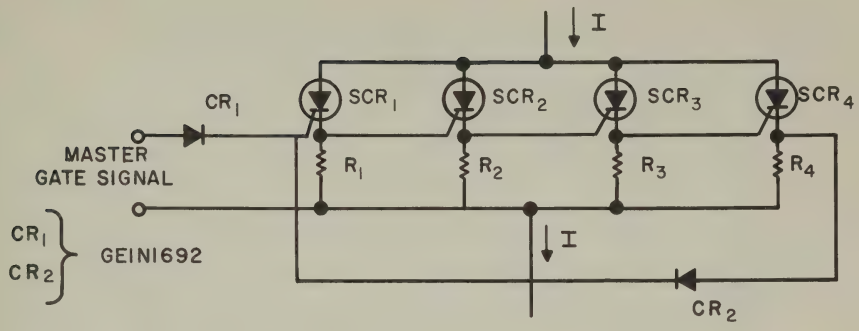
Paralleling Reactor Connections for Three Parallel SCR's
Figure 6.5

6.5 USE OF UNMATCHED SCR'S

When paralleling unmatched SCR's for higher current handling capacity, some external means of forced current sharing is essential. In this case, the components chosen must force current sharing over the whole cell conduction period. Resistors are quite effective but necessarily inefficient, particularly where large amounts of power are involved. In applications where the SCR's are not required to *switch* heavy currents, paralleling resistors may be inserted in the SCR cathode leads as shown in Figure 6.6. In this way, only one master SCR need be fired, the gate signal for SCR_2 being provided by current through R_1 as SCR_1 turns on, etc. With the closed loop provided by diode CR_2, the total load current could drop as low as the holding current of a single SCR, yet pick up the remaining parallel SCR's when the load current rises again. This action would take place even though the SCR with the lowest holding current was not in position SCR_1.

At higher power levels, paralleling reactors and circuits similar to those used for firing purposes are usually the most effective and efficient solution. (Ref. 2) The action of this type of reactor was discussed earlier under operation of matched SCR's. For unmatched SCR's, however, the core must be capable of providing a current-balancing voltage throughout the entire conduction period without saturating. The core may rely on an airgap to return the flux density to a low level at the end of the cycle or on a reset winding to actually reverse the flux before the next cycle starts.

In a single phase circuit, the paralleling core should be capable of sup-



Use of Resistors For Parallel Matching
Figure 6.6

porting $\frac{\Delta V}{2f}$ volt-sec without saturating where f = supply frequency in c.p.s. and ΔV = voltage mismatch at peak load current. For SCR's with maximum mismatch, which is the worst case that might be encountered from selecting SCR's of the same type at random, ΔV may conservatively be selected as one volt (2N681 or 2N1909).

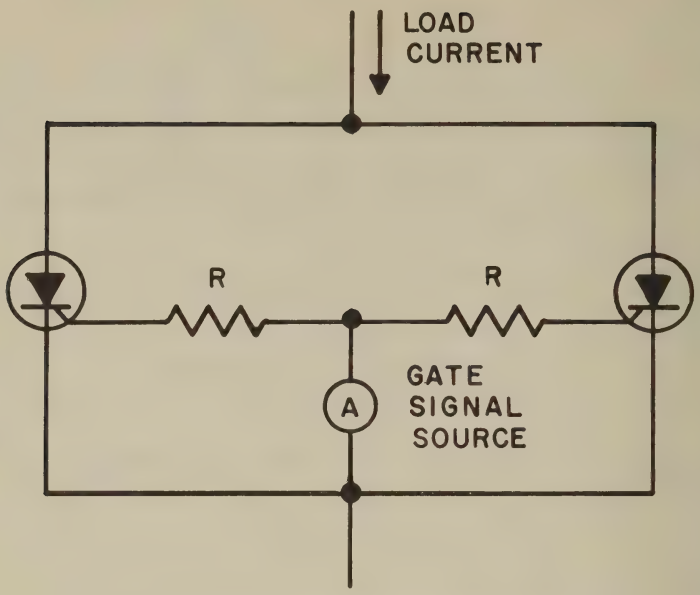
For two unmatched 2N681 (C35) SCR's operating in a 60 cps circuit, a Silectron AA-81 cut "C" core (Arnold Engineering) with two windings, each with 50 turns of #16 AWG enamelled wire, will ensure current sharing within a few per cent. An air gap of approximately 5 mils should be introduced at each face to reduce the residual flux to a low value. Use an AA48 core and 50 turns of #10 AWG wire for unmatched 2N1909's (C50's).

Additional cells may be paralleled in a similar manner to that shown in Figure 6.5.

6.6 GATE CONNECTIONS FOR PARALLEL SCR'S

If parallel SCR's are fired from a common source, which is an essential requirement when very large resistive or capacitive loads are involved, each cell must be supplied with sufficient drive to exceed its own specific firing needs. As pointed out in Chapter 4, firing requirements may differ quite widely between individual SCR's *whether parallel matched or not.* To prevent a cell with a low impedance gate characteristic from shunting the signal away from a cell with a high impedance gate characteristic, resistors should be inserted in each gate lead, as shown in Figure 6.7. The value of these resistors should be selected to provide a gate load line that falls above the maximum current and voltage firing requirements for any cells of that type. If a relatively stiff gate voltage of 6 volts or more is available at A in Figure 6.7, 30 ohms in each gate lead will be satisfactory for the 2N681, or 10 ohms for the 2N1909.

Where the total energy available to fire a parallel array is limited, as in some pulse firing arrangements, it is preferable to replace these resistors with a 0.1 μf capacitor in series with each gate lead. Series capacitors tend to equalize



Resistor R Permits Firing Both SCR's From A Common Gate Signal Source
Figure 6.7

the *charge* coupled to each SCR gate during trigger pulses, thus reducing the effects of unequal loading without additional power wastage. When capacitors are used in this manner a 220 Ω — 1 K resistor should be connected from gate to cathode of each SCR (see Section 4.13.5).

6.7 SUMMARY ON PARALLEL OPERATION

SCR's may be paralleled with the following precautions:

(A) Factory Matched Cells.

1. Derate load current through each cell.
2. Mount all parallel cells on a common heatsink.
3. Keep gate signal applied until anode current through each cell has exceeded its valley point.
4. Slave firing arrangements using paralleling reactors may be used to make this less critical when SCR's operate into inductive loads.

(B) Unmatched Cells.

1. Same external forced current sharing is essential.
2. Balancing resistors may be useful for this purpose in some applications. Balancing resistors should not be employed as *slave-gating* elements, however, when high switching currents are involved.
3. Balancing reactors are generally a more acceptable solution in high current applications. Same comments on slave gating as in (B)2 above.

(C) Gate Connections.

1. When paralleled cells operate into capacitive or very high resistive loads where high switching currents are a problem, each gate must be driven individually and independently on its own load line.
2. These requirements may be satisfied by using a common firing source with series resistors or capacitors in each gate lead.

REFERENCES

1. "Excitation Requirements for Controlled Semiconductor Rectifiers," E. E. Moyer and A. Schmidt, Jr., AIEE CP 60-439.
2. "Current Balancing Reactors for Semiconductor Rectifiers," I. K. Dortort, AIEE TP 59-219.

CHAPTER 7

STATIC SWITCHING CIRCUITS

7.1 GENERAL

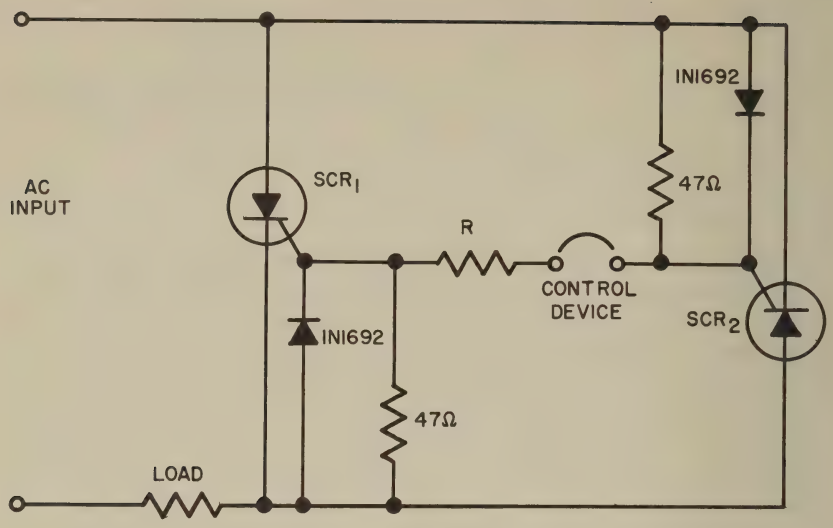
Since the SCR is a bistable device, one of its broad areas of application is in the realm of signal and power switching. This chapter describes circuits in which the SCR is used to perform simple switching functions of a type that might also be performed non-statically by various mechanical and electromechanical switches. In these applications the SCR is used to open or close a circuit completely, as opposed to applications in which the SCR is used to control the magnitude of average voltage or energy being delivered to a load. These latter types of applications are covered in detail in the three succeeding chapters.

The first five circuits have one main characteristic in common: current through the SCR's is turned off or commutated by the reversal of the AC line voltage. Since the turn-off time of standard SCR's may be as high as 25 microseconds if the SCR has not been specifically tested for this characteristic, line-commutated circuits have an inherent upper operating limit of approximately 20 KC unless the SCR is of the fast turn-off type. Above this frequency, standard SCR's may not turn off between cycles.

The remaining circuits described in this chapter operate from a DC supply voltage. Turn-off of the SCR in this type of circuit must be accomplished by one of the means described in Chapter 5 other than use of an AC supply. Typical means are use of a series interrupting switch or a parallel capacitor. The turn-off time characteristic of the SCR is usually critical when optimizing DC circuits which use capacitor or pulse types of turn-off. Inverter-type SCR's such as the C40 and C55 which have tested turn-off time specifications should therefore be used in these DC applications. For a more detailed discussion of SCR turn-off methods see Chapter 5.

7.2 AC STATIC SWITCH

The circuit in Figure 7.1 provides high-speed switching of AC power loads and is ideal for applications with a high duty cycle. It eliminates contact sticking, bounce, and wear as experienced on relays or contactors. The control device indicated can be initiated by light, heat, voltage, current, pressure, speed, frequency, coincidence, or phasing, etc. Signals from magnetic cores, transistors, or electronic tubes can be used to control sizeable blocks of power in this type of circuit. Resistor R is provided to limit gate current peaks. Its resistance should be greater than the peak supply voltage divided by two amperes. This AC switch can be used for such applications as welder controls, furnace heat controls, X-ray supplies, illumination controls, or limit switches. As a substitute for control relays, the SCR overcomes the differential problem, that is, the



AC Static Switch
Figure 7.1

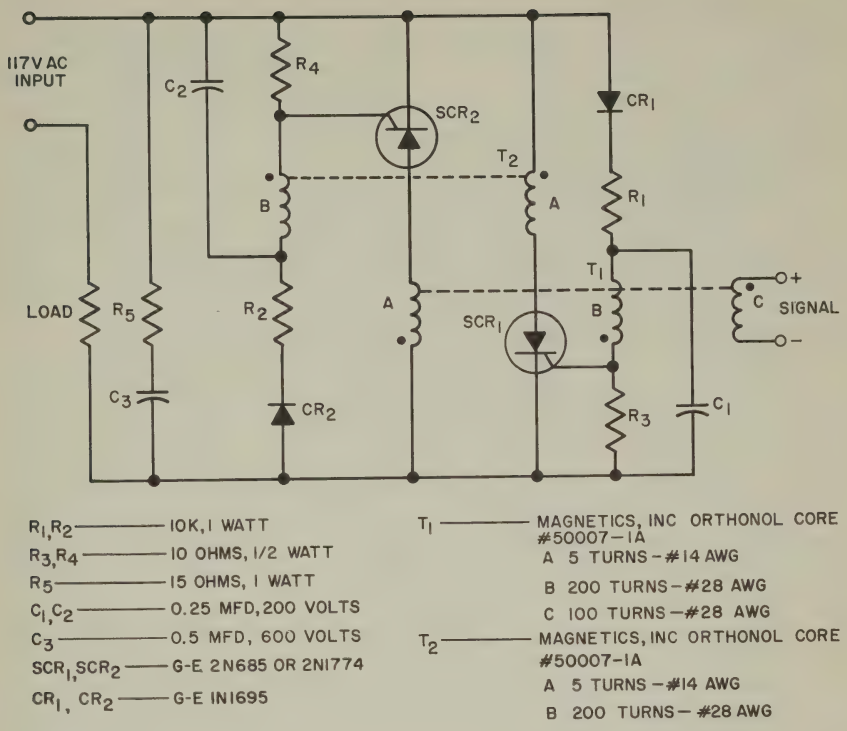
spread in current or voltage between pickup and dropout because it effectively drops out every half cycle. Provided resistor R is properly selected, this circuit is operable over a much wider voltage range than a conventional relay or contactor.

The use of hermetically sealed reed switches as control devices in combination with SCR's provides reasonable cost and extremely long life. The reed switch may be actuated by passing current through a winding around it or by a small magnet. In either case, electrical isolation exists between the controlling signal and the main power circuit. Acting as a sensitive current relay, the SCR reed-switch combination can interrupt fault currents in as little as one cycle. With permanent magnet actuation of the reed switch, the combination becomes a power limit switch.

Full wave AC switching can be accomplished with a single SCR by connecting the SCR across the DC terminals of a bridge rectifier whose AC terminals are connected in series with the load. Other variations of Figure 7.1 can be used in connection with conventional DC rectifier power supplies to provide both switching and rectification with the same device.

7.3 AC STATIC CONTACTOR AND LATCHING RELAY

By combining the characteristics of square-loop core materials with the SCR, many useful circuits can be developed. Figure 7.2 uses two small toroidal cores in conjunction with two back-to-back SCR's in a variation of Figure 7.1 to secure a direct analogy to a single pole electromechanical contactor with an electrically isolated solenoid or, with slight modification, an analogy to an electromechanical latching relay.



AC Static Latching Relay with Isolated Input
Figure 7.2

When SCR_1 and SCR_2 are furnished with a gate signal, they will conduct and supply full wave AC to the load, thus simulating the closed contacts of a relay or contactor. If no gate signal is supplied to the SCR's, the switch will be "open."

During the "open" state, both core T_1 and T_2 are saturated by the flow of current from the main AC supply through their respective B windings during alternate halves of the cycle. This current is limited by resistors R_1 and R_2 respectively. Under these conditions, the gate voltage applied to the SCR's is limited to less than 0.25 volt by the voltage-dividing action of R_1 and R_3 across SCR_1 and R_2 and R_4 across SCR_2. Neither SCR fires, and no current flows in any of the reset windings of the cores.

If a low level voltage is now applied to the "Signal" C winding of T_1, this core will reset during the half cycle that the anode of SCR_1 is negative and CR_1 is blocking. When the anode of SCR_1 starts to swing positive on the following half cycle, winding B on T_1 will sustain part of the supply voltage and capacitor C_1 will charge through CR_1 and R_1. After about 1 or 2 milliseconds, depending on its design, core T_1 will saturate, discharging C_1 through the gate of SCR_1 and firing it. Current will flow from the line through SCR_1 to the load.

The gate firing circuit on SCR_2 is identical to that on SCR_1 except no separate "Signal" winding is used. Core T_2 depends on current through its winding A to reset the core and thus permit firing of SCR_2. Thus, if SCR_1 is fired by the foregoing sequence, anode current in SCR_1 will reset T_2 and SCR_2 will fire on the following half cycle. Full wave voltage will be delivered to the load.

With winding A on T_1 connected in the anode circuit of SCR_2, T_1 will in turn be reset by the anode current through SCR_2. Thus, once conduction has been initiated in SCR_1 by a positive pulse on the "Signal" winding of T_1, the switch will remain "closed" even though no further signal is applied to the input. The switch may be turned off by a negative pulse on the "Signal" winding of T_1. This prevents winding A from resetting T_1, and SCR_1 is in turn not fired on the following half cycle. This interruption of load current stops the reset action on T_2 as well, and the circuit reverts to the "open" state.

In this mode of operation, the circuit behaves like a latching relay. Once it has been turned on, it remains in the conducting state even though the main line voltage is interrupted for long periods of time. In other words, as a latching relay this circuit "remembers" whether it was open or closed even through power interruptions. Positive reset action requires that a minimum load current flow whenever the circuit is closed. For the design in Figure 7.2, this minimum current is approximately one ampere. A lower load current can be sustained by use of a bleeder across the load or by increasing the number of turns in the A windings.

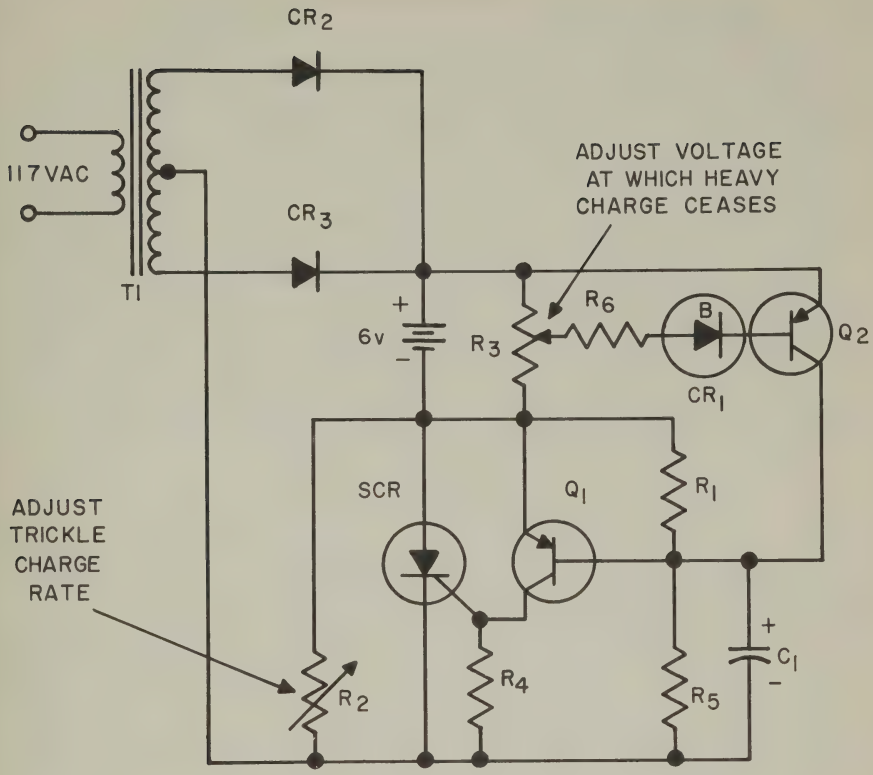
A direct analogy to a conventional single pole contactor can be derived by eliminating the A winding on T_1. With this change, load current will not reset T_1, and a continuous positive DC signal on winding C of T_1 will be necessary to keep the contactor closed. The contactor will open within one cycle after this DC signal has been removed. Sensitivity of the switch to a control signal can be improved by increasing the number of turns on the C winding.

C_3 and R_5 serve as a filter to prevent line voltage transients from triggering the switch. They also assist in completing reset action of the cores in the latching mode if the line voltage is interrupted at a critical part of the cycle. The impedance of the switch in the "open" state is fixed by the impedance of R_5 and C_3 at the line frequency.

7.4 BATTERY CHARGING REGULATOR

Figure 7.3 illustrates a relatively inexpensive means of utilizing the SCR as a battery charger regulator, thus eliminating the problems inherent in elec- and dropout, wear, etc. As shown, this circuit is capable of charging at up to a 16 ampere rate. When the battery voltage reaches the level of full-charge as set by R_3, the SCR cuts off and a trickle charge determined by the value of R_2 continues to flow.

CR_2 and CR_3 deliver full wave rectified DC to the SCR in series with the battery. Transistor Q_2 compares a portion of the battery EMF with a reference diode CR_1. If the battery voltage is low, Q_2 will be cut off and a positive voltage will be developed across resistor R_1 and between emitter and base of transistor Q_1 whenever the SCR anode is positive. Q_1 will conduct heavily into the gate of



R_1, R_5	300Ω, 2 WATT	C_1	100 MFD, 25 VOLT ELECTROLYTIC
R_2	50Ω, 1 AMP RHEOSTAT	SCR	G-E 2N683
R_3	200Ω, LINEAR POT	CR_1	IN468
R_4	47Ω, 1/2 WATT	CR_2, CR_3	G-E IN2154 OR IN1200A
R_6	15Ω, 1/2 WATT	Q_1, Q_2	G-E 2N525
T_1	117 VOLT PRI, 8/0/8 VOLT SEC.		

Battery Charging Regulator
Figure 7.3

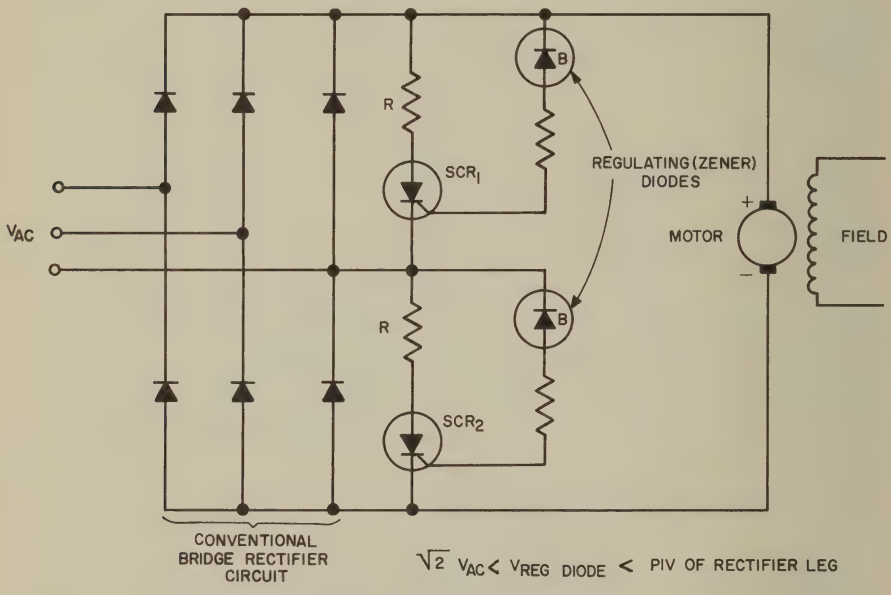
the SCR, firing it and thus charging the battery. When the battery voltage rises to the point where Q_2 starts to conduct, the voltage across R_1 will reverse, cutting off Q_1, and thus removing the gate signal from the SCR. In this mode, only resistor R_2 will control the charging rate.

This circuit switches from trickle charge to the full charging rate with less than a three percent drop in battery voltage.

For charging a 12 volt battery, a 300 ohm 1 watt resistor should be inserted in the collector of Q_2, R_3 should be increased to 400 ohms, and the secondary voltage of T_1 should be doubled.

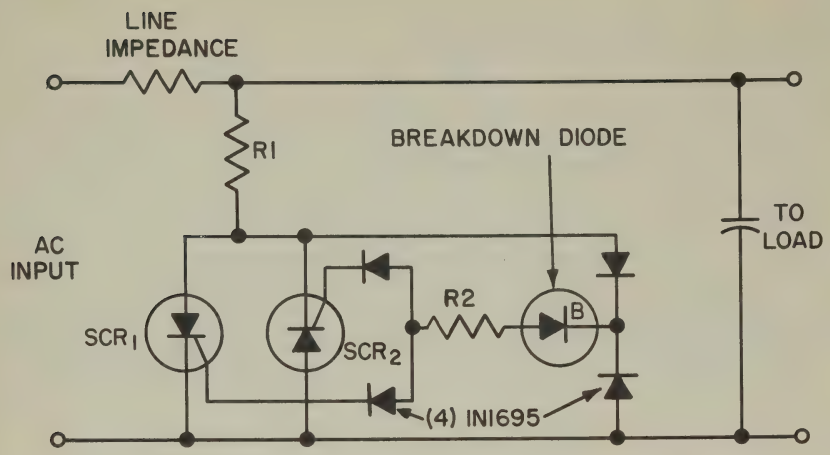
7.5 OVERVOLTAGE PROTECTION ON AC CIRCUITS

The SCR makes possible some interesting protective circuits that capitalize on the fast switching speed and high current-carrying ability of these semiconductors. Figure 7.4 illustrates a method by which SCR's may be used as a substitute for a dynamic braking contactor to protect a rectifier equipment feeding a regenerative load as typified by a DC shunt motor. An SCR in series with a current limiting resistor R is connected across each of two of the rectifier legs adjacent to one of the AC lines. Under normal operation, neither SCR_1 nor SCR_2 conducts and no energy is lost in the resistors. However, when the DC bus voltage rises to a point determined by the avalanche voltage of the regulating diodes, SCR_1 and SCR_2 are fired, connecting the resistors across the bus thus preventing the DC voltage from damaging the rectifier equipment. As soon as the DC bus voltage drops below the AC supply, SCR_1 and SCR_2 are commutated by the AC line and return to their non-conducting state.



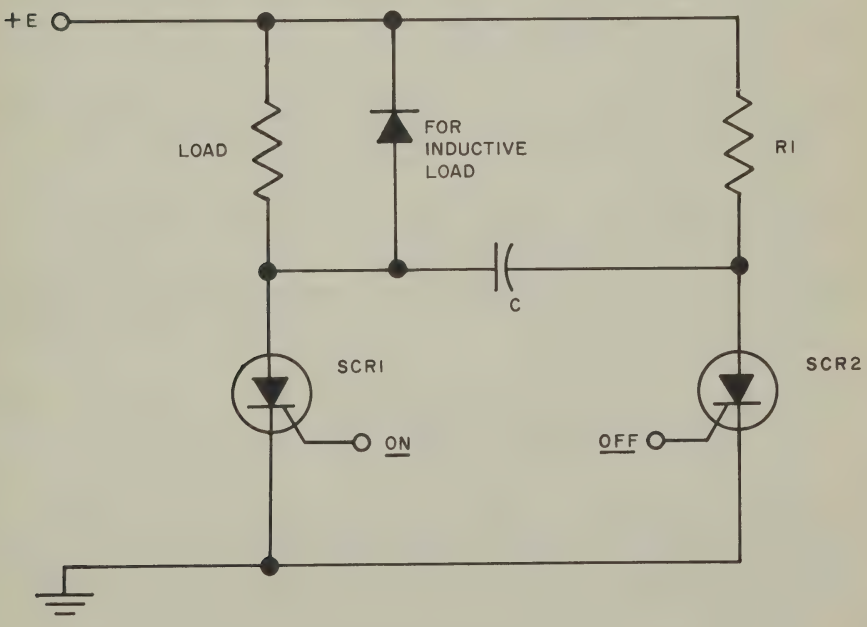
Regenerative Voltage Protection
Figure 7.4

Since SCR's switch into their highly conductive state in a matter of microseconds, they can be used for suppressing transient voltages with a much higher rate of rise than could be handled by electromechanical devices such as relays. Figure 7.5 illustrates a circuit that may be employed for general transient protective service on AC lines. When the line exceeds the avalanche voltage of the breakdown diode, either SCR_1 or SCR_2 fires, depending on the polarity of the AC line at that instant. Resistor R_1 limits the current to the short term surge



Transient Voltage Protection Using Silicon Controlled Rectifiers
Figure 7.5

capabilities of the SCR's. For the C35, R_1 must limit the one cycle peak current to less than 150 amperes. This loading effect on the circuit drops the transient voltage across line impedance. Alternation of the AC line voltage turns off the current through the conducting SCR at the end of the cycle.



DC Static Switch
Figure 7.6

7.6 DC STATIC SWITCH

Figure 7.6 illustrates a static SCR switch for use in a DC circuit. When a low power signal is applied to the gate of SCR_1, this SCR is fired and voltage is applied to the load. The right hand plate of C charges positive with respect to the left hand plate through R_1. When SCR_2 is triggered on, capacitor C is connected across SCR_1, so that this SCR is momentarily reverse biased between anode and cathode. This reverse voltage turns SCR_1 off and interrupts the load current, provided the gate signal is not applied simultaneously to both gates.

SCR_1 should be selected so that the maximum load current is within its rating. Since SCR_2 need conduct only momentarily during the turn-off action, it can be one size smaller in rating than SCR_1. The minimum value of commutating capacitance C can be determined by the following equations:

$$\text{For Resistive Load: } C \geqq \frac{1.4\ t_o\ I}{E}\ \mu\text{fd} \qquad 7.1)$$

$$\text{For Inductive Load: } C \geqq \frac{t_o\ I}{E}\ \mu\text{fd} \qquad (7.2)$$

Where t_o = Turn-off time of SCR in μ seconds (See specification for inverter-type SCR)

I = Maximum load current (including possible overloads) in amperes at time of commutation

E = Minimum DC supply voltage

The resistance of R_1 should be ten to one hundred times less than the minimum effective value of the forward blocking resistance of SCR_2. This latter value can be derived from the published leakage current curves for the SCR under consideration.

In some cases a mechanical switch may be substituted for SCR_2 to turn-off SCR_1 when it is momentarily closed. Many other useful variations of this DC static switch can be devised, among them the following circuits.

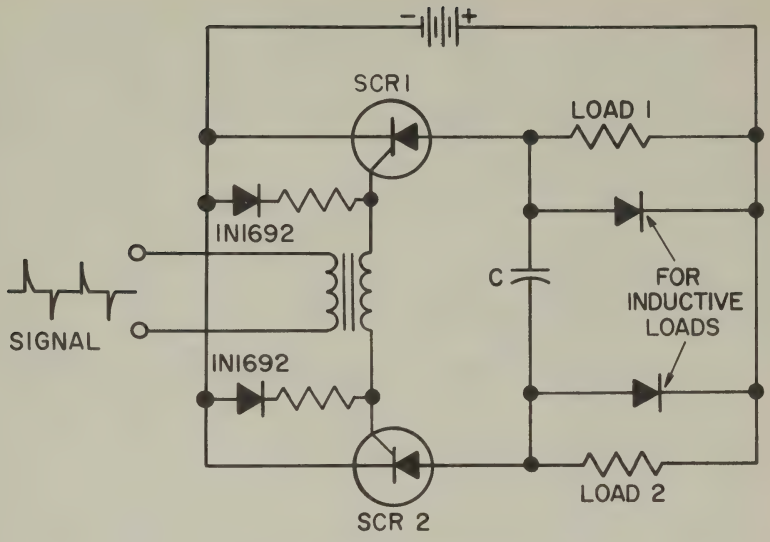
7.7 FLIP-FLOP AND DC LATCHING RELAY

Figure 7.7 is a power flip-flop or latching relay which transfers voltage from one load to the other each time the pulse train reverses polarity. The signal may also consist of a sinewave or square wave, and the coupling transformer may be of the saturating type.

7.8 SCR CURRENT-LIMITING CIRCUIT BREAKERS

In some phase controlled applications, the fault current due to a short circuit may reach destructive proportions within one-half cycle. This would prohibit use of conventional circuit breakers for protection. Also, in some types of inverters operating on DC it may be desirable to have a fast electronic circuit breaker in the event of loss of commutation in the inverter for any reason.

An SCR current limiting circuit breaker of the type shown in its simplest form in Figure 7.8 will provide these protective functions very nicely. This

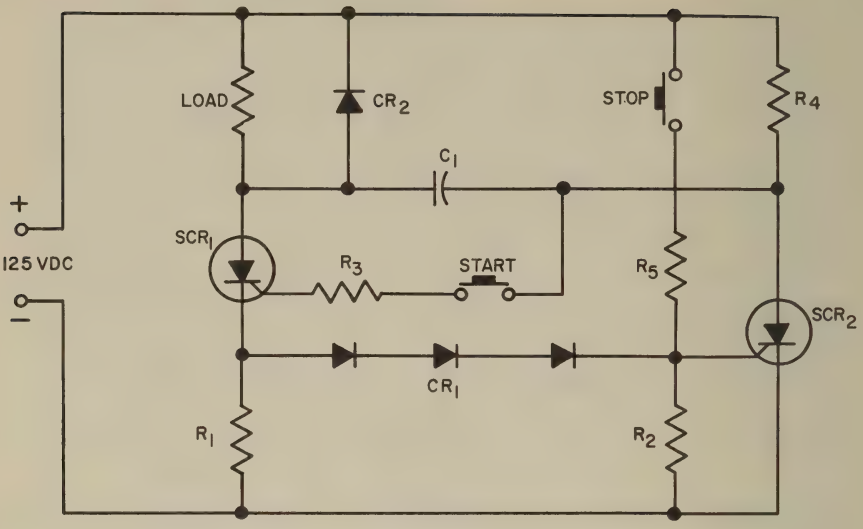


Latching Relay or Flip-Flop
Figure 7.7

package can be inserted in series with the DC output of a phase-controlled rectifier or in series with the DC input to an inverter circuit.

The circuit breaker is basically a parallel capacitor commutated flip-flop. When the "Start" button is momentarily depressed, SCR_1 starts to conduct and delivers power to the load provided the load current is above the minimum holding current of SCR_1. Capacitor C_1 then charges to the load voltage through R_4, the right hand terminal of C_1 being positive with respect to the left hand terminal. When SCR_2 is fired by momentary closing of the "Stop" button, the positive terminal of capacitor C_1 is connected to the cathode of SCR_1, reversing the polarity across this SCR and turning it off. This interrupts the flow of load current and opens the circuit. SCR_2 will also be fired by the voltage developed across R_1 by load current if this exceeds the forward voltage drop of the string of series diodes CR_1 plus the gate firing requirements of SCR_2. By adjustment of the value of R_1 and by selecting the proper number of series diodes CR_1, the circuit can be made to trip out and interrupt overload or fault current at any predetermined level. For a more consistent tripping level under temperature variations, a zener diode can be substituted in place of all but one of the series diodes at CR_1. For still more precise tripping, a UJT overcurrent senser can be used.

The characteristics of the newly developed tunnel diode are also very useful in developing a gate signal when a specific level of current is exceeded. The tunnel diode has a very stable peak current at which it switches from a low resistance to a relatively high resistance. This, combined with a very low voltage drop makes it almost ideal for this type of application. A tunnel diode overcurrent detecting circuit for the circuit breaker in Figure 7.8 is shown in Figure 7.9. Main load current flows through SCR_1 and R_1. Part of the load is shunted

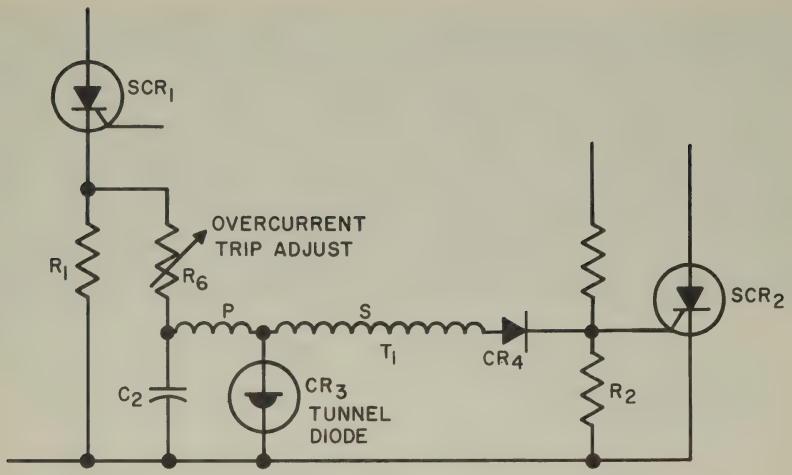


$R_1 \cong 3/I_{trip}$ OHMS NON-INDUCTIVE
R_2 — 220 OHMS, 1/2 WATT
R_3 — 100 OHMS, 1/2 WATT
R_4 — 2200 OHMS, 10 WATTS
R_5 — 2200 OHMS, 5 WATTS
$C_1 \geqq 0.4 I_{trip}$ MFD
SCR_1, SCR_2 — G.E. C40B
CR_1 — (3) G.E. IN1692
CR_2 — G.E. IN2158

16 Ampere DC Circuit Breaker
Figure 7.8

through R_6, tunnel diode CR_3, and the primary winding of T_1, R_1 and R_6 are selected so that less than ½ amp flows through the tunnel diode at maximum rated load. Under this condition CR_3 remains in its low resistance state. If the main load current rises to the point where more than ½ amp flows through CR_3, it switches instantaneously to its high resistance state. If the current through the tunnel diode is maintained constant through the switching interval, the voltage across it increases about five-fold. This sudden change in voltage across CR_3 induces a pulse of voltage in the primary of T_1 which is stepped up by autotransformer action and applied to the gate of SCR_2, thereby tripping the circuit breaker. The tripping point is stable within a few percent over a wide temperature range and is independent of the firing characteristics of SCR_2.

The component values in Figure 7.8 apply for a 125 volt DC system. When using the C40 SCR, the tripping current level should not exceed 100 amperes in order to stay within the switching rating of SCR_2.



R_1 —— $\approx 3/I_{trip}$ -OHMS, NON-INDUCTIVE
R_2 —— 47 OHMS, 1/2 WATT
R_6 —— 10 OHM, LINEAR POT
C_2 —— 2 MFD, 200 VOLT
CR_3 —— GERMANIUM TUNNEL DIODE WITH $I_{PK} = 0.5A$
CR_4 —— G.E. IN91
T_1 —— AIR CORE TRANSFORMER, 1/4" DIA., P = 50T, S = 500T, #26 AWG

Tunnel Diode Current Sensing and Trip Circuit for Figure 7.8
Figure 7.9

Because of the fast switching action of SCR's, short circuit current can be interrupted long before it reaches destructive levels. In typical stiff systems with rates of fault current rise on the order of 10 million amperes per second, this type of switch has limited the peak fault current to less than 50 amperes and has interrupted the fault in as little as 20 microseconds after its inception.

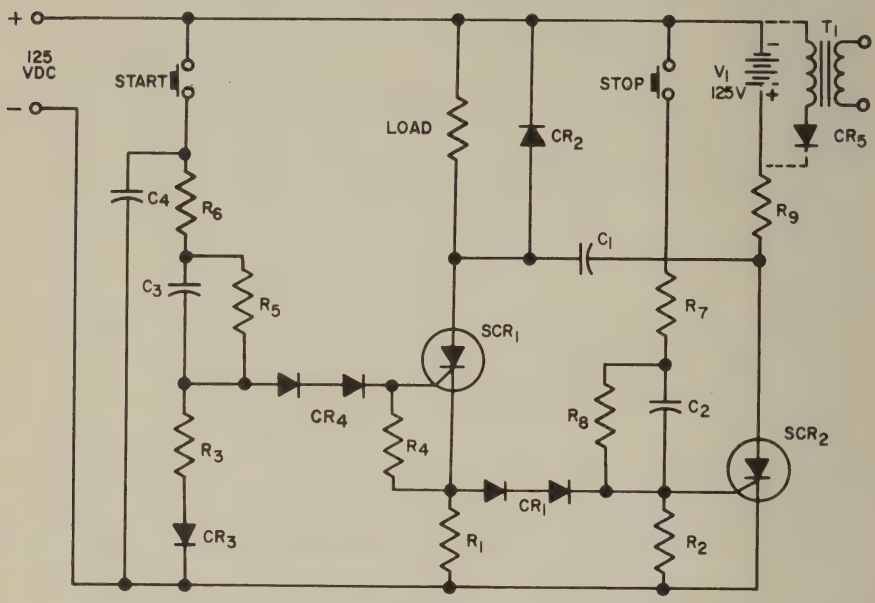
In some high reliability applications the flip-flop action of this circuit can be used as a high speed transfer switch in the event of a fault in one load. For instance, both the load in series with SCR_1 and the load represented by R_4 in Figure 7.8 could be DC motors, driving a common load. If the main drive motor in series with SCR_1 should fail short, it would be disconnected from the line and power would be applied to the standby motor R_4 within a matter of microseconds after the fault occurred.

C_1 must have sufficient capacitance to commutate the fault current at the point of tripping. Expressed another way, it must reverse bias SCR_1 for at least 12 microseconds if SCR_1 is to reliably recover its open state and block further flow of fault current.

For proper operation of Figure 7.8, SCR_1 must be conducting normally before the fault condition occurs in order to build up commutating voltage across

C_1. After it has been tripped out after a fault occurs, it is very likely the operator of the equipment will try to start it again. If a fault exists in the load, no voltage will build up across C_1 and it will no longer be possible to interrupt the fault current by commutating SCR_1.

To avoid this possibility, a circuit variation such as shown in Figure 7.10 can be adopted. Here C_1 is precharged to approximately line voltage by an auxiliary power supply represented by battery V_1 or a half wave rectifier CR_5

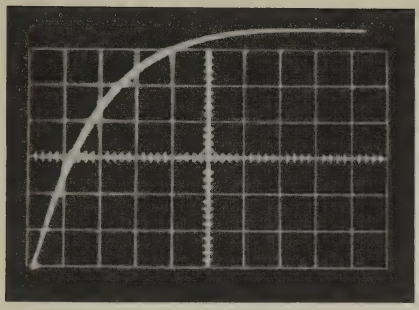


R_1	0.25 OHMS NON-INDUCTIVE	C_1	6 MFD PAPER, 400 V.
R_2	220 OHMS, 1/2 WATT	C_2, C_3	0.1 MFD PAPER, 400 V.
R_3	5 OHMS, 1/2 WATT	C_4	1.0 MFD PAPER, 400 V.
R_4	22 OHMS, 1/2 WATT	SCR_1, SCR_2	G-E C40B
R_5, R_8	1 MEG, 1/2 WATT	CR_1, CR_4	(4) G-E IN1692
R_6, R_7	56 OHMS, 1/2 WATT	CR_2	G-E IN2158
R_9	2200 OHMS, 30 WATT	CR_3, CR_5	G-E IN1693

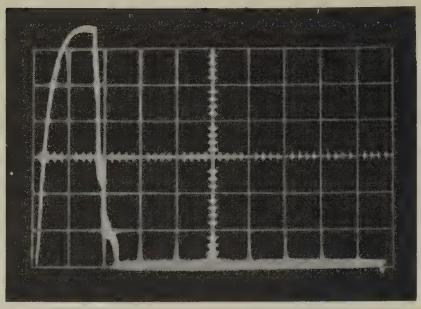
Circuit Breaker with Tripping Protection When Closing on a Short Circuit
Figure 7.10

and transformer T_1. If, when SCR_1 is turned on by the "Start" button, normal load current flows, the circuit will continue to operate similar to Figure 7.8. If on the other hand, a short circuit exists in the load, SCR_2 will fire as soon as the fault current through R_1 reaches its tripping value. The precharge on C_1 will turn off SCR_1 and return the circuit to the off state. As long as the fault exists, it will be impossible to keep the circuit turned on.

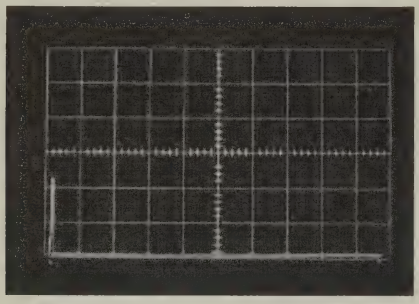
Figure 7.11A shows the rise of short circuit current to about 150 amperes maximum available in about 0.6 millisecond. The oscillogram was taken by



(A) Available Fault Current With SCR 1 Shorted Out (Horizontal — 100 μSec/ Large Division)



(B) With 15 Amp Current Limiting Fuse Substituted for SCR 1 (Horizontal — 500 μSec/Large Division)



(C) With SCR 1 in Circuit as Shown in Figure 7.10 (Horizontal — 500 μSec/Large Division)

Load Current in Circuit of 7.10 when Closing on Short Circuit (Vertical = 22.5 Amp. per large Division) Figure 7.11

shorting the SCR_1 externally with a dead short already existing in the load. The maximum available current was limited to about 150 amperes by the DC supply impedance and the rate of rise of fault current was limited by inherent circuit inductance estimated at 100 microhenries.

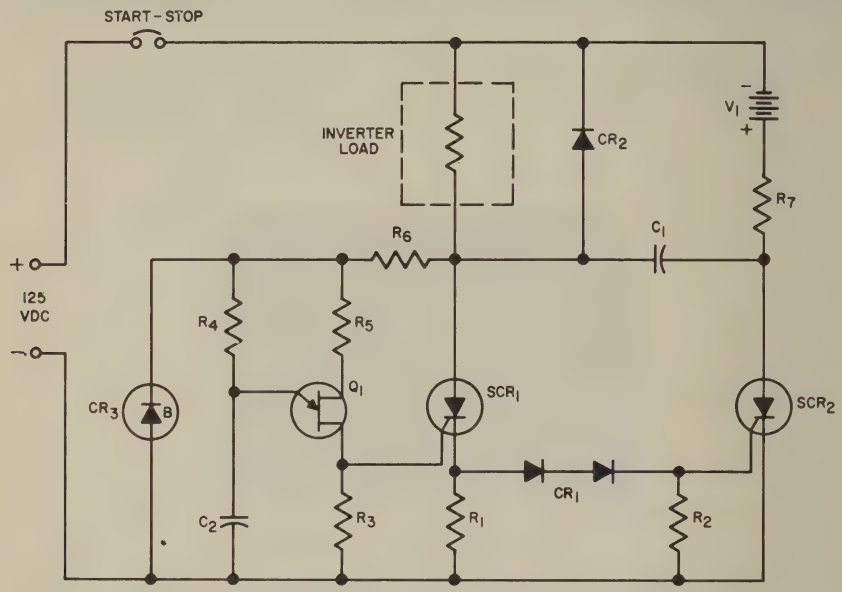
Figure 7.11B illustrates the action of a 15 ampere fast-acting current limiting fuse in series with the current. (Time scale is compressed 5 times from 7.11A.) Note that the current still reaches maximum available value and that it requires 1.2 milliseconds to detect and interrupt the fault.

Figure 7.11C shows the fault current using the SCR circuit breaker. The same short exists in the load as for the oscillograms in Figures 7.11A and 7.11B. SCR_1 is turned on by depressing the "Start" button, but before the current is able to exceed 50 amperes, SCR_2 is fired and the circuit is interrupted. Total

interrupting time is approximately 50 microseconds. Unlike a fuse, the SCR need not be replaced after performing its function.

The arrangement of capacitors, resistors, and diodes in the gate circuit of SCR_1 are necessary to prevent contact bounce of the "Start" button from supplying a multiple gate signal to SCR_1. If more than a single pulse would be applied to the gate of SCR_1, malfunctioning of the circuit would occur when closing the circuit breaker on a fault condition.

An automatic reclosing version of the current limiting circuit breaker is shown in Figure 7.12. As shown, this circuit is connected to the supply voltage



R_1	≅ 3/Itrip OHMS, NON-INDUCTIVE	C_1	≅ 0.4 Itrip MFD
R_2	220 OHMS, 1/2 WATT	C_2	0.1 MFD
R_3	47 OHMS, 1/2 WATT	SCR_1, SCR_2	G-E C40B
R_4	1 MEG, 1/2 WATT	CR_1	(2) G-E IN1695
R_5	150 OHM, 1/2 WATT	CR_2	G-E IN2158
R_6	5600 OHM, 2 WATT	CR_3	IN1529 BREAKDOWN DIODE
R_7	2000 OHM, 10 WATT	Q_1	G-E 2N1671B

Circuit Breaker with Automatic Reclosing
Figure 7.12

by a series switch labeled "START-STOP" although this function could also be incorporated into the SCR triggering with additional circuitry. As soon as the main line switch is closed, positive anode voltage is applied to SCR_1. This voltage is reduced by the regulator action of R_6 and CR_3 and applied to the UJT relaxation oscillator formed by Q_1 and its associated components. After a timing interval determined by the time constant of R_4 and C_2, Q_1 triggers and fires SCR_1. As soon as SCR_1 fires, it closes the circuit to the load. Since its anode potential is now essentially at ground potential, voltage no longer is applied to

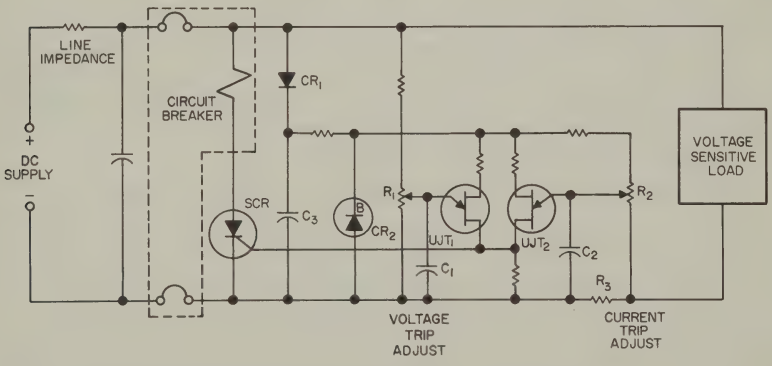
Q_1 and no further gate signals are generated. If a short circuit or an overload occurs, SCR_2 will fire and open the load circuit by turning off SCR_1. Positive voltage again appears at the anode of SCR_1 and a new timing cycle is initiated. If, when SCR_1 is again triggered, the fault condition still exists in the load, SCR_1 will be turned off as soon as the load current reaches the tripping level of SCR_2. This action will continue indefinitely until the overload condition or fault is removed from the load. As soon as this correction takes place, the circuit will automatically continue into normal operation.

This circuit is particularly useful in series with the DC supply feeding capacitor commutated inverter circuits. If for any reason the inverter fails to commutate, the resulting fault condition will trip the SCR circuit breaker and interrupt the fault current. As soon as the UJT circuit times out, the circuit breaker will automatically reclose, thus starting the inverter again. The speed of interruption and reclosing is fast enough, that only a relatively minor disturbance can be noticed in the output of a typical inverter.

The permissible delay time between opening the circuit and reclosing it is limited only by the speed with which V_1 can again build up a commutating charge on C_1, and by thermal considerations in SCR_1 and SCR_2. The delay time before reclosing must be substantially more than the time constant of R_7C_1, and the thermal limitations on SCR_1 and SCR_2 can be determined for a given set of conditions by the intermittent duty rating techniques discussed in Chapter 3. The circuit of Figure 7.12 has successfully operated at a delay time of less than 10 milliseconds between opening and reclosing.

7.9 HIGH SPEED SWITCH OR "ELECTRONIC CROWBAR"

A form of "electronic crowbar," shown in Figure 7.13, has proved very useful for protecting DC circuits against input line voltage transients and short circuit load conditions. If the DC supply exceeds the desired maximum value as determined by the setting of potentiometer R_1, the voltage at the emitter of UJT_1 exceeds the peak point voltage causing UJT_1 to fire which in turn fires



Electronic Crowbar Protection of DC Circuits Against Overvoltage and/or Overcurrent
Figure 7.13

the SCR. The full supply voltage is then applied to the circuit breaker trip coil causing the circuit breaker to open the main DC supply bus. Besides increasing the speed of the circuit breaker action this circuit instantly loads down the DC bus, preventing the voltage on the load from rising until the circuit breaker has time to operate. The circuit also protects the load and the supply against short circuit conditions by monitoring the current through resistor R_3. When the voltage across R_3 exceeds the desired maximum value as determined by the setting of potentiometer R_2 the voltage at the emitter of UJT_2 exceeds the peak point voltage, causing UJT_2 and the SCR to fire as before. Due to the stable firing voltage of the UJT the trip voltage across R_3 can be very low, a value in the range from 100 millivolts to 500 millivolts being suitable for most applications. If only overvoltage protection is desired the circuit of Figure 7.13 can be simplified by eliminating UJT_2 and its associated circuitry. Similarly, if only overcurrent protection is desired UJT_1 and its associated circuitry can be eliminated.

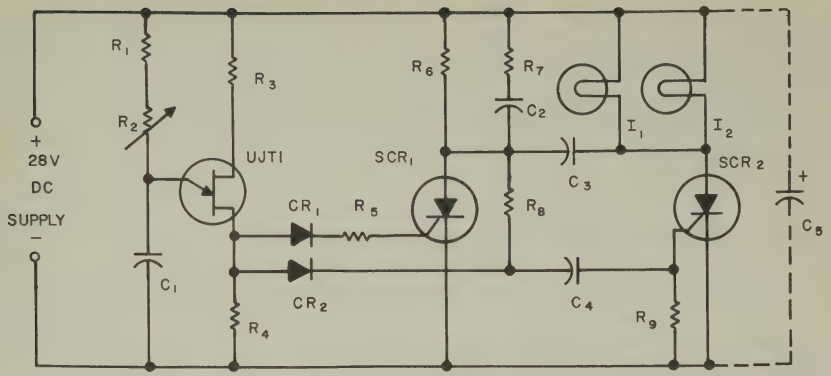
In the circuit of Figure 7.13 rectifier CR_1 and capacitor C_3 are used to provide filtering against negative voltage transients which would otherwise result in false tripping of the circuit. The values of potentiometer R_1 and R_2 are chosen to have appropriate time constants with C_1 and C_2 so as to give the desired voltage-time response in the tripping action.

The SCR is ideal for this type of circuit because of its ability to switch on within a few microseconds after being triggered. Its high surge rating permits it to carry momentary currents as high as 2000 amperes for 2 milliseconds without damage in the case of the 2N1909 SCR series.

7.10 FLASHER CIRCUIT

Flasher circuits for incandescent lamps are widely used in a variety of applications such as traffic lights, navigational beacons, aircraft beacons and illuminated signs. The SCR is ideally suited for this type of application since it can function over a wide range of current and voltage with a much higher degree of reliability than the commonly used electromechanical systems. The SCR also offers an advantage over power transistors in that it does not require an excessive derating of current in order to handle the high inrush currents of incandescent lamps. The UJT makes an ideal partner for the SCR in this type of application since it permits an economical method for obtaining a wide frequency range and a high degree of frequency stability.

The circuit shown in Figure 7.14 has been chosen to illustrate the basic principles of an SCR/UJT flasher which can be easily simplified or modified to meet specific application requirements. The circuit as shown operates a lamp load of up to 3 amperes over a supply voltage range of 17 to 35 volts and a temperature range of −50°C to 100°C. This circuit is basically a parallel inverter with capacitor commutation. The SCR's conduct alternately and are triggered by the free running UJT relaxation oscillator. The frequency of the relaxation is determined by the time constant, $(R_1 + R_2)\ C_1$, and may be adjusted to the value desired by means of potentiometer R_2.



R_1	750K, 1/2 WATT	C_1, C_2	0.47 μfd, 50 VOLTS
R_2	500K, LINEAR POT	C_3	2 μfd, 100 VOLTS
R_3	270 Ω, 1/2 WATT	C_4	0.22 μfd, 50 VOLTS
R_4	100 Ω, 1/2 WATT	C_5	50 μfd, 50V
R_5	18 Ω, 1/2 WATT	SCR_1	G-E 2N1930
R_6	250 Ω, 5 WATT	SCR_2	G-E C12F
R_7	47 Ω, 1/2 WATT	CR_1, CR_2	G-E 1N1692
R_8	4.7K, 1/2 WATT	I_1, I_2	G-E 50C, 1.4A LAMP
R_9	2.2 K, 1/2 WATT	UJT1	G-E 2N1671B

High Power Electronic Flasher
Figure 7.14

Special consideration must be given to the proper starting of the circuit. When the supply voltage is first applied both SCR's are off, and if a pulse is applied to the gates of both SCR's simultaneously they will both turn on and the circuit will fail to function. This problem is overcome by means of the gating action of CR_2, R_8, and C_4. If SCR_1 is off it will be turned on by the first trigger pulse, but SCR_2 will not be turned on since CR_2 is reverse biased by approximately 28 volts and hence blocks the trigger pulse from the gate of SCR_2. If SCR_1 is on, however, then CR_2 will be reverse biased by less than 1 volt so that the trigger pulse will be able to fire SCR_2 which then turns off SCR_1 through the action of commutating capacitor C_3. In this case triggering SCR_1 and SCR_2 at the same time is permissible since the time constant R_6C_3 is much longer than the trigger pulse width so that SCR_1 remains reverse biased after the end of the trigger pulse long enough to assure reliable commutation of SCR_1.

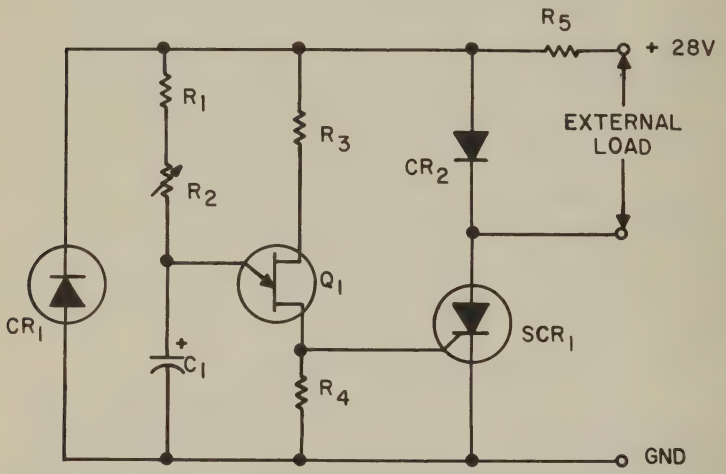
Resistor R_7 and capacitor C_2 are used in the anode of SCR_1 to furnish a higher current to SCR_1 during the commutating interval so as to prevent SCR_1 from improperly turning off due to the effect of inductance in the power supply. In some cases it may also be necessary to place a capacitor C_5 directly across the circuit as shown or to reduce the value of R_6.

For higher values of supply voltage or for greater frequency stability a Zener diode with a dropping resistor can be used to provide the bias voltage

for the UJT. The circuit as shown operates the lamps at a 50% duty cycle. For operation at other values of duty cycle an appropriate value of resistance can be connected between the emitter of the UJT and the anode of one of the two SCR's. If independent adjustment of the on and off time of the load is required, a version of the hybrid timing circuit can be used (GE Transistor Manual, 5th Edition, pages 145-147).

7.11 TIME DELAY CIRCUITS

Time delay circuits are used frequently in industrial controls and aircraft and missile systems to apply or remove power from a load a predetermined time after an initiating signal is applied. Cascaded time delay circuits can be used to sequentially perform a series of timed operations.



R_1 - 2.2K, 1/2 WATT
R_2 - 1K TO 500K LINEAR POT
R_3 - 150 Ω, 1/2 WATT
R_4 - 27, Ω, 1/2 WATT
R_5 - 560 Ω, 2 WATT

C_1 - 0.2 TO 100 mfd, 15 V
SCR_1 - G-E 2N1930 OR 2N1771
CR_1 - 18 V, 10%, 1 WATT ZENER
CR_2 - G-E 1N1692
Q_1 - G-E 2N1671B

Precision Solid State DC Time Delay Circuit
Figure 7.15

Figure 7.15 illustrates an extremely simple yet accurate and versatile solid state time delay circuit. The operating current and voltage of the circuit depend only on the proper choice of the SCR. Resistor R_5 and Zener diode CR_1 provide a stable voltage supply for the UJT. Initially SCR_1 is off and there is no voltage applied to the load. Timing is initiated either by applying supply voltage to the circuit or by opening a shorting contact across C_1. The timing capacitor C_1 is charged through R_1 and R2 until the voltage across C_1 reaches

the peak point voltage of the UJT at which time the UJT fires, generating a pulse across R_4 and firing SCR_1. The full supply voltage minus the SCR drop then appears across the external load terminals. Holding current for SCR_1 is provided by the current through R_5 and CR_2. Thus the external load may be removed or connected at any time without affecting the performance of the circuit. When SCR_1 fires, the voltage across the UJT drops to less than 2 volts due to the clamping action of CR_2. This acts to rapidly set and maintain a low voltage on C_1 so that the time interval is maintained with reasonable accuracy if the circuit is rapidly recycled. For the highest accuracy, however, additional means must be used to rapidly and accurately set the initial voltage on C_1 at the beginning of the timing cycle.

The time delay of the circuit depends on the time constant $(R_1 + R_2)\,C_1$ and can be set to any desired value by appropriate choice of R_1, R_2, and C_1. The upper limit of time delay which can be achieved depends on the required accuracy, the peak point current of the UJT, the maximum ambient temperature, and the leakage current of the capacitor and UJT (I_{EO}) at the maximum ambient temperature. The absolute upper limit for the resistance $R_1 + R_2$ is determined by the requirement that the current to the emitter of the UJT be large enough to permit it to fire (i.e. be greater than the peak point current) or

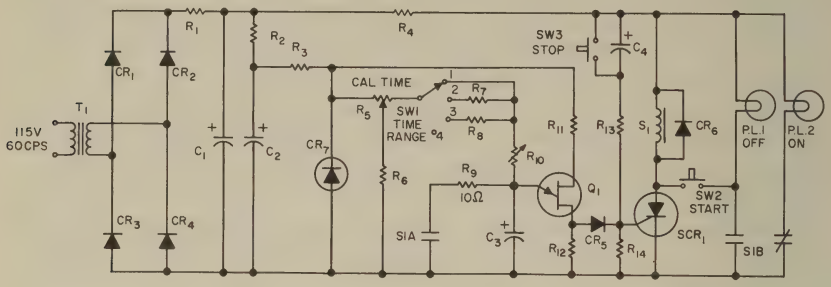
$$R_1 + R_2 < \frac{(1 - \eta)\ V_1}{\frac{25I_P}{V_1} + I_c} \qquad (7.3)$$

where η is the maximum value of intrinsic standoff ratio, V_1 is the minimum supply voltage on the UJT, I_P is the maximum peak point current measured at an interbase voltage of 25 volts, and I_C is the maximum leakage current of the capacitor at a voltage of ηV_1. If high values of capacitance are required it is desirable to use stable, low leakage types of tantalytic capacitors. If tantalytic or electrolytic capacitors are used it is necessary to consider forming effects which will cause the effective capacitance and hence the period to change as a function of the voltage history of the capacitor. These effects can be reduced by applying a low bias voltage to the capacitor in the standby condition. In some cases where operation at high ambient temperature is not required a smaller capacitor can be used by adding a UJT oscillator circuit which generates negative pulses of approximately 0.3 to 0.5 volts peak at base two of Q_1. These pulses act to reduce the effective value of peak point current of Q_1 by a factor of as much as 100, thus permitting the use of a larger value of charging resistance $(R_1 + R_2)$ and hence a lower value of capacitance (C_1). This frequently permits the use of a low leakage paper or polyester-film capacitor in place of an expensive tantalytic capacitor.

The resistor R_3 can serve as a temperature compensation for the circuit, increasing the value of R_3 causes the time delay interval to have a more positive temperature coefficient. The overall temperature coefficient can be set exactly zero at any given temperature by careful adjustment of R_3. However, ideal compensation is not possible over a wide range because of the nonlinear effects involved.

To reset the circuit of Figure 7.15 in preparation for another timing cycle

SCR_1 must be turned off either by momentarily shorting it with a switch contact or by opening the DC supply.



R_1 — 2Ω, 1 WATT
R_2, R_3 — 330Ω, 1/2 WATT
R_4 — 35Ω, 5 WATT
R_5 — 2.5K, LINEAR POT
R_6 — 25K, 1/2 WATT
R_7 — 100K, 1/2%, 1/2 WATT
R_8 — 200K, 1/2%, 1/2 WATT
R_9 — 10Ω, 1/2 WATT
R_{10} — 100K, 10 TURN HELIPOT
R_{11} — 150Ω, 1/2 WATT
R_{12} — 18Ω, 1/2 WATT
R_{13} — 1.2K, 2 WATT
R_{14} — 100Ω, 1/2 WATT
C_1 — 500μFD, 50V
C_2 — 100μFD, 50V
C_3 — 100μFD, 20V TANTALUM
C_4 — 10μFD, 50V
SCR_1 — G-E 2N1930
CR_1 — CR_6 — G-E 1N1692
CR_7 — 18V, 10%, 1WATT ZENER
Q_1 — G-E 2N1671B
S_1 — G-E CR2791G122A4 4PDT RELAY
PL_1, PL_2 — G-E 1477, 24V LAMP
T_1 — 115V/25V 1A TRANSFORMER

Variable Time Control Circuit
Figure 7.16

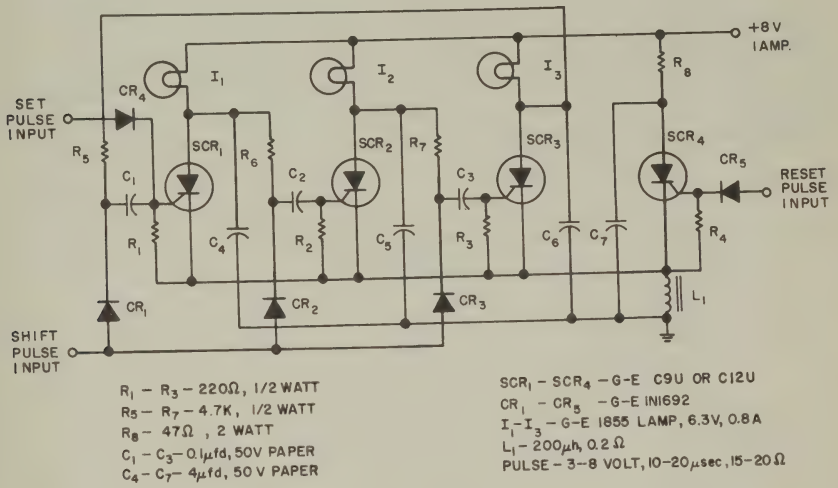
Figure 7.16 illustrates a time delay circuit using a relay output with a push button initiation of the timing sequence. In the quiescent state SCR_1 is on and relay S_1 is energized. Contact S_1A is closed, shorting out the timing capacitor C_3. To initiate the timing cycle push button switch SW_2 is momentarily closed which shorts SCR_1 through contact S_1B causing SCR_1 to turn off. When SW_2 is released S_1 is deenergized and the timing sequence begins. The particular configuration of SW_2 and S_1B is used to prevent improper operation in case SW_2 is closed again during the timing cycle. Capacitor C_3 is charged through R_5 and R_{10} until the voltage across C_3 reaches the peak point voltage of Q_1 causing Q_1 to fire. The positive pulse generated across R_{12} fires SCR_1 which pulls in the relay and ends the timing cycle. The timing cycle can be terminated at any time by push button switch SW_3 which causes current to flow in R_{13} thus firing SCR_1. Capacitor C_4 supplies current through R_{13} during the instant after the supply is turned on thus firing SCR_1 and setting the circuit in the proper initial state.

The timing interval is determined by the setting of a precision ten turn helipot R_{10} which may be set from 0.25 to 10.25 seconds in increments of 0.01 second. The initial setting of 0.25 seconds takes into account the added series resistance of the time calibration potentiometer R_5. Additional series resistance of 100K and 200K may be added by SW_1 to extend the time range by 10 seconds and 20 seconds. A fourth position of SW_1 open circuits the timing resistors and thus permits unrestricted on-off control of the circuit.

Tests of the circuit have shown an absolute accuracy of 0.5% after initial calibration and a repeatability of 0.05% or better.

7.12 RING COUNTER

A ring counter may be considered as a circuit which sequentially applies voltage to two or more loads one at a time. These may either be power loads or signal loads. An SCR flip-flop (Figure 7.7) is thus a two stage ring counter and most SCR ring counters are simply an extension of the basic flip-flop circuit with minor modifications in the pulse gating circuitry and the commutating circuitry. Several configurations of the SCR ring counter are possible differing mainly in the commutating principle used, but the circuit of Figure 7.17 is presented as being one of the most versatile and as offering a good example of the principles involved.



Three Stage SCR Ring Counter Circuit
Figure 7.17

In this circuit SCR_1, SCR_2, and SCR_3 form a three stage ring counter. SCR_4 is a reset pulse generator which is not required for all applications. When power is first applied to the circuit none of the SCR's will turn on. To "set" the circuit a positive pulse is applied to the "set pulse input" which turns on SCR_1 and applies voltage to the lamp load I_1. The diodes CR_1 and CR_3 will be reverse biased by 8 volts while CR_2 will be reverse biased by less than 1 volt as determined by the voltages on the anodes of the various SCR's. If a positive pulse with a peak amplitude of less than 8 volts and greater than 3 volts is applied to the "shift pulse input," CR_1 and CR_3 will block the pulse from the gate of SCR_1 and SCR_3 while the pulse will be transmitted to the gate of SCR_2 through CR_2 and C_2 causing SCR_2 to turn on. When SCR_2 turns on the discharge current of C_5 through SCR_2 causes a large voltage pulse to appear across inductor L_1 thus reverse biasing SCR_1 and causing it to turn off. Note that C_4 serves to hold the anode voltage of SCR_1 down during the commutating interval. When the next shift pulse occurs SCR_3 turns on and SCR_2 turns off in a similar manner, SCR_1 turns on and SCR_2 turns off, etc.

If a pulse occurs at the "reset pulse input" at any time SCR_4 will fire and turn off any of the other SCR's which happens to be on at the time. SCR_4 will then remain on until one of the other SCR's turns on which will then cause SCR_4 to turn off. Additional stages can be added to the circuit as desired. A ten stage circuit using 10 SCR's can be used to perform the function of a decade counter with direct lamp readout.

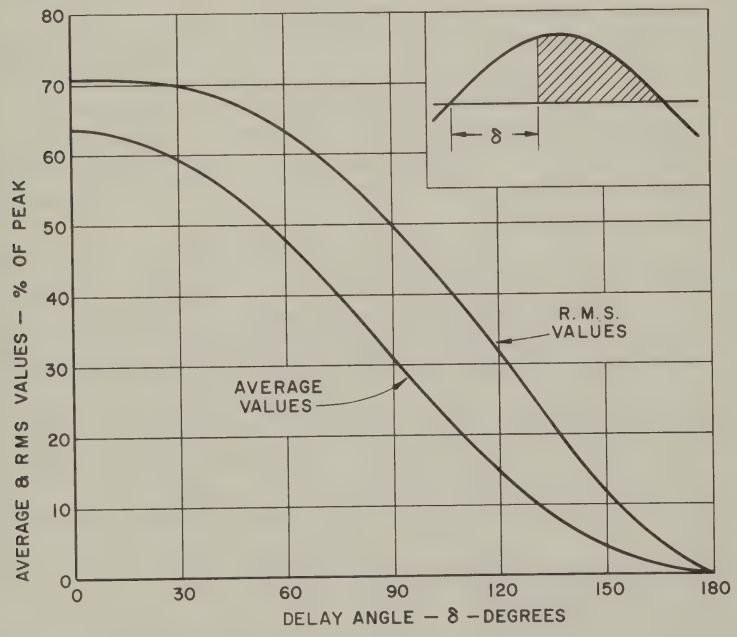
The circuit as shown can function as a shift register in which any combination of SCR's can be on at one time and the entire pattern will move one stage to the right each time a pulse occurs at the trigger pulse input. The circuit also has the advantage that the commutation pulses do not appear across the loads that are not being switched.

An alternate version of the circuit in which the commutating capacitors C_4, C_5, and C_6 are connected between the anodes of the adjacent SCR's can be used if only simple ring counter operation is required and if the appearance of the commutating pulses across all the loads is not objectionable. This version permits both the commutating capacitors and the commutating inductor to be reduced by a factor of 2 for a given load over that for the circuit of Figure 7.17.

8.1 PRINCIPLE OF PHASE CONTROL

In an AC circuit the SCR must be triggered into conduction at the desired instant of time during the half-cycle of the applied voltage wave during which the anode is positive. The "static" AC switch is typically triggered at the beginning of the voltage wave resulting in "on-off" operation, as discussed in the previous chapter. In the phase controlled circuit, initiation of conduction is delayed by an angle δ so that the SCR conducts for only a predetermined portion of the positive half-cycle. In this manner the average power delivered to the load can be varied, resulting in continuously variable operation from full "off" to full "on." Figure 8.1 illustrates the effect of this delayed firing or phase-control on the average and RMS output voltage and current in single phase full-wave AC or DC resistive load circuits.

Common to all AC circuits is the manner in which the SCR is turned-off. Since the line voltage reverses every half-cycle the SCR will be commutated by



Average and RMS Values of Output Voltage and Current Single Phase Full Wave Phase Controlled Circuits Resistive Load
Figure 8.1

the supply line. This is in contrast to SCR operation in DC circuits where special means have to be taken to commutate the device, as discussed in Chapters 5 and 9.

The basic power circuits fall into two classes depending on whether the load is AC or DC in nature. Basic AC load circuitry is described in Sections 8.2, 8.3 and 8.4. Substituting SCR's for diode rectifiers in conventional rectifier circuits allows supplying variable power to DC loads from an AC line. Some basic DC load circuits are discussed in the remaining sections of this chapter.

A variety of firing circuits is possible, as discussed in Chapter 4. The firing circuits in this chapter are of the unijunction transistor type.

8.2 BASIC PHASE CONTROLLED AC SWITCH

Figure 8.2(A) shows a typical circuit of this type—a parallel-inverse, or back-to-back, circuit. It is a fundamental AC control circuit used in lighting and heating (temperature) control, and in voltage regulation.

With the unijunction transistor firing circuit it draws on the voltage developed across the SCR's during blocking for the interbase supply and synchronization for the unijunction transistor. The firing circuit is connected to the output of a single phase bridge formed by diodes CR_1, CR_2, CR_3, and CR_4. Through the action of these diodes, zener regulating diode CR_5, and resistor R_3, a clipped and rectified voltage with a waveform as shown in Figure 8.2(B), is applied to the UJT and its emitter circuit.

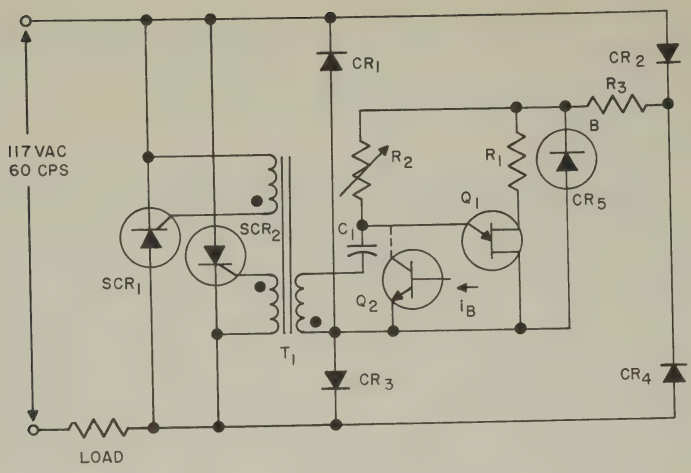
The power capabilities of this circuit are limited only by the size and number of SCR's used. Typically, with two high current G-E 2N1909 SCR's the circuit is capable of continuous control up to 34 kw in a 220 VAC circuit.

Transistor Q_2 in Figure 8.2(A) is shown to illustrate that only a small base current is required to control the full power output of the circuit. The analysis of a transistor-controlled unijunction firing circuit is given in Sections 4.15.2 and 4.15.3 of Chapter 4.

When this circuit is used to control highly inductive loads it can happen, particularly at small conduction angles, that current build-up is delayed sufficiently so that the triggering signal is removed before SCR holding current has been reached. In this case the SCR will not remain in the on-state. If the other SCR does fire on the next half-cycle, the DC component in the load circuit may saturate the inductive load or the supply transformer core. Also, with two SCR's having dissimilar holding currents, one may drop out before the other one at the end of the conduction period; this type of operation will also contribute a small DC component to the load current.

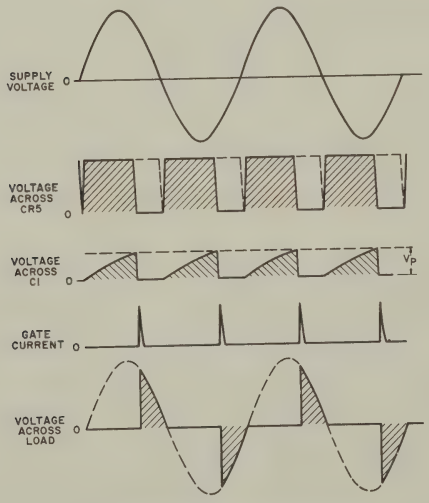
This situation, should it arise, can be resolved by some of the following alternatives:

1. Use of the bridge circuit described in Section 8.3;
2. Square wave gate drive;
3. Sufficiently low value of bleeder resistance across the load;
4. Prevent operation of firing circuit below a minimum phase retard angle;
5. RC filter anode to cathode designed to supply current to the SCR while load current builds up.



R_1	390Ω
R_2	100,000Ω LINEAR POT
R_3	3300Ω, 5 WATT
C_1	0.2 MFD
SCR_1, SCR_2	G-E 2N685
CR_1, CR_2, CR_3, CR_4	G-E IN1695
CR_5	IN1527 ZENER DIODE, ONE WATT, 22 VOLTS
Q_1	G-E 2N1671A
T_1	PE 2231, UTC H51, OR EQUIVALENT

AC Phase Controlled Switch
Figure 8.2 (A)

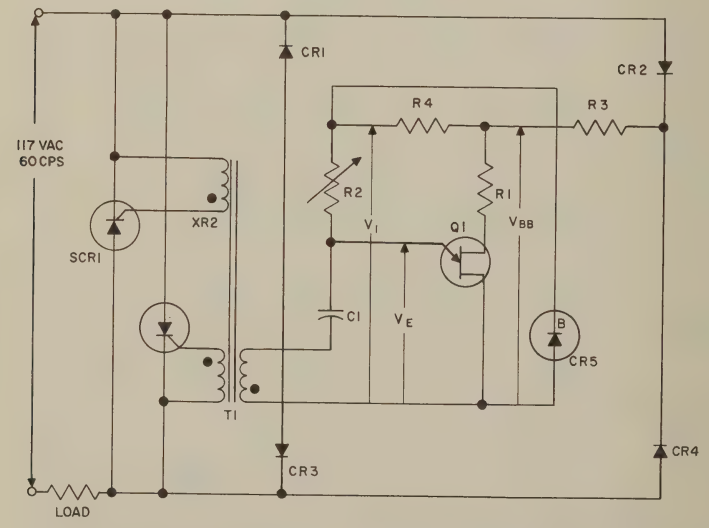


Waveshapes in AC Phase Controlled Switch
Figure 8.2 (B)

The basic AC switch circuit of Figure 8.2(A) can be easily modified to provide regulation for input line voltage variations. The circuit as shown would vary its output as the line voltage changes. With the circuit shown in Figure 8.3(A) a regulation feature can be added to the circuit for the cost of an additional small resistor.

This circuit is identical to that given in Figure 8.2(A) except that resistor R_4 has been added and the zener diode is connected at the common point of R_2 and R_4. With this modification the charging voltage for the capacitor is equal to the zener voltage and is essentially constant over the half cycle prior to the instant when the SCR is fired. This is shown in the waveforms of Figure 8.3(B). The interbase voltage, V_{BB}, of the UJT is not constant during this interval, but is equal to the breakdown voltage of the zener diode plus a small fraction of the line voltage determined by the voltage dividing ratio of R_3 and R_4. Thus at any given phase angle the interbase voltage will increase if the line voltage increases as shown in Figure 8.3(B). The peak point voltage of the unijunction transistor is equal to the interbase voltage times the standoff ratio and is given in Figure 8.3(B) to correspond to the two interbase voltage curves.

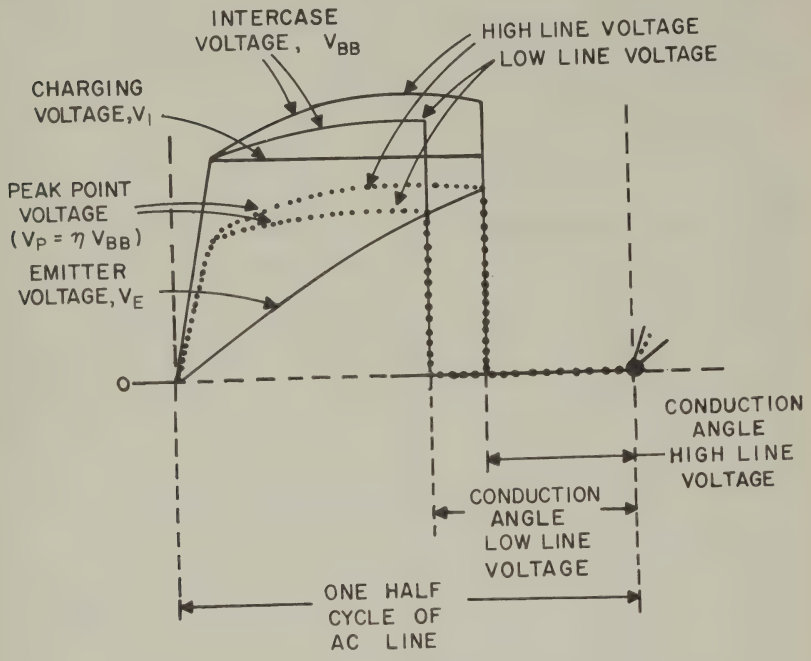
The emitter voltage follows the normal exponential charging characteristic since the charging voltage, V_1, is constant. The UJT and SCR's fire when the emitter voltage equals the peak point voltage. It is readily apparent from Figure 8.3(B) that, as the line voltage increases, the delay before the UJT and SCR's are fired increases and hence the conduction angle of the SCR's decreases. The decreased conduction angle reduces the power to the load, thus offsetting the increase of power to the load otherwise due to the increase in line voltage. By proper choice of the voltage divider ratio of R_3 and R_4 it is possible to obtain perfect compensation of the circuit for small changes in line voltage.



Simple SCR/UJT Phase Control Circuit Modified for Voltage Regulation
Figure 8.3 (A)

Component values same as in Figure 8.2(A) except that

R_1 — 470 ohms
R_2 — 30K-40K
R_4 — 270 ohms



Voltage Waveforms of SCR/UJT Phase Control Circuit with High and Low Line Voltage
Figure 8.3 (B)

The circuit shown was adjusted to give optimum regulation at 25 volts rms output and 115 volts input, and the component values listed were found to be suitable. For a change in line voltage from 115 volts to 100 volts the change in output voltage was less than 0.1 volt with any output voltage setting from 10 volts to 30 volts.

If regulation is desired over a wide range of output voltage, a ganged pot can be used with R_2, and the value of R_4 can be changed with the position of the potentiometer. The value of R_1 is chosen to achieve the desired temperature compensation in the ordinary manner. There is some interaction between the adjustment of R_4 for voltage compensation and the adjustment of R_1 for temperature compensation so several successive adjustments may be required.

8.3 FULL WAVE PHASE CONTROLLED AC SWITCH USING SINGLE SCR

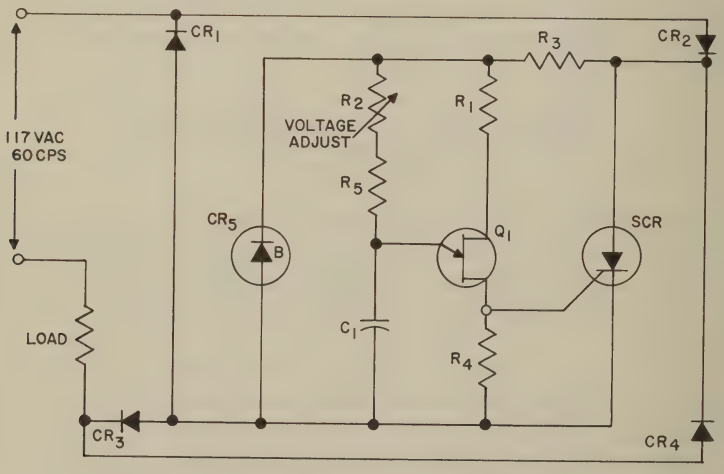
The circuit shown in Figure 8.4 is a variation of the AC phase controlled switch described in Figure 8.2. It consists of a single phase full wave bridge

rectifier circuit in series with the load. The DC leg of the bridge contains a single SCR. The load sees full wave phase controlled power as in the circuit of Figure 8.2.

In lower ratings the circuit offers economic advantages. It improves the current duty cycle on the SCR, and requires less critical overcurrent protection for the SCR. Very little safety factor in SCR voltage rating is necessary since practically no PRV can be applied to the SCR. Efficiency of this circuit is somewhat lower than the back-to-back arrangement of SCR's in Figure 8.2 because of the added voltage drop in the diode rectifiers.

The SCR in this circuit is subjected to a single phase full wave rectified sine wave voltage by the action of the diodes. As long as negligible inductance exists in the DC section of the single phase bridge, current must reach essentially zero each half cycle and must be discontinuous because of the three forward biased diode drops in series at any instant across the line (two diodes and the SCR). On a 60 cps 117 volt system, the current is restrained to a sufficiently low value each half-cycle to allow the SCR to regain its forward blocking state. It is of some importance that relatively slow recovery diode rectifiers be used in the bridge. The turn-off time of the SCR should be in the order of the reverse recovery time of the diodes. The circuit has, for example, been successfully operated at 400 cps at maximum allowable operating junction temperature using standard G-E medium current alloy junction diode rectifiers.

The components listed in Figure 8.4 make this particular circuit capable of controlling up to 150 watts continuously on a 117 volt line.



R_1	390Ω, 1/2 WATT	C_1	0.1 MFD
R_2	100K, LINEAR POT	SCR	G-E 2N1774A
R_3	3.3K, 5 WATT	CR_1 THRU CR_4	G-E IN1695
R_4	47Ω, 1/2 WATT	CR_5	IN1527, 20 VOLTS 1 WATT BREAK-DOWN DIODE
R_5	3.3K, 1/2 WATT		
Q_1	G.E. 2N1671A		

150 Watt Voltage Controller
Figure 8.4

The circuit of Figure 8.4 has a particular advantage when working into the primary of a transformer. This is sometimes necessary in order to control voltage or current levels out of range of conventional SCR's. Since two SCR's will seldom if ever have exactly the same holding current under operating conditions, there is a good possibility of firing only one SCR at very low current levels in the parallel-inverse circuit of Figure 8.2. The resulting DC load component can easily lead to transformer core saturation unless a large amount of bleeder resistance is used. The circuit of Figure 8.4 eliminates unsymmetrical firing since only one SCR is involved. Some amount of bleeder resistance may still be advantageous in order to operate into a highly inductive load at very low current levels.

8.4 TYPICAL PHASE CONTROLLED CIRCUITS FOR AC LOADS

In the following examples the basic AC switch is used to satisfy functional requirements, such as temperature control, motor control, etc. For very simple SCR circuits the reader is referred to Chapter 4 in which simple resistor-capacitor-diode firing circuits control AC power. For regulated systems reference is made to Chapter 10.

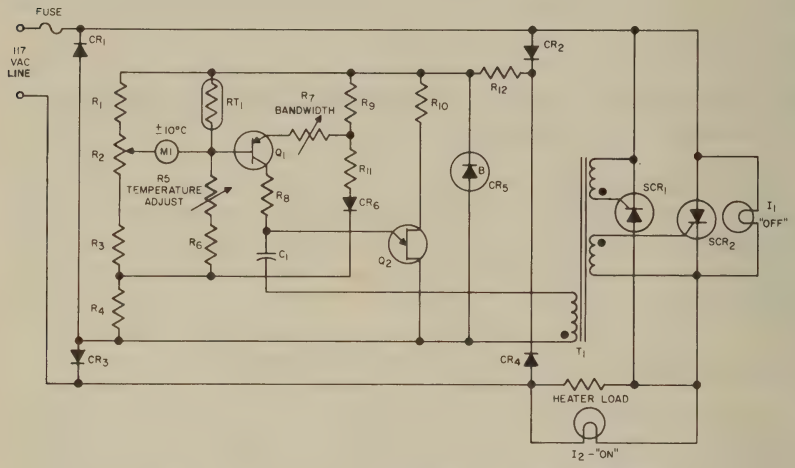
8.4.1 Temperature Control Circuits

A variation of Figure 8.2 as shown in Figure 8.5 has been used successfully to provide precise static control of temperature in such equipments as electric ovens, furnaces, and surface units. With 2N681's operating as phase-controlled switches, this controller will regulate up to 4KW of heaters steplessly, maintaining the temperature at the sensing element within less than one degree variation anywhere within the temperature range from ambient to 300°C. It lends itself very nicely to programmed or manual process control and its main features are high reliability, low maintenance, and the absence of temperature cycling in the unit being controlled.

The UJT timing capacitor C_1 is charged by a series transistor Q_1. The base signal on this transistor is derived across the bridge formed by R_5 and R_6, R_9, R_{11}, and thermistor RT_1. If the temperature at the thermistor drops below the preset value, the resistance of RT_1 increases. The voltage at the base of Q_1 decreases, causing more base and collector current to flow. This will charge C_1 up more quickly, and UJT Q_2 will fire the SCR's earlier each cycle. More power will be applied to the heaters and the temperature will return to the preset value. The reverse action will take place if the temperature attempts to rise above the preset value. Waveshapes are similar to those shown in Figure 7.6.

Meter M_1 provides a visual indication of temperature deviation from the preset value. By means of R_2, it is adjusted to center scale when the temperature is the correct value. Lamps I_1 and I_2 indicate by their relative intensity the proportion of the voltage cycle being applied to the heating elements. CR_6 is inserted in the sensing bridge to temperature compensate the variation of base to emitter voltage of Q_1. Thermistor RT_1 in Figure 8.5 is designed for temperature control around 150°C. For other temperature ranges, RT_1 should

be selected to have approximately the same resistance as R_5 at the low end of the temperature range to be controlled. Series/parallel arrangements of thermistors with suitable switching means can be used to cover these other temperature ranges at the wish of the operator. The maximum temperature at which a specific thermistor type or combination should be used is limited by the internal dissipation of the thermistors. This will introduce a sensing error if the themistor temperature becomes higher than its surrounding ambient due to self-heating.

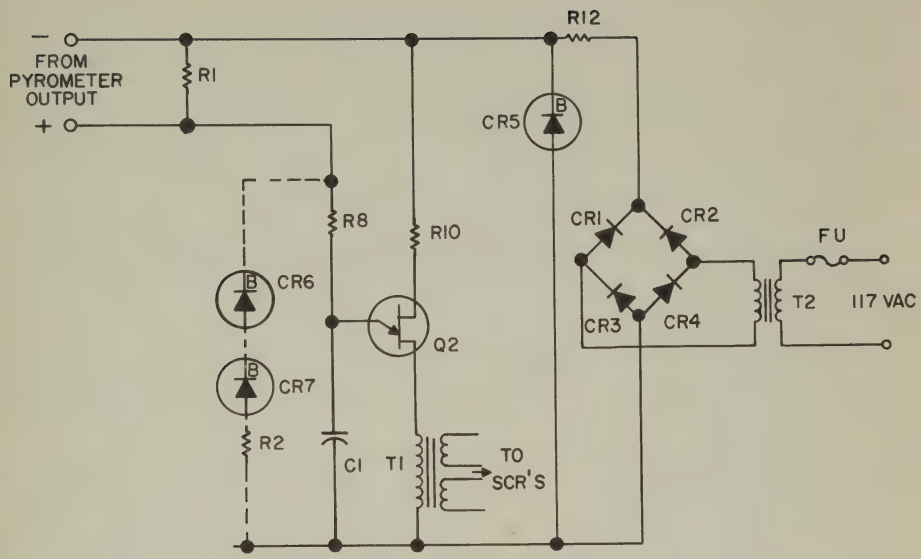


R_1	82K 1/4 WATT	R_8	2 2K 1/4 WATT	CR_5	IN1527
R_2	25K VARIABLE	R_9, R_{11}	300 Ω --- WIRE WOUND	CR_6	G-E IN91
R_3	82K 1/4W	R_{10}	470 Ω 1 W	Q_1	G-E 2N525
R_4	1K 2W	R_{12}	1500 Ω 10W	Q_2	G-E 2N1671A
R_5	10K HELIPOT 10 TURN	C_1	.25 μf 600V	T_1	PE 2231, UTCH51 OR EQUIVALENT
R_6	500 Ω, 1 WATT	SCR_1, SCR_2	G-E 2N686	M_1	METER 20 μa MOVEMENT
R_7	500 Ω VARIABLE	CR_1, CR_2, CR_3, CR_4	G-E IN1695	I_1, I_2	LAMP 115V 6W
				RT_1	THERMISTOR VECO 51A1 OR FENWAL GA55P8

Temperature Controller
Figure 8.5

The emitter circuit of the UJT in Figure 8.5 can easily be modified to take its input signal from a variety of sources. For example, when using a commercially available pyrometer delivering about a zero to 100 volt swing when calling for zero to full output of the furnace heating element, the firing circuit of Figure 8.6 can be used.* Zener diode CR_5 and resistor R_1 determine the threshold characteristic of the circuit; R_1 also determines the maximum input voltage. Zener diodes CR_6 and CR_7 and resistor R_2 are shown dotted to indicate that they are optional for improving linearity and the transfer characteristic for large values of output. Conversely, by omitting this network and making R_8 adjustable the circuit can be linearized over the particular control range of interest.

*The circuits in Figures 8.5 and 8.6 were suggested by R. Senft of the General Electric Co., Auburn, N. Y.



Q2		GE 2N1671A
CR1, CR2, CR3, CR4		GE IN1695
CR6, CR7,		IN1517 (25V/1/4W)
CR5		IN1528 (25V/1W)
R1	8.2K/2W	
R2	2.2 K/1/2W	
R8	82 K/1/2W	
R10	470 Ω/1/2W	
R12	7.5 K/5 W	
FU	FUSE=1 AMP	
C1	.25 MFD/600V	
T1	PULSE TRANSFORMER PE2231, UTC H51, OR EQUIVALENT	
T2	ISOLATION TRANSFORMER 115 V/10 VA	

UJT Firing Circuit for Temperature Controller Operating from a Pyrometer
Figure 8.6

8.4.2 Lamp Dimming

Figure 8.7 illustrates the basic circuit of Figure 8.2 in a 10 kw lamp dimmer.

The circuit gives stepless control of a 10KW incandescent lamp load.[2] Due to the positive temperature coefficient of incandescent filament lamps, this type of circuit must handle very high inrush currents when starting a cold lamp. In Figure 8.7 a peak current limit is used to reduce the inrush current to the short term ratings of the SCR's. Phase control is achieved by series transistor (Q_1) control of a UJT (Q_3) which was discussed in Chapter 4.

The output of the circuit is controlled by potentiometer R_1 which determines the base drive on transistor Q_1. Overriding control of the output is achieved by the current limit circuit of Q_2. Current transformer CT_1 supplies a signal to drive Q_2 in accordance with the current in the load circuit. Beyond a level set by current limit potentiometer R_2, transistor Q_2 will conduct. This effectively brings the potential of the base of transistor Q_1 closer to its emitter and reduces its collector current. This action phases back the SCR and reduces the voltage applied to the load. The time constants of the control circuit are selected to give a response of one-half cycle of line frequency.

If the circuit is initially energized with full output called for (arm of R_1 in bottom position), delay capacitor C_3 will cause the firing angle of the SCR's to advance from maximum phase retard to full output over a period of several cycles of line frequency. If the peak current limit setting on one cycle is exceeded slightly during this starting sequence, transistor Q_2 will take over and keep the SCR firing angle retarded until the load resistance approaches its steady-state value.

Potentiometer R_2 is set for the maximum allowable repetitive peak current rating of the SCR's under the particular application conditions. Thus the full capability of the SCR's at maximum rated junction temperature can be employed to bring the load to full output very quickly without the possibility of damage to the SCR's.

A mechanical patch interlock is provided for cases where additional load is plugged into the circuit while already energized. When momentarily closed, this interlock discharges C_3 and re-initiates the starting sequence. With the interlock mounted as an integral part of the plugging arrangement, the delay circuit will be reset every time load is added, ensuring maximum long term reliability by holding recurring peak currents through the SCR's to rated values.

At lower power levels much simpler SCR lamp dimming circuits are given by Figure 8.4 or by some of the simple AC circuits discussed in Chapter 4.

8.5 TYPICAL PHASE CONTROLLED CIRCUITS FOR DC LOADS

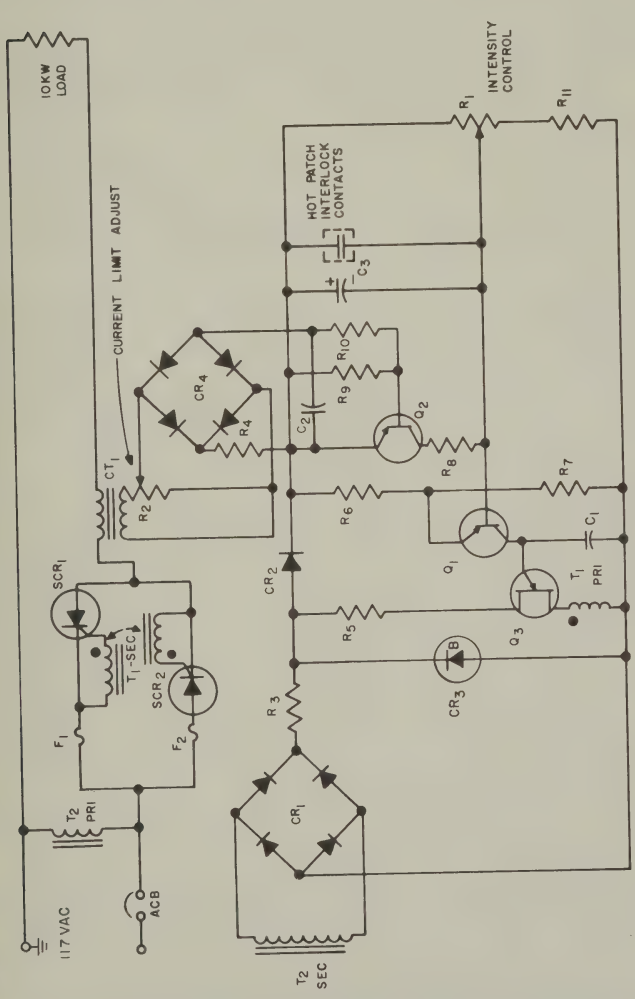
As mentioned earlier, diode rectifiers can be replaced by SCR's in conventional rectifier circuits giving continuous control over a DC load from an AC source. The following examples in the power supply and motor drive area illustrate this.

8.5.1 Phase Controlled DC Supplies

Figure 8.8 illustrates the use of SCR's in a typical single phase centertap phase controlled rectifier. By varying R_7, the DC voltage across the load can be steplessly adjusted from its maximum value down to zero. As in the AC phase controlled switch shown in Figure 8.2, a single UJT (Q_1) is used to develop a gate signal to fire both SCR's on alternate half cycles. Through the rectifying action of CR_1 and CR_2 and the clipping action of CR_3 and R_1, a square wave of voltage with 20 volt amplitude is applied to UJT Q_1. This voltage permits

Q_1 to operate as a relaxation oscillator and to develop a pulse of gate current in the SCR's at a firing angle determined by the time constant of R_6, R_7, and C_1. Whichever of the two SCR's has positive anode voltage at the time the gate pulse occurs will fire, thus applying voltage to the load for the remainder of that half cycle. The firing angle can be adjusted by means of R_7. At 60 cps, the firing angle of this circuit can be varied from approximately 10° to 180° (fully off). Figure 8.9 defines the average load voltage e_o as a function of frequency in cps, emitter capacitor C in farads, emitter resistor R in ohms, and the intrinsic standoff ratio of the UJT.

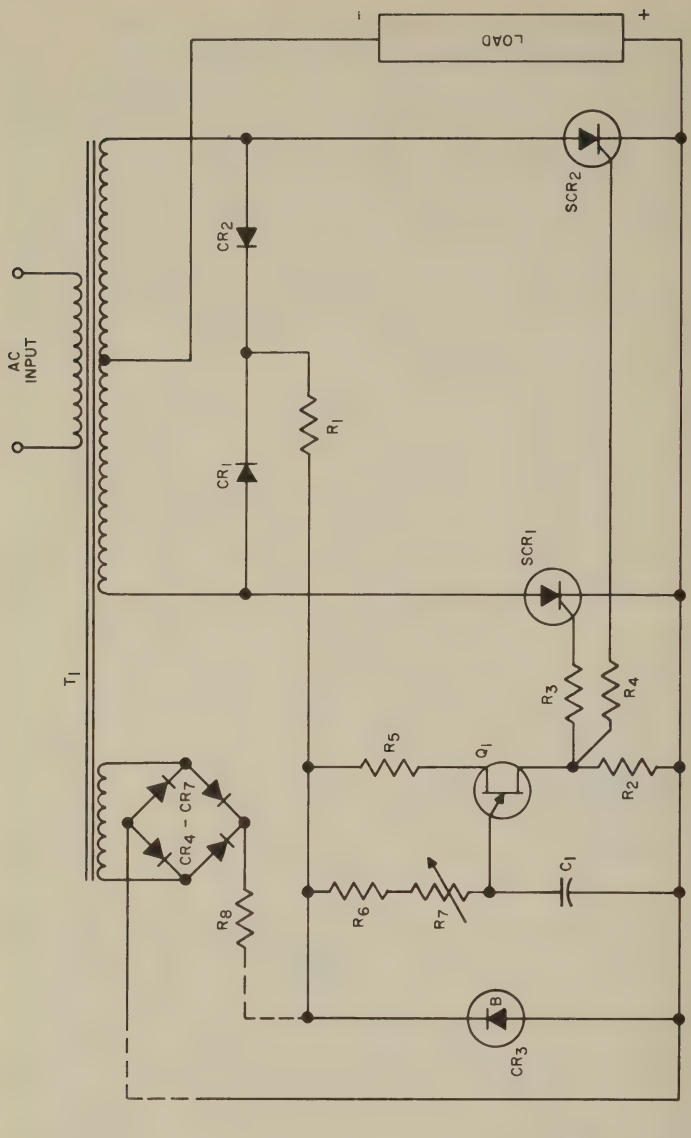
The output voltage e_o is expressed in terms of its ratio to the output voltage at zero firing angle (fully on). This curve can be used to analyze the transfer



R_1 — 1000 OHM POT
R_2 — 500 OHM POT
R_3 — 3300 OHM, 5 WATTS
R_4 — 15 OHM, 1/2 WATT
R_5 — 220 OHM, 1/2 WATT
R_6 — 470 OHM, 1/2 WATT
R_7 — 22K, 1/2 WATT
R_8 — 47 OHM, 1/2 WATT
R_9 — 330 OHM, 1/2 WATT
R_{10}, R_{11} — 10K, 1 WATT
C_1 — 0.22 MFD
C_2 — 1.0 MFD
C_3 — 200 MFD, 20 VOLTS
T_1 — PE 2231, UTC H51, OR EQUIVALENT
T_2 — 117/117 V ISOLATION TRANSFORMER, 50 VA
CT_1 — G-E 258X20 (100:5A)

SCR_1, SCR_2 — G-E 2N1913
Q_1, Q_2 — G-E 2N525
Q_3 — G-E 2N1671A
CR_1, CR_4 — (8) G-E 1N1695
CR_2 — G-E 1N536
CR_3 — 1N1527 BREAKDOWN DIODE

10KW Lamp Dimmer
Figure 8.7



Phase-Controlled DC Power Supply
Figure 8.8

characteristics of any type of single phase full wave rectifier system that works into a resistive load and uses this type of UJT control. The transfer characteristics of UJT firing circuits using series or shunt transistors are described in Chapter 4 and Reference 1.

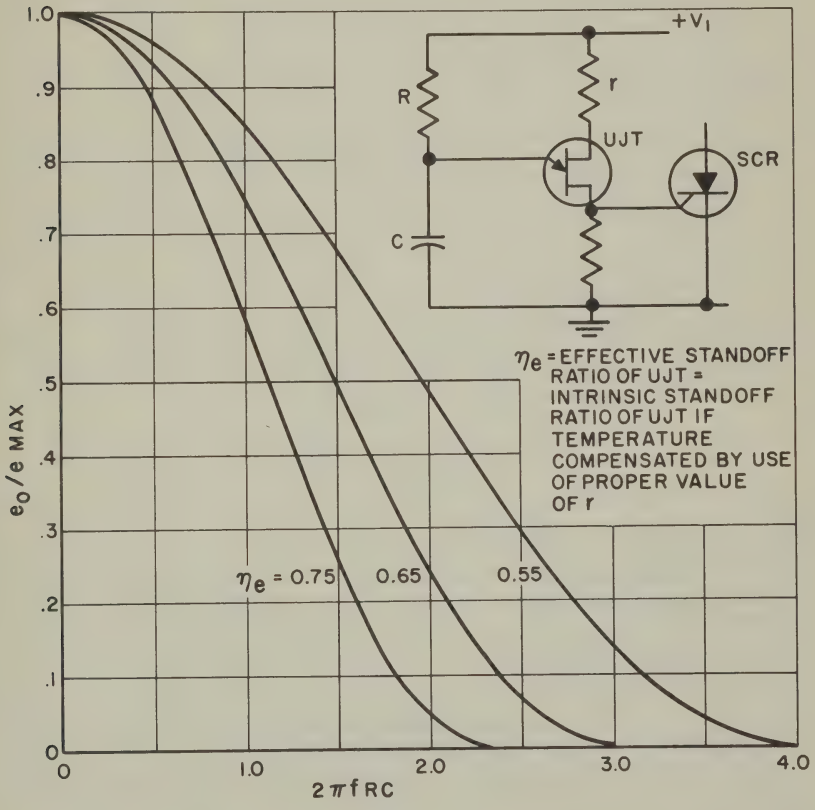
If the secondary voltage applied to the SCR anodes is less than approximately 100 volts RMS, a separate voltage supply should be used for the UJT control. In Figure 8.8 an additional 117 VAC winding on T_1 in conjunction

with a diode bridge CR_4-CR_7 can be substituted for CR_1, CR_2, and R_1 if the main secondary voltage is low. A more steeply rising square wave of voltage with sufficient amplitude is thereby provided for control purposes.

8.5.2 *Full Wave DC Motor Drives*

SCR's are well suited for supplying both armature power and field excitation to DC machines.

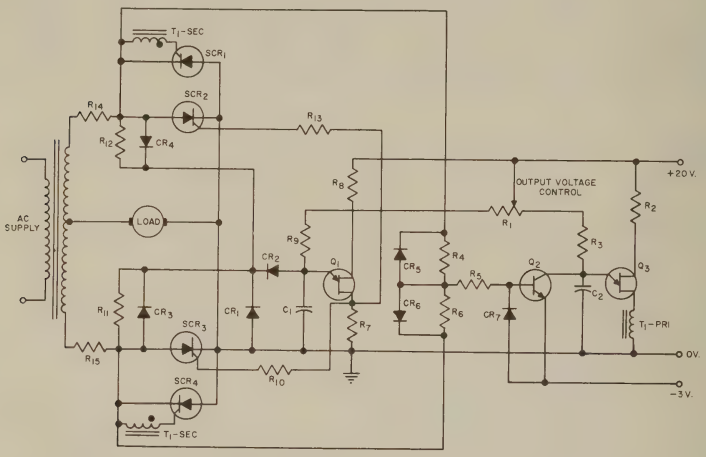
A full wave reversing control or servo as shown in Figure 8.10 can be designed around two SCR's with common cathode (SCR_2, SCR_3) and two SCR's with common anodes (SCR_1, SCR_4). In this circuit, SCR_2 and SCR_3 are fired by UJT Q_1. Since SCR_1 and SCR_4 have electrically isolated cathodes, the gate signal pulse generated by UJT Q_3 is coupled to the SCR gates by isolated secondary windings on transformer T_1. Transistor clamp Q_2 synchronizes the firing of Q_3 to the anode voltages across SCR_1 and SCR_4.



Transfer Characteristics of Unijunction Controlled Single Phase Rectifier Circuits (Half and Full Wave Rectifiers with Resistive Load)
Figure 8.9

Potentiometer R_1 can be used to regulate the polarity and the magnitude of output voltage across the load. With R_1 at its center position, neither UJT fires and no output voltage appears across the load. As the arm of R_1 is moved to the left, Q_1 and its associated SCR's begin to fire. At the extreme left hand position of R_1, full output voltage appears across the load. As the arm of R_1 is moved to the right of center, similar action occurs except the polarity across the load is reversed.

If the load is a DC motor, plugging action occurs if R_1 is reversed abruptly. R_{14} and R_{15} are used in series with each end of the transformer to limit fault current in the event a voltage transient should fire an odd- or even-numbered SCR pair simultaneously.



R_1 — 100K LINEAR POT
R_2, R_8 — 470 OHMS, 1/2 WATT
R_3, R_9 — 2700 OHMS, 1/2 WATT
R_4, R_6 — 10K, 2 WATTS
R_5 — 4700 OHMS, 1/2 WATT
R_7 — 47 OHMS, 1/2 WATT

R_{10}, R_{13} — 22 OHMS, 1/2 WATT
R_{11}, R_{12} — 2200 OHMS, 2 WATTS
R_{14}, R_{15} — 2 OHMS, 500 WATTS OR LESS, DEPENDING ON RATING OF LOAD
C_1, C_2 — 0.2 MFD
$SCR_1, SCR_2, SCR_3, SCR_4$ — G-E SCR (VOLTAGE RATING DEPENDENT ON SECONDARY TRANSFORMER VOLTAGE)

$CR_1, CR_2, CR_3, CR_4, CR_5, CR_6$ — G-E IN1695
CR_7 — G-E IN1692
Q_1, Q_3 — G-E 2N1671A
Q_2 — G-E 2N335
T_1 — PE2231, UTC H51, OR EQUIVALENT

Full Wave Reversing Drive
Figure 8.10

8.5.3 Half Wave DC Motor Drives

For adjustable speed operation of lower rated motors half-wave control has great economic advantages at quite adequate performance levels in many cases. The machines may have shunt fields, series fields (universal motors), or be of the permanent magnet type.

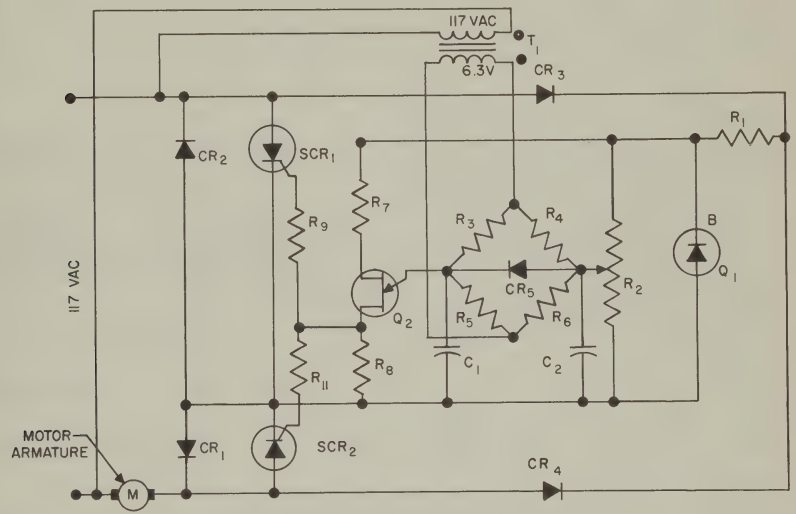
The drive discussed in connection with Figure 8.11 is illustrative of permanent magnet motors or separately excited shunt motors. However, one SCR is normally all that is required in the armature circuit for one direction of rotation. This feature is illustrated more fully in the universal motor speed control circuit shown in Figure 8.13.

8.5.3.1 Phase Sensitive Servo Drive

A phase sensitive servo drive supplying reversible half wave power to the armature of a small permanent magnet or shunt motor is shown in Figure 8.11.

The power circuit consists of two half-wave circuits back-to-back (SCR_1, CR_1; and SCR_2, CR_2) fired by unijunction transistor, Q_2, on either the positive or negative half cycle of line voltage depending on the direction of unbalance of the reference bridge resulting from the value of the sensing element R_6. R_6 can be a photoresistor, as in Figure 8.11, a thermistor, a potentiometer, or an output from a control amplifier.

The potentiometer R_2 is set so that the DC bias on the emitter of unijunction transistor, Q_2, is slightly below the peak point voltage at which Q_2 fires by an amount dependent upon the deadband desired. With R_6 equal to R_5 the bridge will be balanced, UJT (Q_2) will not fire and no output voltage appears across the load. If R_6 is increased thus unbalancing the bridge, an AC signal will appear at the emitter of the UJT causing the emitter to be biased above the firing voltage during one half cycle of the AC. Q_2 will fire and, assuming that SCR_2 is forward biased, SCR_2 will fire. When R_6 is decreased, similar action occurs except that SCR_1 will fire, reversing the polarity across the load.



R_1 — 3.3K 2 WATT
R_3, R_4 — 2.2K
R_5 — 6.8K
R_6 — PHOTO RESISTOR FERROXCUBE #B8731.03 OR 50K POTENTIOMETER
R_2 — 2K POT

R_7 — 510 Ω
R_8, R_9, R_{11} — 47
C_1 — .01 uf
C_2 — 0.2 uf
Q_1 — 20 VOLT 1 WATT ZENER

Q_2 — GE2N1671A
CR_1–CR_5 — GE IN645
SCR_1, SCR_2 — GE 2N1932
T_1 — UTC H-131 OR EQUIVALENT
ALL RESISTORS ARE 1/2 WATT EXCEPT AS NOTED.

Phase Sensitive Servo Drive
Figure 8.11

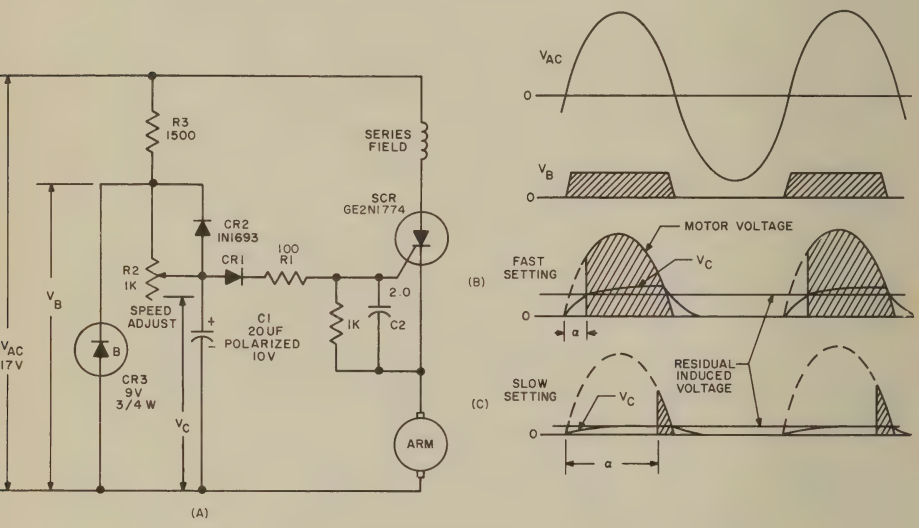
8.5.3.2 Universal Motor Adjustable Speed Drive

The universal motor has found wide use in many applications which require high torque during starting and at low speeds. When used in a half-wave circuit, the series or universal motor has an added advantage over the shunt motor since its output torque is approximately proportional to the square of

the RMS value of armature current rather than the first power of the average value as is the case with the fixed field shunt motor.

Speed control is achieved by varying the conduction angle of the SCR placed in series with the armature and field of the universal (AC-DC) motor. When conduction is initiated at a point determined by the motor speed, a regulated speed control results. Two methods of achieving this type of operation rely either on the residual field induced voltage of the motor for a speed signal, or on excitation of the series field during the "off" half-cycle for developing a similar speed sensitive signal.

The circuit of Figure 8.12(A) shows a speed control which makes use of the motor residual field to induce a counter emf in the armature proportional to speed. This voltage is employed as the speed feedback signal. This circuit is suggested particularly for applications requiring stable operation at low speeds and in the presence of nominal line voltage variations.



Universal Motor Adjustable Speed Drive
Figure 8.12

During the negative half cycle of the supply voltage capacitor C_1, which may be of the polarized electrolytic type, is discharged to zero. During the positive half cycle C_1 charges from a constant potential (zener voltage of CR_3) at an exponential rate dependent on the time constant R_2C_1. If the motor armature is standing still, no voltage is induced in it by the residual field, and gate current to the SCR flows as soon as v_c exceeds the forward voltage drop of CR_1 and the gate drop of SCR. This will fire SCR early in the cycle, providing ample energy to accelerate the motor. As the motor approaches its preset speed, the residual induced voltage in the armature builds up. This voltage is positive on the top terminal of the armature and bucks the flow of gate current from capacitor C_1 until v_c exceeds the armature voltage. This higher voltage requirement on C_1 retards the firing angle and allows the motor to cease accelerating.

Once the motor has reached operating speed, the residual induced voltage provides automatic speed regulating action. For instance, if a heavy load starts to pull down the motor speed, the induced voltage decreases, and SCR therefore fires earlier in the cycle. The additional energy thus furnished to the motor supplies the necessary torque to handle the increased load. Conversely, a light load with its tendency to increase speed raises the motor residual induced voltage, retarding the firing angle and reducing voltage on the motor.

R_2 adjusts the desired speed by controlling the charging rate of capacitor C_1. The waveform of voltage, v_c, on capacitor C_1 is shown in Figures 8.12(B) and 8.12(C). When R_2 is adjusted to a low value, v_c builds up fast and fires SCR early in the cycle. This high speed setting is depicted by the v_c waveform in Figure 8.13(B). When R_2 is set to a large value, v_c builds up slowly so that firing occurs late in the cycle as in Figure 8.13(C) and the motor speed is therefore low.

Not all types and makes of motors perform satisfactorily in the circuit of Figure 8.13(A) because of the varying degree of their residual induced voltage. Motors with low hysteresis iron tend to have a low residual induced voltage and therefore do not have ample feedback voltage for satisfactory operation of the circuit. Reference 5 discusses the motor characteristic requirements of this and other universal motor speed controls.

While the performance achieved by this circuit is entirely adequate for a majority of universal motor drive applications, a higher degree of speed regulation can be achieved by more sophisticated types of feedback and firing circuitry. Feedback gain and pulsed types of gate signals such as developed by unijunction transistors provide improved regulation and stability over wide speed ranges with little or no need for special calibrating adjustments for individual SCR characteristics. These more complex circuits also eliminate the effects of temperature on the SCR firing characteristics and therefore on the speed regulation also.

8.6 POLYPHASE SCR CIRCUITS

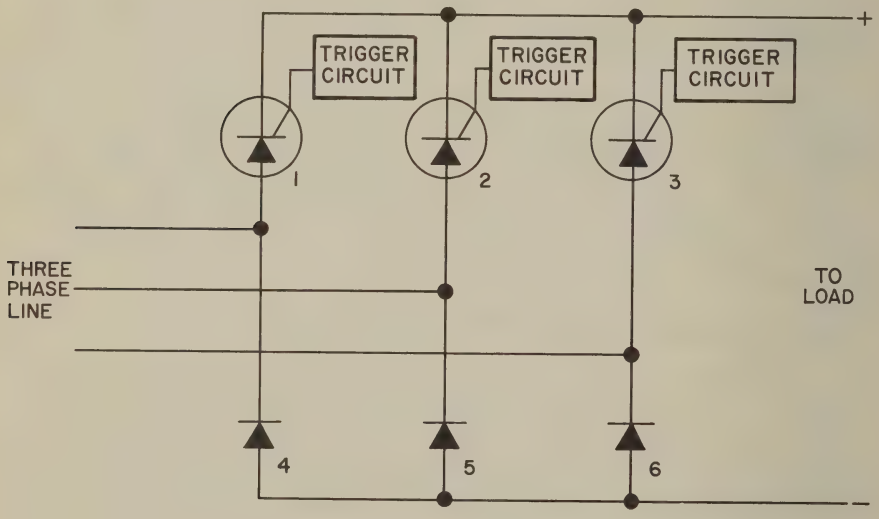
The use of controlled rectifiers is by no means limited to single phase AC circuits. They may be used in polyphase circuits just as conventional two element semiconductor rectifiers. Regardless of the particular circuit configuration the two basic requirements that must be met are the supplying of a trigger turn-on signal at the appropriate time and provision in the circuit external to the controlled rectifier for turn-off.

With regard to turn-off the reversal of the line voltage across the device in common rectifier circuit configurations will return the controlled rectifier to a forward blocking state; this is often referred to as line commutation. On commutating the rectifier is subjected to reverse voltage which facilitates the turn-off process. For this reason, common AC rectifier circuits do not impose unusual turn-off requirements on the controlled rectifier as do certain types of inverter or DC chopper circuits in which forward voltage is reapplied to the controlled rectifier immediately following turn-off. However, depending on the amount of phase retard the controlled rectifier and its associated rectifiers may be sub-

jected to full peak reverse blocking voltage immediately after having conducted full rated current. This type of service is conducive to the generation of recovery voltage transients. Particularly, in cases where SCR's are used in series in a leg of such a circuit, steps must be taken to force proper sharing of these transients between all the cells of the leg. This is discussed more fully in Chapter 6.

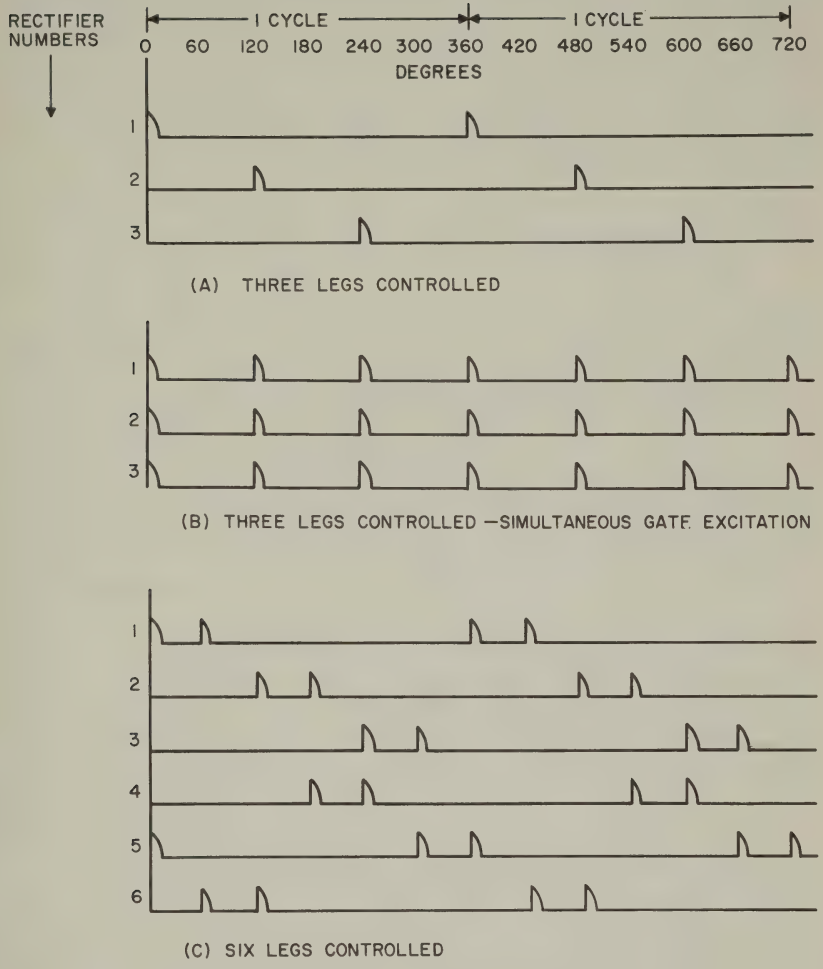
The question of utilizing controlled rectifiers in polyphase circuits involves providing appropriately timed triggering signals in accordance with the type of circuit used and the degree of phase control required. For example, the circuit of Figure 8.13 shows the popular three phase bridge circuit in which the forward legs are controlled and the back legs consist of uncontrolled conventional two element rectifiers. This circuit will give full continuous control from zero to 100% of its DC output when triggering signals capable of being phase shifted over 180 electrical degrees are supplied as shown in Figure 8.14(A).

The circuit discussed in Section 8.6.3 will provide such triggering signals. If triggering signals are supplied as shown in Figure 8.15(B) such that they can be phase-shifted over 120 electrical degrees, the circuit will deliver full control from about 25% to 100% of full output power to the load. A circuit to do this is discussed in Section 8.6.2.



Three Phase Bridge Circuit With Three Controlled Legs Figure 8.13

In some special cases it is desirable to control all six elements of the three phase bridge circuit. Regenerative braking of a DC machine where either field or armature reversing is provided is an example of such a case. For this case, triggering signals capable of being phase shifted over 120 electrical degrees must be supplied as shown in Figure 8.14(C).

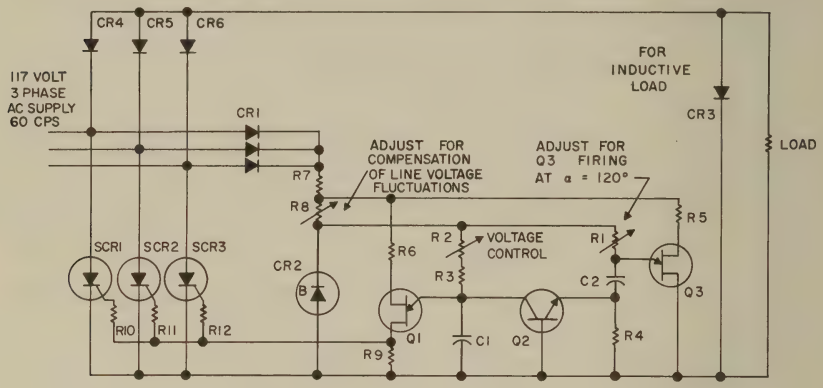


Triggering Pulses for Three Phase Bridge Circuit
Figure 8.14

8.6.1 Simple Three Phase Firing Circuit (25% To 100% Control)

This section describes a simple three-transistor SCR firing circuit that provides stepless control of the DC output voltage from a three-phase bridge between 25% and 100% of maximum output voltage, and also full interruption of output voltage. Means are incorporated to provide automatic compensation for line voltage fluctuations and for phase unbalance without closed loop feedback.

This circuitry is readily applicable wherever stepless control is not required over the full range from zero to 100% of the maximum DC output voltage. Its main features are its simplicity, low cost, compactness, and reliability. Its inherent characteristics provide symmetrical output in all three phases without the need for special matching and adjustment of individual circuits, and the circuit is insensitive to power factor or phase reversal. It lends itself readily to electrical feedback techniques and does not require a separate control voltage supply. No magnetic components are needed.



CR1 — (3) G-E IN1695
CR2 — 20 VOLT, 1 WATT ZENER DIODE, IN1527
CR3, CR4, CR5, CR6 — AS REQUIRED FOR LOAD (e.g. IN2156)
SCR1, SCR2, SCR3 — AS REQUIRED FOR LOAD (e.g. GE2N685)
Q1, Q3 — G-E 2N1671A Q2 — G-E 2N635
R1 — 10K POT
R2 — 20K POT
R3 — 470 Ω
R4 — 100 Ω
R5, R6 — 390 Ω
R7 — 3.3K, 2W
R8 — 500 Ω POT, 2W
R9 — 100 Ω
R10, R11, R12 — 25 Ω
C1 — 0.5 MFD
C2 — 1.0 MFD

Simple Three Phase Firing Circuit
Figure 8.15

Figure 8.15 illustrates the complete firing circuit. CR_1 supplies positive line voltage to the control circuit whenever the anode voltage on an SCR swings positive with respect to the positive DC bus. This voltage is clipped at 20 volts by zener regulator CR_2 and supplies a conventional unijunction transistor relaxation oscillator firing circuit of a type described in detail in Chapter 4. R_2 controls the firing angle of Q_1 by regulating the charging rate to capacitor C_1. The pulse of voltage developed across R_9 as unijunction Q_1 discharges C_1 is coupled simultaneously to the gates of all three controlled rectifiers, SCR_1, SCR_2, and SCR_3, through R_{10}, R_{11}, and R_{12}. Whichever SCR has the most positive anode voltage at the instant of the gate pulse starts conduction at that point.

The circuit composed of transistors Q_2 and Q_3 prevents Q_1 from firing at any delay angle greater than 120°. If triggering pulses are retarded beyond 120°, the output voltage rises abruptly to 100% as the following phase is fired

at the beginning of its cycle. Q_3 is an independent unijunction oscillator which initiates its timing cycle at the same instant as Q_1. R_1 is set at a fixed value so that Q_3 fires at an angle slightly less than 120°. Two modes of operation are possible:

1. If Q_1 triggers before retard angle $\delta = 120°$, it fires the SCR whose positive anode voltage is providing the interbase bias for the unijunctions through CR_1. Firing this SCR shorts the control circuit supply voltage. The interbase bias voltage of Q_3 drops to zero, causing Q_3 to fire and discharge C_2 in preparation for the next cycle. This is the mode of operation when Q_1 is controlling the DC output voltage between 25% and 100% of maximum. In this mode, Q_2 and Q_3 have no effect on the functioning of the bridge.
2. If Q_1 is delayed beyond $\delta = 120°$, Q_3 fires, discharging C_2 through the base-emitter junction of Q_2, saturating this device, and discharging C_1 through Q_2. This alternate mode of discharging C_1 does not impose a pulse on the SCR gates, and the DC output voltage is therefore zero in this mode.

Instead of mechanical manipulation of potentiometer R_2 to control the DC output voltage, electrical signals can be used to control the output by inserting a transistor in series with R_2 in the charging path for C_1, or alternately a transistor in shunt with C_1. Both methods are readily useful in conjunction with feedback systems and are described in Chapter 4.

The success of this circuit depends on Q_3 maintaining its firing angle at slightly less than 120°. For this reason, base 2 of unijunction transistor Q_3 is connected through R_5 to a point separated from the clipped and regulated voltage across CR_2 by resistor R_8. This acts to maintain the timing cycle of Q_3 fixed at slightly less than 120° regardless of normal line voltage variations. Without this precaution, a drop in line voltage would make Q_3 fire at a somewhat greater angle than 120° due to the lesser slope on the front of the clipped sine wave voltage being applied to R_1.

R_8 serves another useful purpose. As was discussed in Section 8.2, by connecting base 2 of unijunction transistor Q_1 to the top of R_8, a marked degree of regulation of the DC output voltage is provided for AC line voltage fluctuations. If the line voltage rises, the interbase bias voltage and therefore the peak point emitter voltage on Q_1 rises depending on the setting of R_8. Since the emitter charging circuit through R_2 is connected to the fixed voltage across regulator CR_2, the firing angle is phased back and the output DC voltage is maintained constant. For a decrease in line voltage, this action advances the firing angle to maintain the output constant. This inherent action is instantaneous and does not depend on a change in the actual output voltage to take corrective action. Where unequal phase voltages exist, this circuit also acts to balance the contribution of the individual phases to the DC output voltage, thus reducing the fundamental frequency ripple content in the DC. Since the compensation provided by R_8 is not constant at all firing angles, R_8 should be adjusted for optimum action near the voltage level at which operation will normally take place.

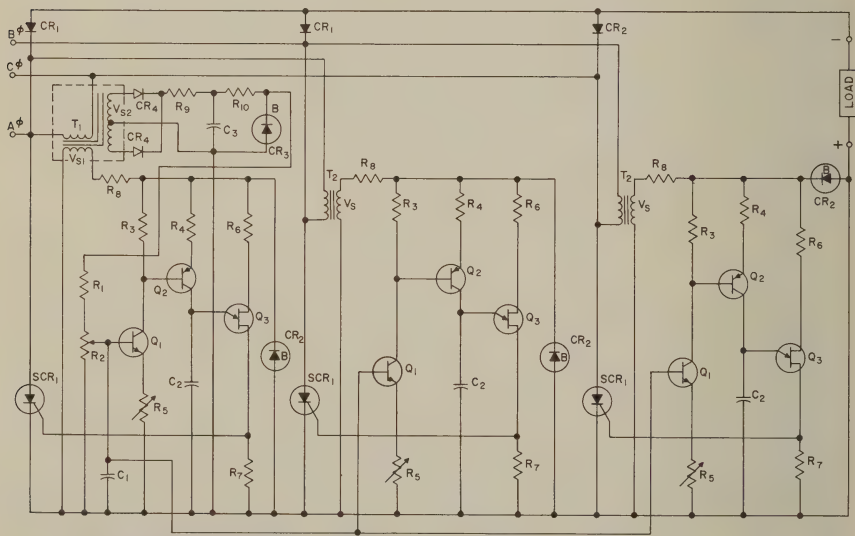
With a three-phase 117 VAC supply, the circuit in Figure 8.15 can be

varied steplessly over DC output voltages from 40 volts to 150 volts DC, a range of 3.75 to 1. It can also be turned off completely. With line voltage variations of ±10%, R_8 can be adjusted to provide essentially constant DC output voltage at both extremes of line voltage. Test data with $R_8 = 350$ ohms, with 10 ohms of load, and with G-E 2N685 cells as the SCR's showed that for a variation in AC line input voltage from 130 volts to 100 volts the DC output varied from 93 volts to 92 volts.

8.6.2 Full Range Three Phase Firing Circuit

The circuit of Figure 8.16 shows the three phase bridge circuit of Figure 8.14 in which three of the six elements are SCR's controlled by their individual UJT firing circuits. Each UJT circuit obtains its supply voltage from the appropriate phase. Transistors Q_2 control the rate of charging unijunction emitter capacitors C_2. Transistors Q_2 are in turn driven by transistors Q_1 that operate from the input signal.

In the circuit of Figure 8.16 the input is represented by the small power supply regulated by zener diode CR_3. The portion of this voltage picked off across capacitor C_1 by means of potentiometer R_2 is the control signal. Since merely the base drive for three transistors must be provided in order to obtain full control over the output power in the load, the circuit lends itself well to low level signal input and closed loop operation.



SCR1 – G.E. CONTROLLED RECTIFIERS SELECTED FOR LOAD REQUIREMENTS
CR1 – G.E. CONVENTIONAL RECTIFIERS OF RATING COMPARABLE TO SCR
CR2 – 20 VOLT ZENER 1 WATT
CR3 – 25 VOLT ZENER 1 WATT
CR4 – G.E. 1N1692
Q1 – G.E. 2N336A
Q2 – G.E. 2N404
Q3 – G.E. 2N1671A
R1 – 2.5K
R2 – 5K / 2 WATT
R3, R4, R5, – 1K / 2 WATT
R6 – 390 Ω
R7 – 47 Ω
R8 – 3.3K / 5 WATT
R9 – 125 Ω
R10 – 125 Ω
C1 – 20 MFD
C2 – 25 MFD
C3 – 100 MFD
T1 – SELECT TO GIVE
a VS1 ≅ 115 VRMS
b VS2 ≅ 20 VRMS (TO CENTER TAP)
T2 – SELECT TO GIVE VS = VS1

Full Range Three Phase Firing Circuit
Figure 8.16

Each transistor acts as an emitter follower and has unity voltage gain. The firing angle is linear with a change in the DC level on the base of transistors Q_2. The conduction angle of the SCR's can be varied from zero to about 170 electrical degrees at 60 cps giving stepless control from zero to about 98% of output voltage. The tracking accuracy of the firing angle can be adjusted by means of potentiometers R_5. At 60 cps input frequency, ± 1 electrical degree tracking can be obtained.

Operation of the circuit of Figure 8.16 over a temperature range at small conduction angles is limited by the I_{CO} stability of the transistors used in the UJT emitter control circuits. For improved temperature stability at low conduction angles additional diode or thermistor temperature compensation is recommended. For an extended temperature range as well as improved temperature stability, silicon PNP transistors can be considered for Q_2.

REFERENCES

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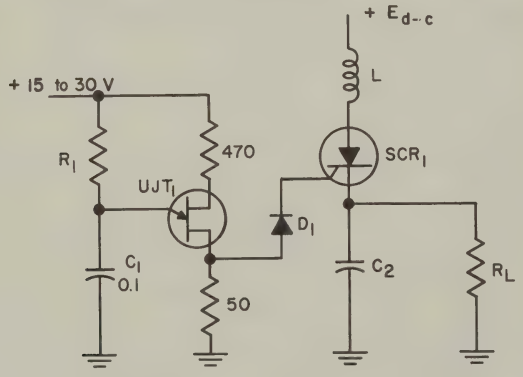
2. "The Silicon Controlled Rectifier in Lamp Dimming and Heating Control Service," E. E. Von Zastrow, Application Note 200.14, available from General Electric Co., Rectifier Components Department, Auburn, N. Y.
3. "Phase-Controlling Kilowatts With Silicon Semiconductors," F. W. Gutzwiller, *Control Engineering*, May, 1959.
4. "Application of Silicon Controlled Rectifiers in a Transistorized High-Response DC Servo System," C. Cantor, AIEE CP 60-864, Summer General Meeting, June, 1960.
5. "Universal Motor Speed Controls," F. W. Gutzwiller, Application Note 200.4, available from General Electric Co., Rectifier Components Department, Auburn, N. Y.

9.1 RESONANT LOAD CAPACITOR COMMUTATED INVERTERS

These types of inverter circuits are characterized by one or more capacitors which are alternately charged and discharged into the load. The load energy is supplied from the resonant reactive elements which also commutate the inverter SCR's. Section 5.4 discussed SCR turn-off with this mode of operation.

9.1.1 Shunt Load

Figure 9.1 shows a simple inverter using one SCR. UJT_1 is in a relaxation oscillator circuit which produces a short pulse across the 50 ohm resistor every time C_1 charges up to the peak point. The time between pulses is approximately R_1C_1 sec. This pulse fires SCR_1 and C_2 starts charging through L. Assuming that R_L is large the current through L, C_2 and SCR_1 tries to oscillate but at the end of the first half cycle when the current reverses, SCR_1 will revert to a blocking state leaving C_2 charged to a voltage greater than the supply voltage. C_2 will discharge through R_L (which might be a step-up transformer) and then another pulse from UJT_1 will cause the cycle to repeat.



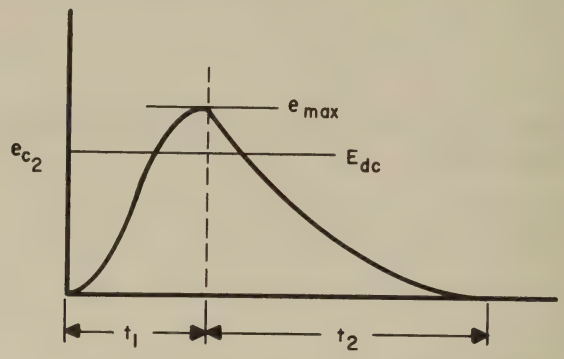
Load Capacitor Commutated Inverter—Shunt Load
Figure 9.1

It is necessary that the L-C_2-R_L circuit be oscillatory in order for the current through SCR_1 to reverse and cause it to turn off. This criterion is theoretically met if:

$$R_L^2 > \frac{L}{4C_2} \tag{9.1}$$

but from a practical standpoint, the minimum R_L should be about four times the value given above.

The waveform across capacitor C_2 is sketched in Figure 9.2.



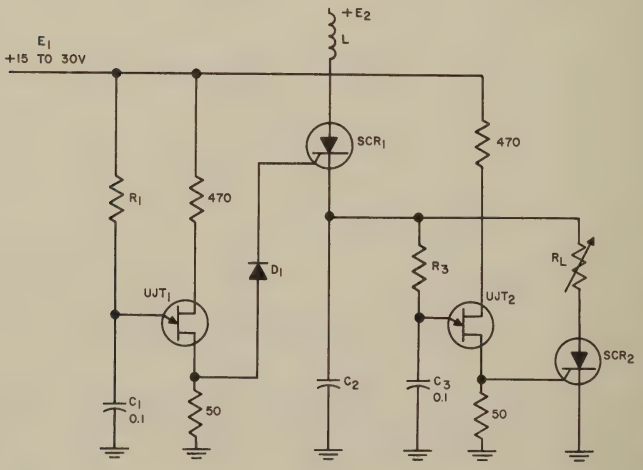
Capacitor Voltage
Figure 9.2

Charging time t_1 is given by $t_1 = \pi/\omega$ where ω, the resonant frequency of the circuit, is:

$$\omega = \sqrt{\frac{1}{LC_2} - \frac{1}{4R_L^2 C_2^2}} \tag{9.2}$$

The voltage, $e_{max.}$, on the capacitor at the end of the charging cycle is:

$$e_{max.} = E_{d-c}\left[1 + \varepsilon^{\frac{-\pi}{2\omega R_L C_2}}\right]\left[1 + \varepsilon^{\frac{-\pi}{2\omega R_L C_2}}\right] \tag{9.3}$$



Load Capacitor Commutated Inverter
—Variable Shunt Load
Figure 9.3

To insure reliable turn-off of SCR_1, $e_{max.}$ should be at least 5 volts above E_{d-c}, that is:

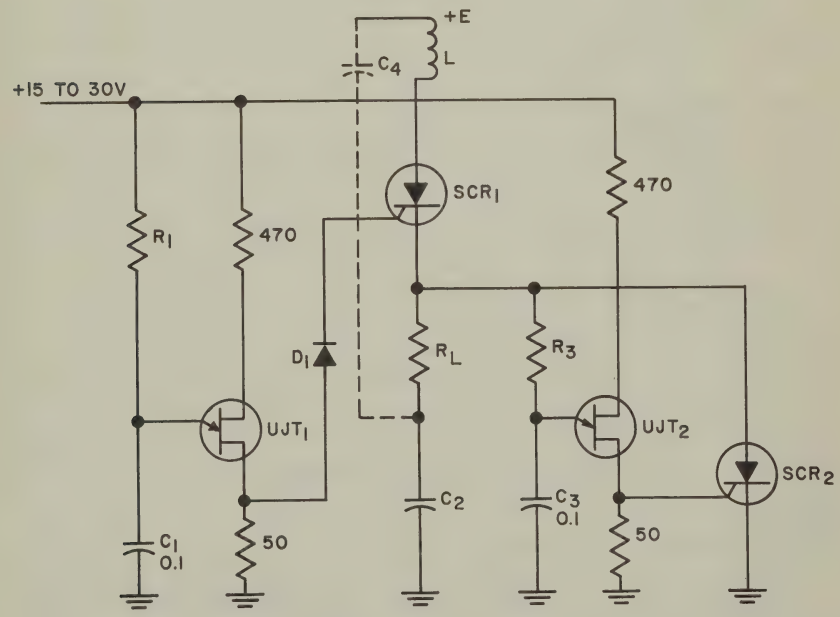
$$E_{d-c}\left(\epsilon^{\frac{-\pi}{2\omega R_L C_2}}\right) > 5 \tag{9.4}$$

The discharge time t_2 is approximately 3 $R_L C_2$. D_1 is necessary to protect the gate from the high reverse voltage existing when C_2 is fully charged and also prevents firing of SCR_1 until C_2 is fully discharged.

When the load consists of a step-up transformer, rectifier and capacitor input filter, the initial effective load resistance may be too small for proper circuit operation. This will result in the SCR remaining fully conducting and no AC voltage will be developed across the load. This problem can be eliminated by using the circuit of Figure 9.3.

In this circuit, C_2 charges to a voltage above E_2 and SCR_1 turns off in the manner previously described but current will not flow into R_L until SCR_2 is fired. The firing of SCR_2 is controlled by UJT_2 and will occur at a time approximately $\eta\ E_1 R_3 C_3 / 2E_2$ seconds after C_2 is fully charged.

This circuit removes all restrictions on the minimum size of the effective load resistance, since R_L is essentially infinity during the charging cycle and has no effect (except fall time) on the circuit performance. To prevent any possibility of both SCR_1 and SCR_2 conducting simultaneously, the $\eta\ E_1 R_3 C_3 / 2E_2$ time should not be shorter than 100 μsec. (η is the stand-off ratio of UJT.)



Load Capacitor Commutated Inverter —Series Load
Figure 9.4

9.1.2 Series Load

The load can be placed in series with the charging circuit as shown in Figure 9.4. With this type of circuit, it is necessary that R_L be smaller than a minimum value given by:

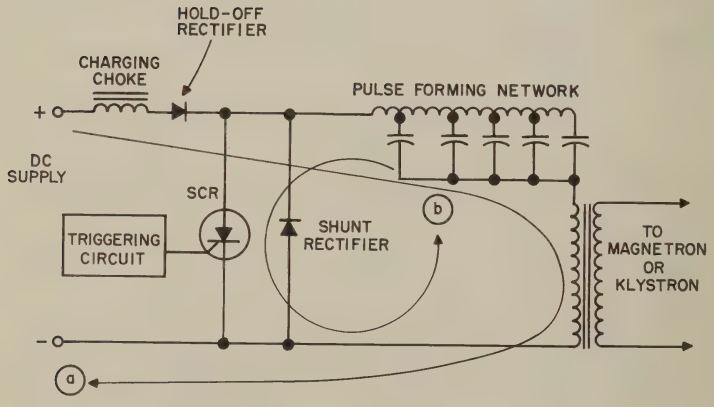
$$R_L^2 < \frac{4L}{C_2} \tag{9.5}$$

The operation of this circuit is essentially the same as for the shunt load type of inverter discussed above, except that current flows through the load in one direction while charging and the reverse direction when discharging. This is an advantage from the standpoint of eliminating a DC component in the load if R_L is a step-up transformer.

The capacitor C_4 is not vital to the circuit operation but is desirable in that it doubles the number of current pulses drawn from the supply. For a given required size of capacitance, it is better to divide it so half is in C_2 and half in C_4. In this manner the current pulses from the supply are half the amplitude (but twice as often) as if all the capacitance were in C_2. The peak voltage to which C_2 charges is given by:

$$e_{max.} = E_{d-c}\left[1 + \varepsilon^{\frac{-\pi R}{2\omega L}}\right] \tag{9.6}$$

$$\text{where } \omega = \sqrt{\frac{1}{LC_2} - \frac{R_L^2}{4L^2}}$$



Typical Line Type Pulse Modulator
Figure 9.5

9.1.3 Pulse Modulators

SCR's have been successfully applied to pulse modulator circuits in radar and beacon systems. One of the most generally used types of circuits is the line type modulator shown in Figure 9.5. When the circuit is initially energized from the DC supply, the capacitors in the pulse forming network (PFN) charge

up to slightly less than twice the DC supply voltage through the charging choke and hold-off rectifier. Current flow during this series resonant charge is indicated by arrow "a". The hold-off rectifier then maintains the voltage on the capacitors in the PFN until SCR is triggered. Discharge of the PFN then takes place through SCR as indicated by arrow "b". The energy stored in the capacitors is delivered in a short flat-top pulse to the transformer and its load. The shunt rectifier may be used to return left-over stored energy in the circuit to the capacitors in the correct polarity and to minimize the commutating duty on the SCR. The existing literature* discusses in detail the design of the PFN and other circuit elements in connection with hydrogen thyratrons as the switching device.

The V_{BO} capability of the SCR in this circuit must be at least twice the DC supply voltage. For high voltage circuits, more than one SCR can be connected in series by use of the techniques discussed in Chapter 6. Because the use of parallel resistors for voltage sharing may lead to excessive power dissipation in modulator circuits with a low duty cycle, zener diodes can be substituted for these resistors. Elements of this type in parallel with the SCR's have negligible leakage until the voltage reaches the knee of their "zener" characteristic. Only enough current passes through the zener diodes to compensate for the unequal leakage characteristics of the SCR's and to maintain approximately equal voltage across each.

In order to minimize jitter, and the delay and rise times of the load pulse, the gate of the SCR should be driven as hard as the maximum SCR gate voltage, current, and power ratings permit. The rise time of the gate pulse should be less than one microsecond, particularly when triggering several series-connected SCR's in order that all SCR's will switch on simultaneously in spite of differences in firing current requirements.

Peak pulse current ratings can be determined by use of Equation 3.17. For very low duty cycles, this equation reduces to a form of the single pulse solution of Equation 3.4. Transient thermal resistance data below 0.001 second can be approximated by extending the r_T curve of the SCR. At 10^{-4} second, the r_T value is approximately 0.32 times the value at 10^{-3} second. At 10^{-5} second, the r_T value is 0.10 times the value at 10^{-3} second.

In switching from blocking to high current conduction very quickly, the SCR experiences very substantial peak switching energy dissipation according to Equation 3.1. The peak current rating must be derated to compensate for this switching heating, as well as heating due to the blocking part of the cycle and the gate pulse. Where switching heating is severe, this power dissipation may be eliminated from the SCR by connecting a small saturable reactor in series with the SCR. Typical reactors have a powdered molybdenum-permalloy core and assume the supply voltage for a microsecond or two while the SCR switches into a very light load. The reactor then saturates and switches the main current. Reactors of this type may help the SCR in commutating the load at the end of the pulse also.

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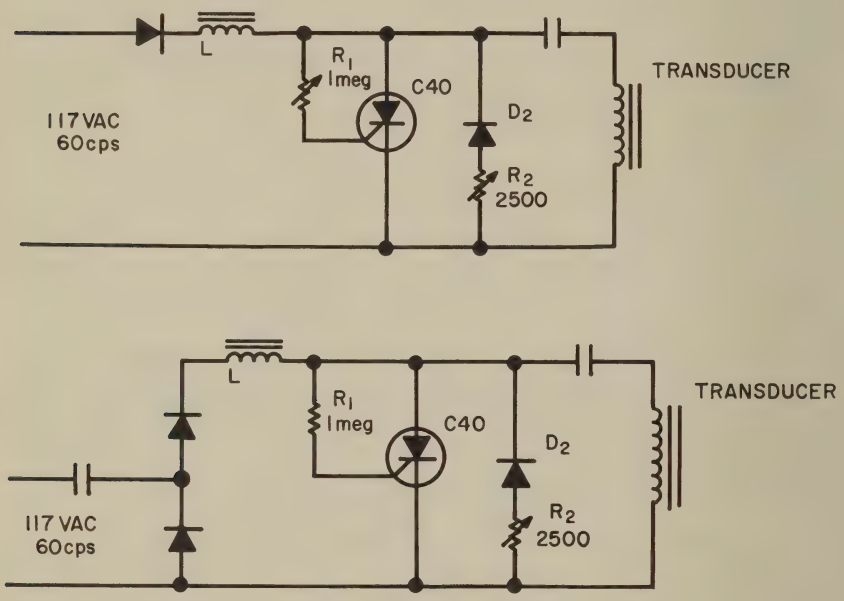
*"Pulse Generators," Glasoe & Lebacqz, McGraw-Hill Book Co., Inc., New York, 1948.

The turn-off characteristics of the SCR may also be a limiting factor if the capacitors in the PFN are recharged too rapidly from the DC supply. If this is the case, an inverter-type SCR, such as the C40 or C55, should be used, and the turn-off time and rate of rise specifications of these SCR's should be met by proper design of the charging choke.

9.1.4 Ultrasonic Oscillator

The reverse time required for the SCR to regain its forward blocking characteristic is a direct function of its junction temperature. With very low average current conduction the junction temperature will rise very little above room temperature and the SCR will turn off with 5 to 7 μsec of reverse time. In the two sketches shown in Figure 9.6 a low Q ultrasonic transducer was driven to frequencies of 20 Kc and above. Either circuit will produce bursts of ultrasonic energy on alternate half-cycles of the power frequency.

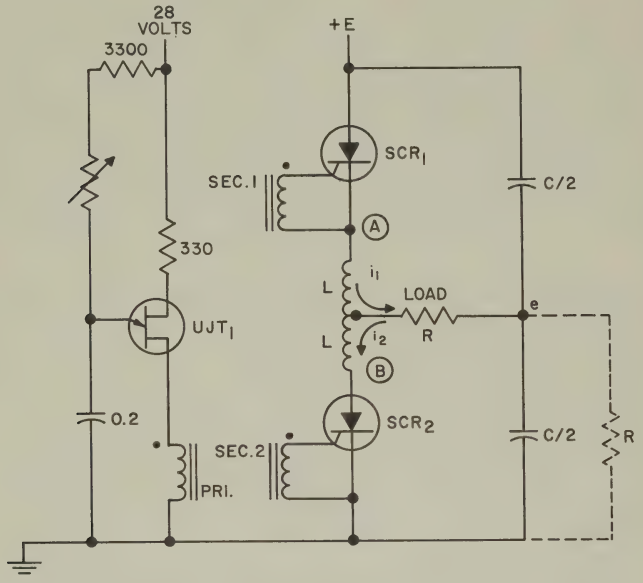


Ultrasonic Oscillator
Figure 9.6

As is usually the case in such simple circuit configurations, component values become more critical. Choke L must maintain the input current at a value slightly less than the circulating current in the tank circuit in order to obtain turn-off. Self-triggering for the SCR gate is derived from the 20 KC appearing across the SCR. Careful adjustment of R_1 will allow the circuit to produce 20 KC energy for approximately 140° of the 60 cycle period. R_2 can be adjusted to optimize turn-off time for the C40 and it in conjunction with D_2 keeps the negative voltage from exceeding the positive swing across the SCR.

9.1.5 Sinewave Inverter Using C. T. Choke

A center-tapped choke can be used to enhance the turn-off of SCR inverters as shown in Figure 9.7.



Sinewave Inverter
Figure 9.7

When SCR_1 turns on, the current i_1 drives point B below ground thus back biasing SCR_2. When SCR_2 is fired, current i_2 drives point A more positive than the supply voltage and back biases SCR_1. This makes it possible to fire both SCR gates simultaneously with a single UJT pulse generator since only the SCR with positive anode to cathode voltage will conduct and the other SCR will be kept back biased by the transformer. The use of a center-tapped choke allows the time delay between charge and discharge to be decreased so that SCR_2 can start conducting the instant that SCR_1 ceases conducting and a sinewave output can be obtained, provided the load resistance is low enough so that the circuit is under-damped, and the load is relatively constant. The operating frequency is:

$$f = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}}$$

With point e initially at ground, UJT_1 will fire SCR_1 and the capacitors will charge to a voltage somewhat less than twice the supply voltage, thus back biasing SCR_1 so it returns to a blocking condition. After a time determined by the RC time constant of the UJT_1 circuit, SCR_2 fires and the capacitors discharge through the resonant circuit until the voltage e is below ground and SCR_2 is reverse biased. When SCR_1 fires again, the current in the resonant circuit is higher since the capacitor voltage is now initially below ground. At the

end of this half cycle, the voltage "e" will therefore be higher than it was at the end of the first half cycle. This action continues until a steady state condition is reached with maximum and minimum voltages as indicated in the following equations:

$$e_{max.} = \frac{E}{1 - \epsilon^{\frac{-\pi R}{2\omega L}}}, \qquad e_{min.} = -\left[\frac{E}{1 - \epsilon^{\frac{\pi R}{2\omega L}}} - E\right] \tag{9.7}$$

As can be seen from the equations, for low values of series resistance, the capacitor voltage will become quite high and for a short-circuited load, the maximum voltage will be determined by the losses in the choke and capacitor. Maximum power output occurs for this type of inverter design when the total capacitance reactance is approximately two times the normal load resistance ($X_c \approx 2R$).

It is possible to take the output power from either a shunt or series resistance as indicated in Figure 9.7. With a series load, the decreasing load resistance increases the peak current flowing in the circuit so that the voltage across the load tends to remain constant. A series load can also be short-circuited indefinitely without causing the inverter to misfire. With a shunt load, a decreasing load resistance will decrease the Q of the circuit and lower the output voltage. This tends to make the power into the shunt load constant under varying load conditions. A short-circuit on a shunt load will cause both SCR's to conduct simultaneously.

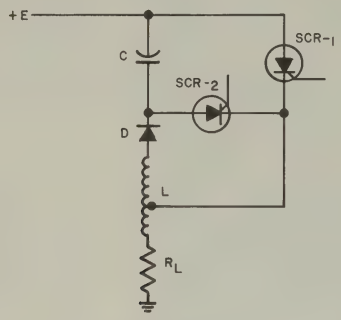
A second mode of operation results with the shunt load when R is low in value so the circuit is overdamped. In this case, current flows continuously in the load after SCR_1 is fired. When SCR_2 is fired, the rapid discharge of the capacitor through the choke turns off SCR_1 by driving its cathode above line potential. This overdamped mode of operation permits current to flow to the load with a pulse width determined by the conduction time of SCR_1. With this mode of operation the circuit is essentially a DC chopper.

9.2 DC CHOPPER CIRCUITS

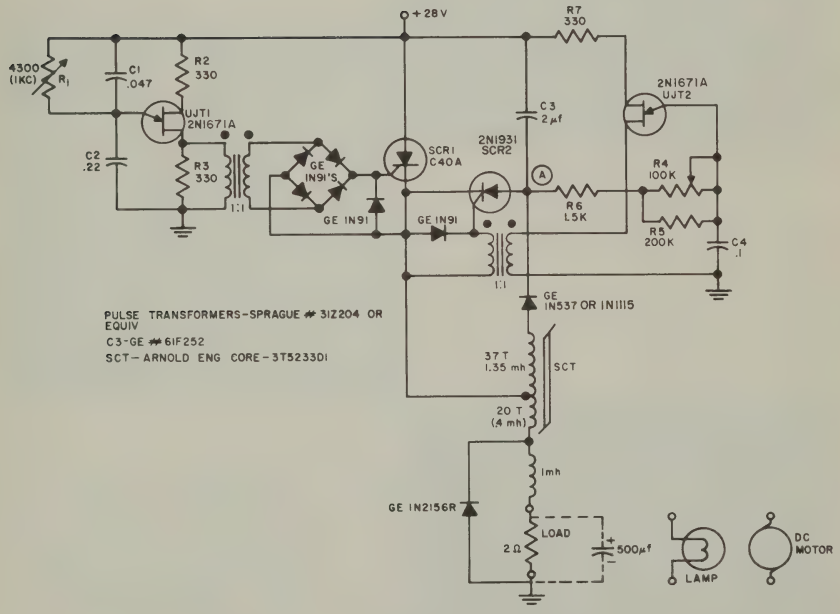
The resonant load capacitor commutated inverters of Section 9.1 have the disadvantage that all the energy that passes into the load must also flow through the inductance and capacitor thus making them physically large. The DC chopper circuit in Figure 9.8 is more satisfactory for many applications since the capacitor only has to store enough energy to turn off the SCR and not carry the full load power. The amount of energy ($1/2\ CE^2$) stored in the commutating capacitor, C, increases as the load current increases due to the auto-transformer action. This is a desirable feature in that the commutating energy requirements increase for higher SCR currents at time of turn-off. This circuit permits the use of a smaller commutating capacitor and operates efficiently with varying load conditions. In Section 5.5, some of the special requirements for the commutating capacitor have been outlined.

In this circuit when SCR_1 is turned on, current flows both into the load and the resonant charging circuit. The capacitor inrush current causes the voltage on capacitor C to rise above the supply voltage. This capacitor charge

is blocked by diode D and SCR_2. The load current will continue to flow until SCR_2 is triggered, at which time the cathode of SCR_1 is driven positive, shutting it off. SCR_2, D, L, and C can be quite small since they only have to carry the turn-off energy. The voltage across the load is a square wave of any duration since the pulse length is determined by the timing of the gate pulses and not the series resonant frequency of L and C. The triggering rate of SCR_1 sets the pulse rate and the triggering time of SCR_2 sets the pulse width. When the tapped inductance is on a saturating core, higher operating frequencies can be achieved since the low saturated inductance permits the commutating capacitor, C, to charge in the shortest time. (Charge time at $A = \pi\sqrt{LC}$ sec.)

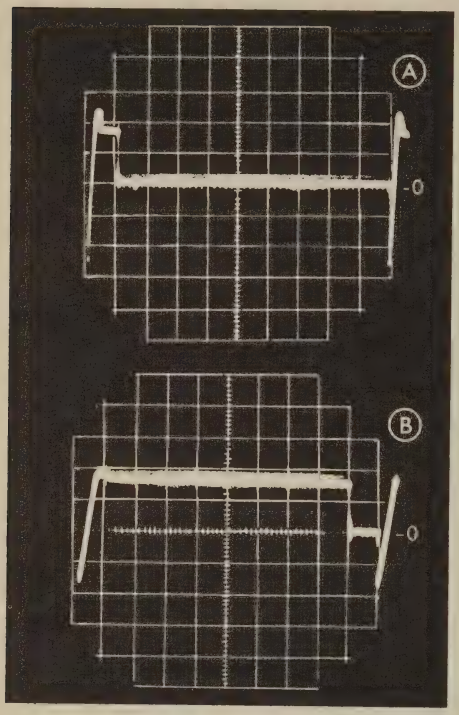


DC Chopper
Figure 9.8



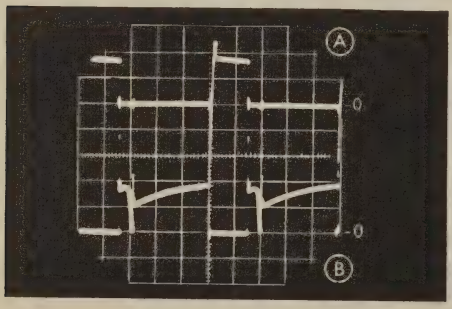
1 Kc DC Chopper
Figure 9.9

Figure 9.9 is a complete DC chopper circuit that operates at 1 Kc chopping frequency (pulse rate), and has a variable pulse width control. The basic operation is the same as Figure 9.8. The variable width control, R_4, gives continuous control of the pulse width from 10% to 90% of the operating period. Figure 9.10 shows the voltage across SCR_1 for both 10% and 90% conduction time.

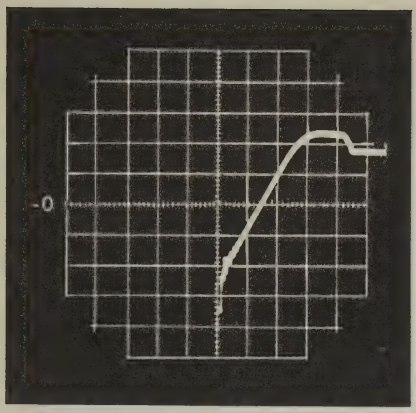


Voltage Across SCR_1
(Vertical Scale—20V/cm)
(Horizontal Scale—100 μsec/cm)
(A) 90% Conduction Time
(B) 10% Conduction Time
Figure 9.10

The following waveforms are with the circuit of Figure 9.9 operating at 70% conduction time for SCR_1. Figure 9.11 shows the voltage and current waveforms for SCR_1. The SCR_1 current rises to 17 amps immediately after turn-on, and is 8.1 amps at the time of turn-off. The value for C_3 is chosen to supply the turn-off energy required with 8.1 amps flowing. C_3 provides a reverse bias across SCR_1 for 15 μsec during the turn-off interval as indicated in Figure 9.12, which is the same as Figure 9.11(A) with the time scale expanded.

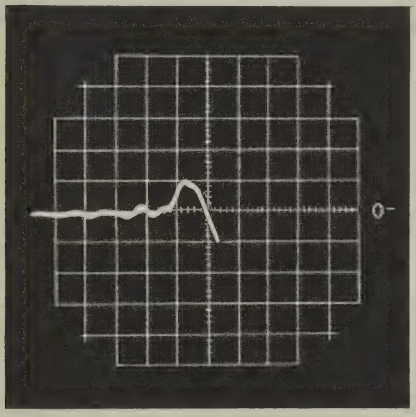


Waveforms for SCR_1
(Horizontal Scale—200 μsec/cm)
(A) Voltage Waveform
(Vertical Scale—20V/cm)
(B) Current Waveform
(Vertical Scale—4.5A/cm)
Figure 9.11



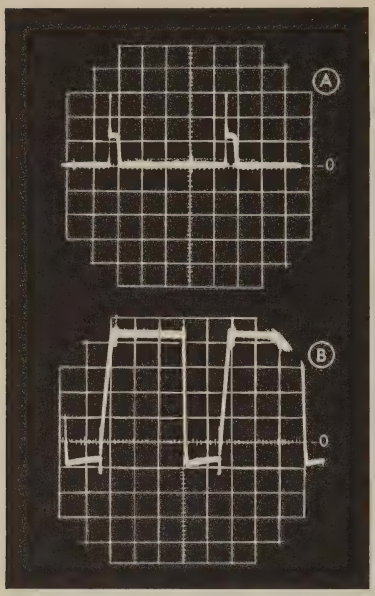
Turn-Off Interval Voltage Waveform for SCR_1 (Vertical Scale—20V/cm) (Horizontal Scale—10 μsec/cm) Figure 9.12

Immediately after SCR_1 is reverse biased with a low impedance external circuit (C_3 and SCR_2 switched on), a reverse current of 4.5 amps flows from SCR_1 as shown in Figure 9.13, which is the same as Figure 9.11(B) with the time scale expanded. The reverse field speeds the recovery time of the two end junctions of SCR_1 by removing the stored charge in about 2 μsec. After recovery of the end junctions, the center junction will recover by a recombination process. After all the junctions have recovered from their saturated condition, which existed during conduction, the SCR is capable of blocking in the forward direction.



Turn-Off Interval Current Waveform for SCR_1 (Vertical Scale—4.5A/cm) (Horizontal Scale—1 μsec/cm) Figure 9.13

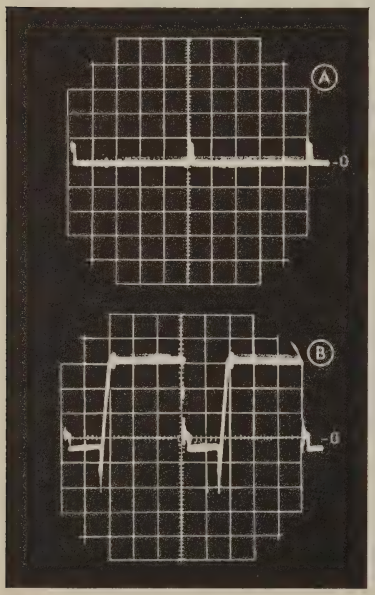
The voltage at the junction (A) of C_3 and the anode of SCR_2 is 16 to 50 volts positive above the supply voltage for the load range of 40 to 2 ohms, respectively. With the 2Ω load of Figure 9.9, the voltage between junction "A" and ground is shown in Figure 9.14(B). This voltage at C_3 is the charging source for the unijunction relaxation oscillator, UJT_2, that is used to turn on SCR_2. SCR_2 will connect C_3 to the cathode of SCR_1, making it more positive than the anode which effectively reverse biases SCR_1 and turns it off. The conduction time of SCR_1 is thus controlled by R_4 in the timing circuit of the UJT_2 trigger generator.



Waveforms for C_3
(Horizontal Scale—200 μsec/cm)
(A) Charging Current
(Vertical Scale—2.25A/cm)
(B) Voltage Waveform
From Junction "A" to Ground
(Vertical Scale—20V/cm)
Figure 9.14

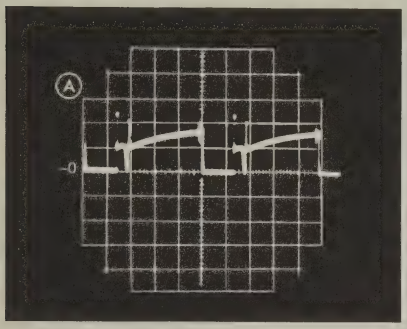
Using the higher voltage available on C_3 as a charging source permits higher frequency operation of the SCR_2 triggering circuit and thus shorter conduction periods for SCR_1.

Figure 9.15 shows the voltage and current waveforms for SCR_2. The initial transient current rises to 1.5 amps and then drops to .72 amp for most of the 40 μsec conduction period.

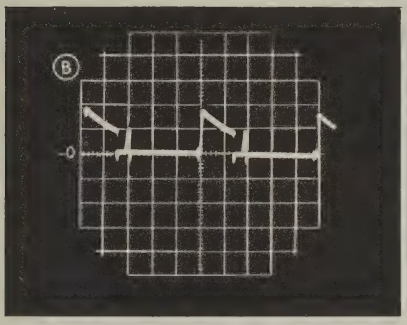


Waveforms for SCR_2
(Horizontal Scale—200 μsec/cm)
(A) Current Waveform
(Vertical Scale—.9A/cm)
(B) Voltage Waveform
(Vertical Scale—20V/cm)
Figure 9.15

The current flowing from the load end of the auto-transformer is shown in Figure 9.16. This current initially rises to 10.3 amps and the difference between this and the 17 amp peak from SCR_1 (see Figure 9.11(B)) is the peak charging current to C_3 of 6.7 amp (see Figure 9.14(A)). The 3 amp pulse of charging current (following the transient) to C_3 is the major remaining difference between the current waveforms of Figure 9.11(B) and Figure 9.16.

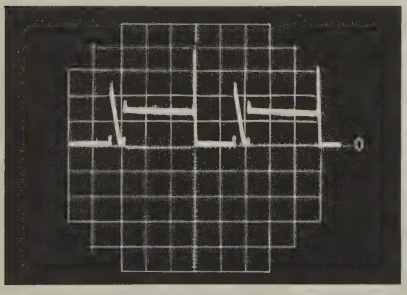


Current from Load End of Auto-Transformer (Vertical Scale—4.5A/cm) (Horizontal Scale—200 μsec/cm) Figure 9.16



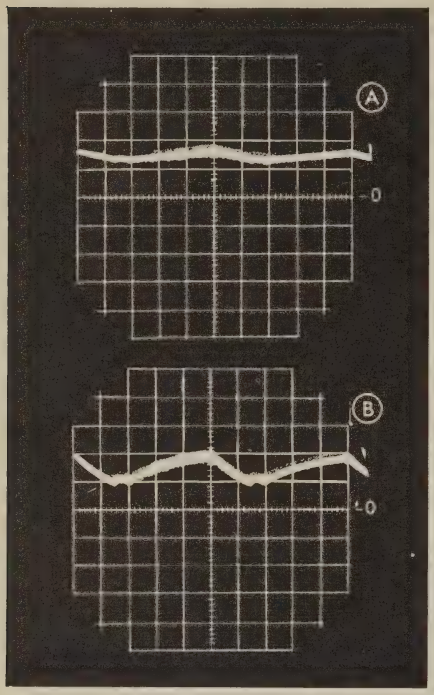
1N2156R Current Waveform (Vertical Scale—4.5A/cm) (Horizontal Scale—200 μsec/cm) Figure 9.17

The 1N2156R rectifier in Figure 9.9 is a clamp which prevents the voltage from swinging below ground and thus decreases the voltage requirements for the SCR's. For reactive loads, it feeds back the reactive current (see Figure 9.17) and with the 1 mh inductance in series with the load it gives filtering (i.e., smoothing action). This smoothing action can be seen by comparing Figure 9.18 with that of Figure 9.19(A), which has an average voltage of 14.3 volts. Figure 9.19(B) shows the additional filtering when shunting the load with a 500 μfd capacitor as in Figure 9.9. This circuit performs as a variable step-down DC



Voltage Across 1N2156R (Vertical Scale—20V/cm) (Horizontal Scale—200 μsec/cm) Figure 9.18

transformer with an output voltage variable with R4 from 3 to 19 volts. The output has a 1 Kc ripple frequency and additional filtering at this higher frequency is more economical. A regulated output can be achieved by a feedback network to automatically adjust the timing of the UJT_2 trigger generator.



Voltage Across 2Ω Load
(Vertical Scale—10V/cm)
(Horizontal Scale—200 μsec/cm)
(B) 500μf Capacitor Added
Figure 9.19

The 1 mh air core series inductance limits the current for loads approaching temporary short circuits as with capacitor, incandescant lamp, or a DC motor. This type of circuit is adaptable for lamp dimming and DC motor speed control. The overall circuit efficiency is better than 80% for a 90% conduction time of SCR_1, and the efficiency decreases for shorter conduction periods where the fixed circuit losses become a higher percentage of the output power.

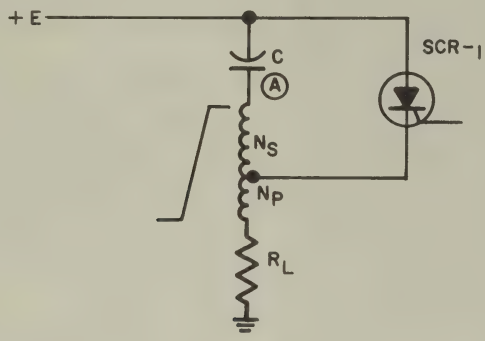
There is a reverse peak current of 10 amp through the 1N2156R (see Figure 9.17) which contributes significantly to the junction temperature rise since there is a reverse voltage transient of 105 volts during part of the same interval (See Figure 9.18).

The 1N91's connected from the gate to cathode on the SCR's provide a low impedance, and thus attenuate negative gate to cathode voltage pulses. Negative pulses that reach base one of the unijunction relaxation oscillator may cause it to fire prematurely. For this reason, the 1N91 bridge was needed for additional isolation between UJT_1 and SCR_1. The positive turn-off pulse applied to the cathode of SCR_1 is the source of the pulse which the 1N91 bridge attenuates.

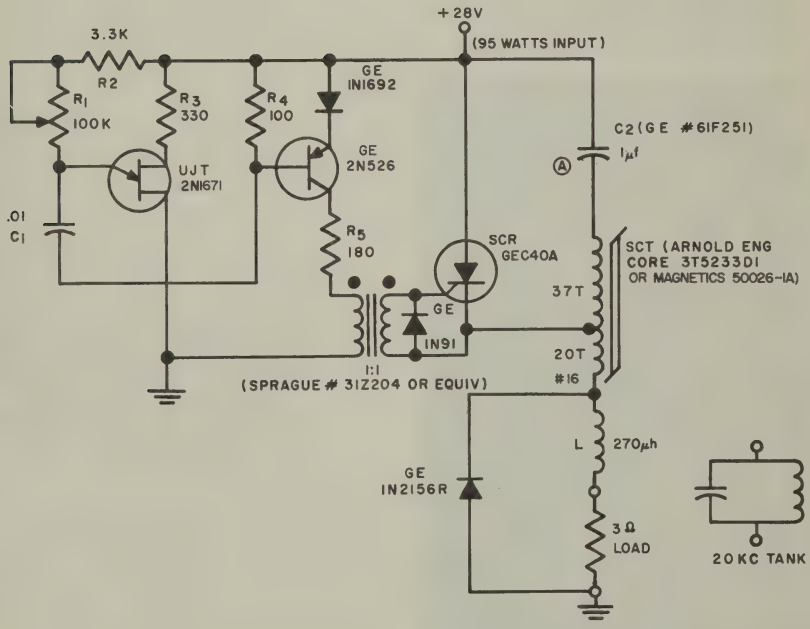
C_1 in conjunction with C_2 serves as an attenuator for positive power supply pulses that appear across C_2 and cause premature firing of UJT_1.

9.2.1 Morgan Circuit

For many chopper circuit applications, the circuit of Figure 9.20 that was invented by R. E. Morgan of the G-E General Engineering Laboratory may be desirable. The Morgan circuit eliminates the need for the diode and SCR_2 of Figure 9.8. The switching function performed by SCR_2 is accomplished by saturating the square loop core. With this circuit, the current pulse width to the load is more or less fixed by the time it takes the core to saturate and the energy to the load can be varied with the trigger rate of SCR_1.



Morgan Circuit
Figure 9.20



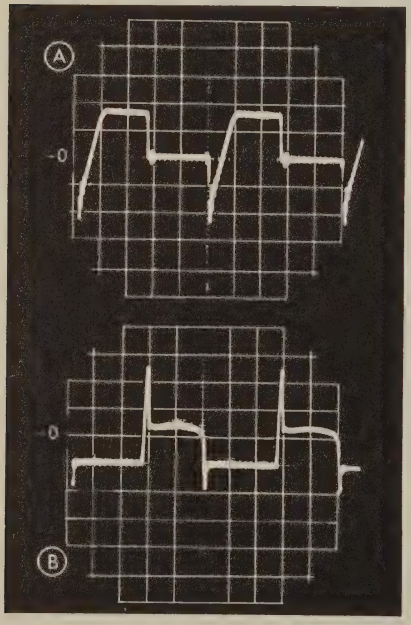
DC Chopper
Figure 9.21

Initially, point A is at zero potential so when the SCR is triggered the full line voltage appears across N_S, quickly driving the core to negative saturation. When the core saturates, the capacitor charges rapidly toward the supply potential and then the increasing load current starts driving the core toward positive saturation. Between negative and positive saturation, the core acts like a transformer and the capacitor is charged above the supply voltage to a potential determined by the load current. When positive saturation is reached, the core again becomes essentially a short-circuit and the charged capacitor drives the cathode of the SCR above the anode voltage, thus turning it off. Because of the circuit inductance, the voltage excursion at point A (after the first cycle) varies from below ground potential in the interval before SCR_1 is fired to above the supply potential at SCR_1 turn-off time.

The design of the saturable current transformer (SCT) is all important for proper operation of the circuit in a particular application. Selection of an approximate core size is simplified by using the Magnetics, Inc. "Tape Wound Core Calculator and Instruction Book." This slide-rule core-selector factors in the pulse width, core voltage, wire size, number of turns, and winding factor.

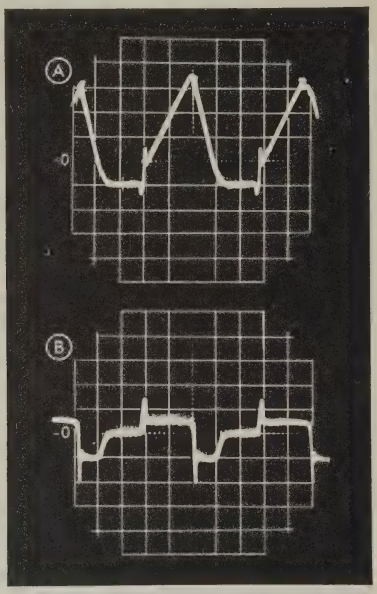
Figure 9.21 is a Morgan circuit that operates with a pulse width of about 40 μsec. The pulse width is partially dependent on both the load and the series inductance L. The pulse frequency is variable with R_1.

For the following waveforms, the circuit of Figure 9.21 was operated at a 10 Kc switching rate. Figure 9.22 shows the voltage and current waveforms for the SCR. Figure 9.23(A) shows the bottom plate of C_2 to be 20 volts below ground in the interval before triggering the SCR. When the SCR is triggered, the additional supply voltage across the 37 turns drives the core toward negative saturation and the inrush of current to C_2 (see Figure 9.23B) raises the



Waveforms for SCR
(Horizontal Scale—20 μsec/cm)
(A) Voltage—Anode to Cathode
(Vertical Scale—20V/cm)
(B) Current—Anode to Cathode
(Vertical Scale—4.5A/cm)
Figure 9.22

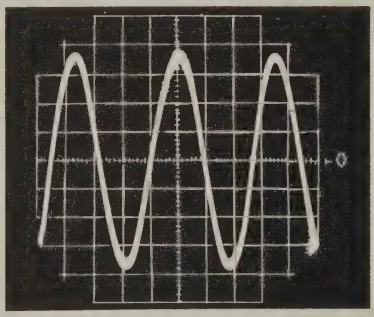
voltage (at point A) rapidly to about ground potential. The load current through transformer action drives the core to positive saturation. The capacitor C_2 then discharges through the saturated inductance and causes reverse current of about 4.5 amp (see Figure 9.22B) to flow in the SCR. The time duration of this discharge current establishes the reverse bias time for the SCR and must be sufficient for the gate to regain control.



Positive Saturation Waveforms for C2 (Horizontal Scale—20 μsec/cm) (A) Voltage at "A" to Ground (Vertical Scale—20V/cm) (B) Current to Bottom of C2 (Vertical Scale—4.5A/cm) Figure 9.23

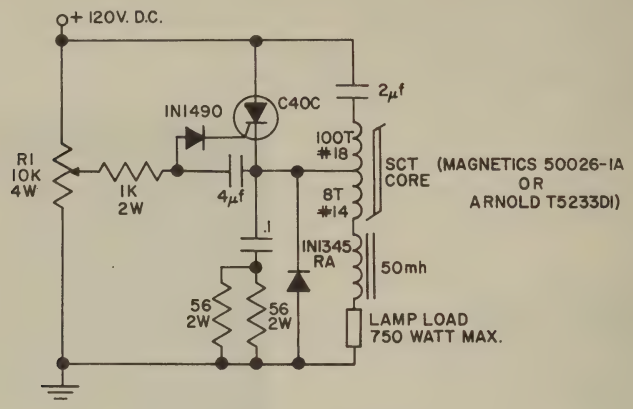
The triggering circuit of Figure 9.21 uses the UJT to drive the 2N526 from cut-off to saturation. Since we are not using the energy in C_1 to trigger the SCR, the smaller (.01 μf) capacitor size can be used and thus achieve UJT operation to 20 Kc. The 1N1692 keeps the emitter-base junction of the 2N526 reverse biased except for the discharge interval of C_1. R_5 limits the voltage amplitude of the trigger pulse to the SCR. The 2N526 also isolates the SCR turn-off pulse from the UJT timing circuit.

The circuit of Figure 9.21 can be used to pulse a tank circuit connected in place of the 3Ω load. Figure 9.24 shows the voltage waveform across the 20 Kc tank with the SCR switching at a 10 Kc rate.



Voltage Waveform Across 20Kc Tank Figure 9.24

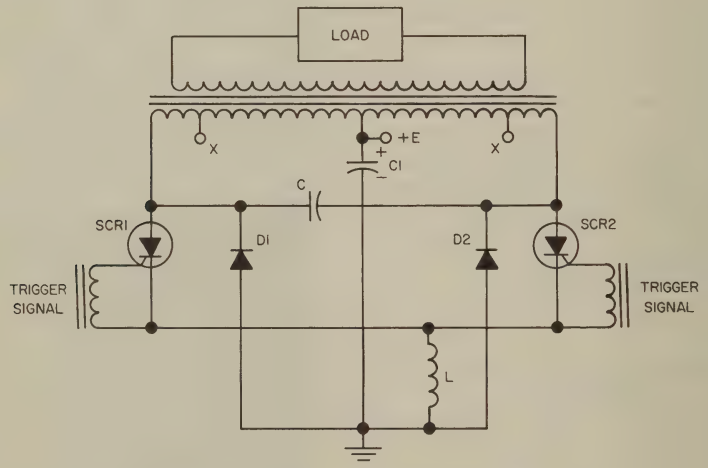
Figure 9.25 is a Morgan circuit that gives a variable chopping rate with variation of R_1 for controlling the intensity of a lamp load.



750 Watt Lamp Dimmer
Figure 9.25

9.3 PARALLEL INVERTERS

One of the major applications for SCR's is converting DC to AC and the parallel inverter is often the most practical method. The parallel inverter configuration shown in Figure 9.26 provides an output that is essentially a square wave at operating frequencies below 3 Kc. By rectifying the output voltage, the circuit makes an efficient DC to DC converter in applications such as power supplies for mobile transmitters. An AC input can be rectified to provide the primary power for the inverter, in which case it will function as a frequency changer.



DC to AC (Square Wave) Inverter
Figure 9.26

A trigger signal that applies a steep wave front of positive polarity alternately to the gates of SCR_1 and SCR_2 is preferable. Assume that SCR_1 is conducting and SCR_2 is blocking. The current from the supply E will then flow through the left hand side of the transformer. Auto-transformer action will produce a voltage of approximately 2E at the anode of SCR_2 and across the capacitor C. When the next trigger pulse is applied to the gate of SCR_2, it will turn on and the top end of L will rise momentarily to about 2E, which reverse biases SCR_1 and causes it to turn off. The capacitor C and inductor L will maintain a reverse bias across SCR_1 long enough for SCR_1 to recover to the blocking state. The next trigger pulse will occur at the gate of SCR_1 and cause the circuit to revert to the original state. In this manner, the current from the supply E will flow alternately through the two sides of the transformer primary and produce an AC voltage at the load.

A conventional parallel inverter circuit differs from the square wave inverter shown in Figure 9.26 in that the diodes and the electrolytic across the supply would be missing and the L and C components would be larger. The conventional parallel inverter presents a problem with varying load conditions, for the correct amount of commutating capacity can be selected for only one load value. Therefore, during light load conditions, the reduced load current makes the waveform depart considerably from a square wave and the peak SCR voltage can rise to several times the supply voltage. This condition is even more predominate when the load power factor (PF) increases with a circuit designed for a lagging low PF load. Thus, the load range must be restricted for the lower PF loads in order to prevent losing commutation voltage (under heavy loads) or having excessive SCR voltage (under light loads).

The improved parallel or square wave inverter shown in Figure 9.26 was developed by W. McMurray and B. D. Bedford of the General Electric General Engineering Laboratory. Although the new circuit superficially resembles a conventional parallel inverter, its method of commutation is entirely different and the use of feedback diodes makes it uniquely suited for driving reactive loads. This circuit has substantially a square wave output voltage under all load conditions and does not create high voltages across the SCR's under lightly loaded or no-load conditions.

A major advantage of the new circuit is its ability to operate under lightly loaded or open circuit conditions. The feedback diodes prevent the voltage across either half of the primary winding from exceeding the supply voltage. These diodes not only maintain a square wave output under all load conditions, but also permit the use of lower breakover-voltage (and less expensive) Silicon Controlled Rectifiers.

The DC source should have a low transient impedance, and a capacitor on the output of the DC supply is usually required so it can accept power as well as supply power. It is often important to have this capacitor (C_1) right at the inverter itself as shown in Figure 9.26 since the inductance of the supply leads of a few feet in length represents an undesirable impedance during the μsec switching intervals.

The series inductance L of Figure 9.26 is quite small (compared to that used in conventional parallel inverters) and chosen to resonate with C to create

a short impulse to turn off the conducting SCR. It also serves as a ballast to prevent excessive current flow during switching. During the switching interval opposing currents flow in both halves of the transformer primary to the commutating capacitor and to the anode of the SCR, which has been turned on. These opposing primary currents decrease the power delivered to the load. This switching interval is decreased by using inverter type SCR's as discussed in Chapter 5. The values of C and L are determined by the maximum current to be commutated, the DC supply voltage, and the turn-off time of the SCR's.

The capacitor discharge of C through L is oscillatory. When the anode of SCR_2 goes below ground, for instance, diode D_2 conducts. This conduction occurs at the end of the commutating interval of SCR_1 and causes the remaining commutating energy stored in L to be dissipated in the forward direction of D_2, SCR_2, and the winding resistance of L.

With an inductive load the operation of the inverter is more complex. Again, assuming that SCR_1 is conducting, turning on SCR_2 will turn SCR_1 off as described previously. An inductive load, however, prevents the main load current from reversing instantaneously so transformed load current must flow through D_2 back into the DC supply until the load current reverses. During this feedback interval the current through SCR_2 will fall to zero and SCR_2 will actually become back-biased so that it will have to be triggered again when the load current reverses. After being re-triggered, SCR_2 will continue conduction for the rest of the half cycle. SCR_2 can be re-triggered either by supplying another pulse at the proper time or more easily by maintaining gate drive for the full half cycle if the load has a varying PF. The 180° drive is easily obtained with a transistor multivibrator that uses a unijunction to stabilize and control the frequency (e.g., see Figures 9.27 and 9.28 and also the General Electric Transistor Manual, Fifth Edition, page 145).

In applications where the feedback current results in considerable circuit losses, the efficiency may be improved by connecting the cathode of each feedback diode to a tap "X" on the primary transformer winding (see Figure 9.26). This arrangement will increase the load voltage during the feedback interval and cause some departure from a square wave.

The last part of Chapter 5 discusses the selection of the type of commutating capacitor. The minimum value of commutating capacity C can be approximated by the following equation:

$$C \geqq \frac{t_o I}{V} \mu fd$$

where t_o = turn-off time in μsec
I = load current in amperes at time of commutation
V = charge voltage on C

The value of L is not critical and usually is in the range of 50 to 200 μh. The final selection of L in conjunction with C may be based on the rate of rise vs. overshoot of reapplied SCR forward voltage, and the minimum trapped commutating energy in L vs. the peak switching current. Finally, L and C are usually selected to resonate in the 15 to 40 Kc frequency range so the resonate pulse developed across L will provide sufficient turn-off time for the inverter SCR's.

9.3.1 Inverter Trigger and Output Transformer Requirements:

The preferred triggering signal for SCR inverters is a steep wave front applied alternately to the SCR gates. The duration of the gate signal depends on the buildup of the load current vs. time, for gate drive must be maintained until the load current through the SCR exceeds the hold-in value for the SCR. If the trigger signal is lost with a parallel inverter circuit, one of the SCR's remains on and the current is limited only by the circuit and supply resistance.

Transistor multivibrators, saturable reactors, unijunction and other transistor trigger generator circuits have been used to drive SCR inverters (e.g., see Chapter 4).

With the improved or square wave inverter circuit, the starting problem is greatly reduced. The small commutating capacitance can be charged to full voltage in a short time and the inverter can start and operate under no-load conditions. However, precautions must still be taken to prevent saturation of the transformer during starting. For example, on starting under full load the condition of the flux in the transformer (together with the order in which the SCR's are triggered) may be important in determining whether the circuit will start successfully. If the initial flux in the transformer is near its peak value and the circuit is started in such a way that the flux is increased further, the transformer may saturate and prevent commutation of the circuit at the next trigger pulse. This situation can be prevented by increasing the size of the transformer or by shortening the time duration of the first half cycle of operation.

A transformer having a toroidal, square loop magnetic core often causes random starting difficulties due to residual effects in the core. Changing to a transformer having a core with an air gap and operating at lower flux densities will remedy the starting difficulties caused by the output transformer. As a general rule of thumb, it is desirable to select a transformer and core with a volt-second saturation capability that is at least two and preferably three times the actual circuit requirements. The leakage inductance should be held to a minimum since the transformer will be subjected to rapidly changing currents during the commutation interval, and the leakage reactance must be offset with sufficient commutating capacity. Bifilar transformer winding is usually used to obtain tight coupling between the two primary windings. Since the SCR inverter output transformer cannot be allowed to saturate, its design must either incorporate an air gap, have a high ratio of saturation to residual flux density, or be used with predictable reset circuitry. Magnetic core reset circuitry is discussed in the last section of this chapter, DC to DC converters.

The above comments indicate that the design of the output transformer is a major factor in a parallel inverter circuit.

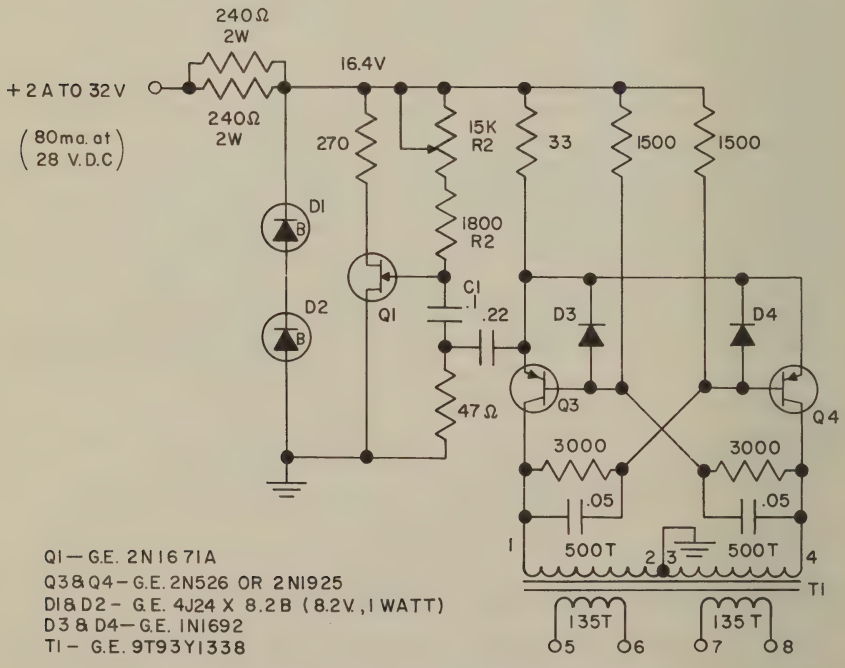
9.3.2 Typical Inverter Trigger Circuit

One of the important design problems for SCR parallel inverter circuits involves the triggering of one SCR enough in advance of the second so that the commutating capacitor will have assumed ample charge for commutation by the time the second SCR is triggered. The triggering circuit of Figure 9.27

does this with alternating trigger signals that meet all the requirements for inverters using C40, C12, or C9 type SCR's. This circuit provides symmetrical square wave gating signals with fast rise time. If an imbalance were to exist in the conducting interval of an SCR inverter, there would be a DC component tending to saturate the transformer and second harmonics would be produced in the output.

The circuit of Figure 9.27 is a slightly modified "hybrid-multivibrator," described in more detail in Chapter 4. The unijunction transistor provides a source of short, precisely timed negative pulses with the period between pulses depending on the C_1R_2 time constant. These pulses are coupled to the common emitter resistor of a conventional transistor flip-flop (Q3 and Q4). Each pulse from the unijunction transistor will turn off the transistor which is on in the flip-flop and the resulting square wave of voltage at the collectors is coupled to the SCR gates by a small transformer. D3 and D4 are used to prevent the emitter-base voltage of Q3 and Q4 from exceeding ratings when a transistor is turned off.

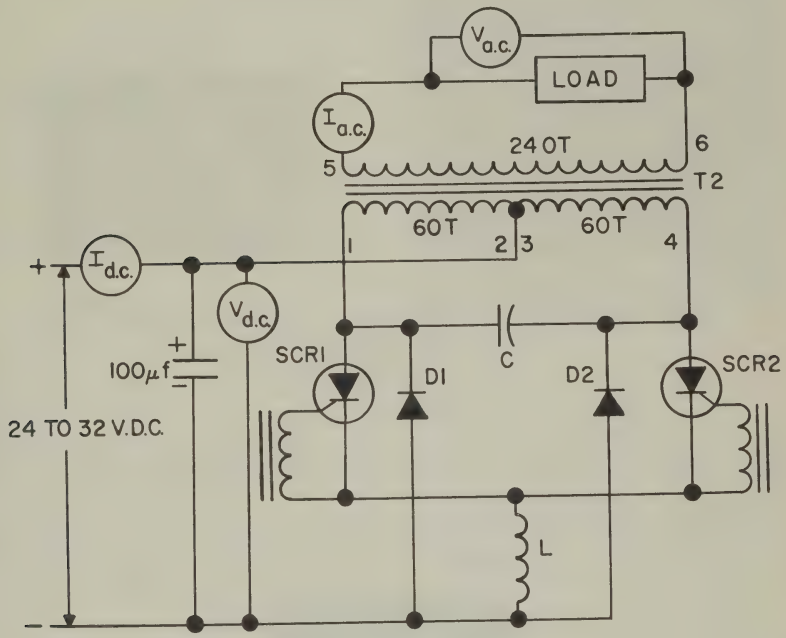
The multivibrator free runs at about 100 cps, but is synchronized and controlled by the unijunction at the higher operating frequencies at which it is designed to operate. The avalanche (zener) diodes form a simple shunt regulator to keep the collector-emitter voltage of the transistors within ratings. This circuit has good frequency stability with variations in supply voltage and ambient temperature, due to the inherent stability of the unijunction. The circuit



Square Wave Inverter Trigger Circuit for C40 or Smaller Type SCR's
Figure 9.27

can trigger an inverter with an output frequency of from 400 cps to 2500 cps in an ambient temperature of up to 70°C. This trigger presents a generator resistance of about 8 ohms and an open circuit voltage of about 4 volts peak.

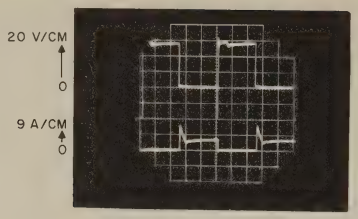
The presence of negative gate voltage during the SCR blocking period is advantageous from the standpoint of avoiding false firing due to either line transients or spurious pulses coupled into the gating circuit. Reverse gate voltage also reduces the forward leakage current of the SCR, yielding increased reliability. Also the possibility of misfiring at the time of reapplication of forward voltage is reduced.



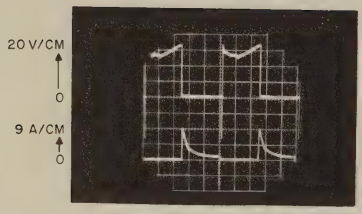
170 Watt Square Wave Inverter
Figure 9.28

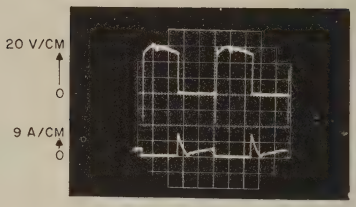
9.3.3 *Typical Square Wave Inverter Circuits*

Figure 9.28 is a square wave inverter circuit that provides 12 μsec or greater turn-off time with the minimum supply voltage of 24 volts and a 70 Ω resistive load. The following waveforms were taken with the inverter frequency at 400 cps and a power input of 170 watts at full load (70 Ω, PF = 1.0) and nominal supply voltage of 28V DC. Figure 9.29 shows the voltage and current waveforms for the SCR's in Figure 9.28.



(A) PF = 1.0



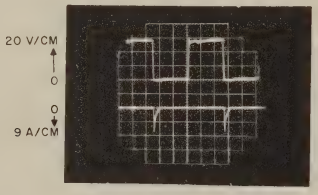


(B) PF ≈ .7 Leading **(C) PF ≈ .7 Lagging**

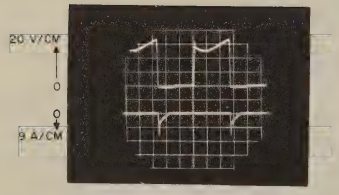
SCR Waveforms for Three Different Load Power Factors (PF)
(Hor. Scale—500 μsec/cm)
Figure 9.29

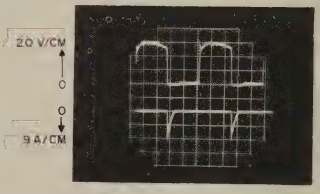
Figure 9.29(B) and (C) with a load PF of about .7 were obtained by inserting the reactive component in series with the 70 ohm resistive load. The high peak current when an SCR turns on is the sum of the load current and the commutating current from C.

Figure 9.30 shows the voltage and current waveforms for diodes D_1 and D_2 of Figure 9.28. The load conditions are the same as for Figure 9.29.



(A) PF = 1.0





(B) PF ≈ .7 Leading **(C) PF ≈ .7 Lagging**

Diode Waveforms for Three Different Load Power Factors (PF)
(Hor. Scale—500 μsec/cm)
Figure 9.30

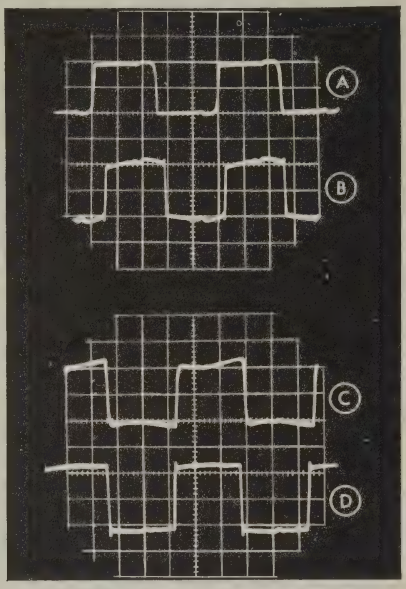
Figure 9.31 shows the load voltage for four different load conditions.

(A) Load PF = 1

(B) Load PF ≈ .7 Lagging

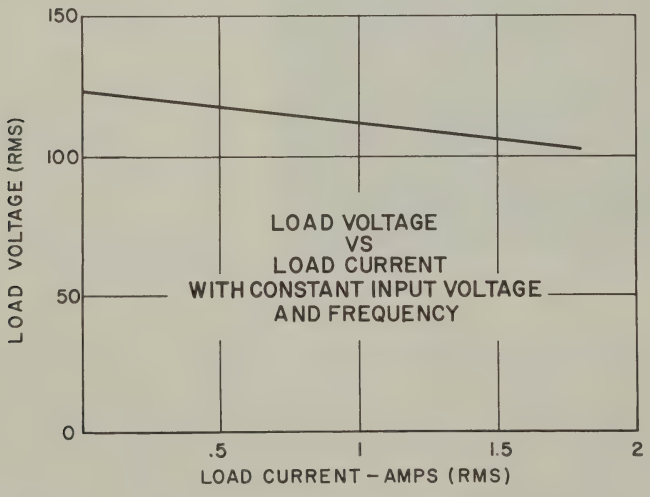
(C) Load PF ≈ .7 Leading

(D) Load Open Circuit



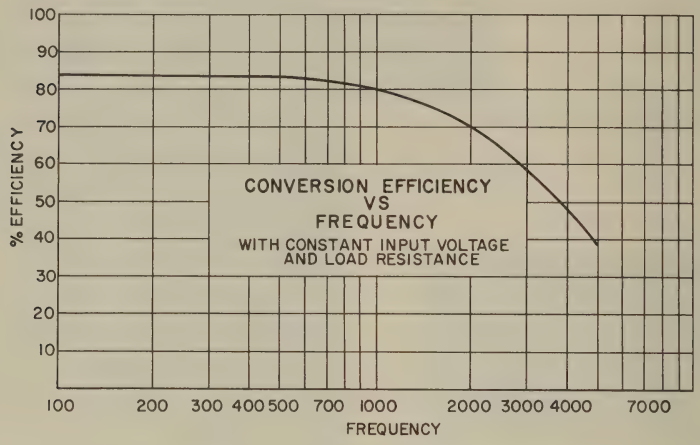
Load Voltage for 4 Different Load Conditions
(Hor. Scale—500 μsec/cm)
(Vert. Scale—100 V/cm)
Figure 9.31

The inherent regulation of the square wave inverter is evident in Figure 9.31 and also in Figure 9.32.



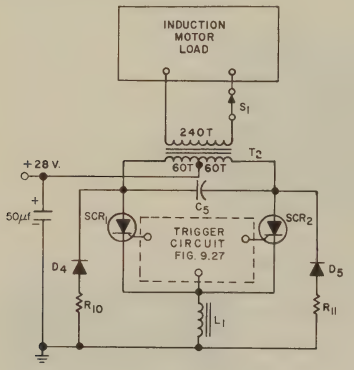
Square Wave Inverter Regulation
Figure 9.32

The efficiency of the square wave inverter circuit of Figure 9.28 vs. frequency is shown in Figure 3.33. The output voltage and current meters are of the thermal type in order to obtain true rms readings.



170 Watt Square Wave Inverter vs. Frequency for Circuit of Figure 9.28
Figure 9.33

The drop in efficiency above 1000 cps becomes more severe because the switching interval becomes an appreciable part of the total period. It is during the switching interval that the power losses in the semiconductors and the commutating capacitor reach their peak. It is also in the switching interval that current cancellation takes place in the transformer primary. Transformer core losses also increase with frequency.



Square-Wave Inverter
Figure 9.34

R_{10}, R_{11} —— 1Ω, 20 W
C_5 —— 2–4 μfd UNITS IN PARALLEL, G.E. #61F254
D_4, D_5 —— G.E. IN2155
SCR_1, SCR_2 —— G.E. C40A
T_2 —— G.E. #9T93Y1337
L_1 —— G.E. #9T93Y1336–50μh

The square wave inverter circuit of Figure 9.34 operates with a reactive load consisting of three Eastern Air Devices, Inc. "J31B Capacitor Motor" blowers. With this inverter it is possible to vary the speed of the induction motors by changing the trigger frequency to SCR_1 and SCR_2.

This circuit differs from Figure 9.28 by having resistors R_{10} and R_{11} in series with the feedback diodes. This permits the trapped commutating energy in L_1 to be dissipated for the most part in these resistors rather than in the semiconductors and the winding resistance of L_1. If these diodes carry considerable reactive load current in addition, the efficiency will be decreased. If high efficiency with reactive loads is important, then eliminate the resistors and couple this reactive current into the load by connecting the diodes to taps which are 10 to 15% in from the ends of the transformer (see Figure 9.26).

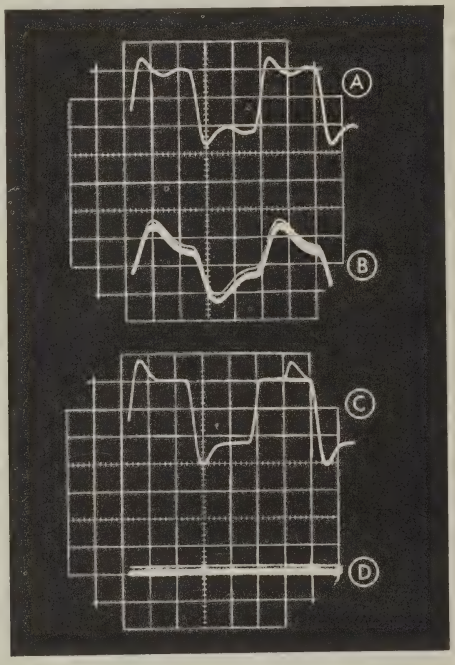
The circuit of Figure 9.34 operating at 1 Kc with 175 watts input has a voltage and current load waveform as shown in Figure 9.35(A) and (B). Figure 9.35(C) and (D) show the open circuit (S_1 open) waveforms.

(A) Voltage—100V/cm)

(B) Current—2A/cm)

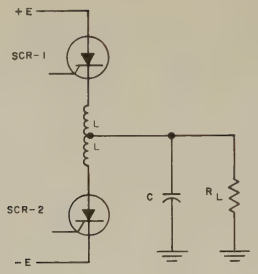
(C) Voltage, S1 Open

(D) Current, S1 Open



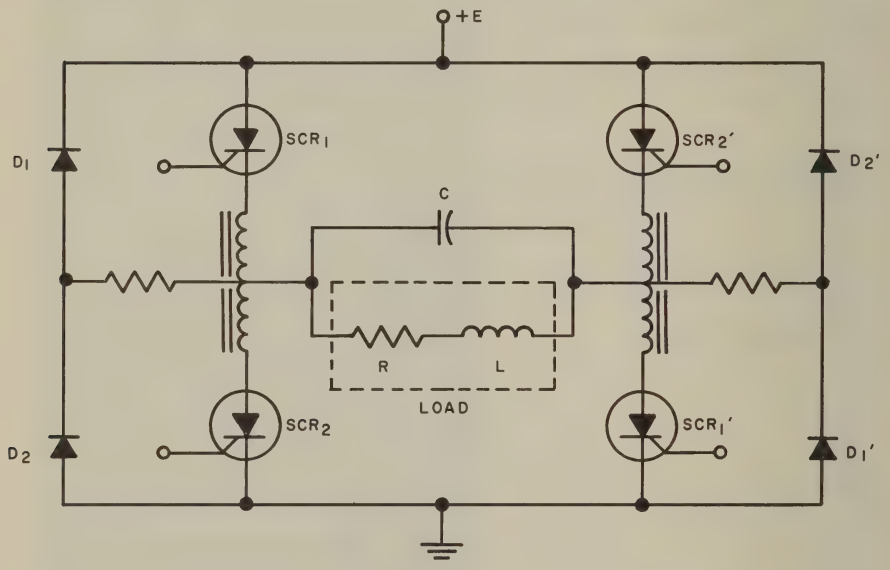
1 Kc Load Waveforms
Figure 9.35

A different form of square wave inverter is shown in Figure 9.36. Notice the similarity of this circuit, with the exception of the tapped power supply, to the circuit in Figure 9.7. The operation is similar to the overdamped shunt load and by using both a positive and negative supply as in Figure 9.36 a square wave output can be obtained across the load. With the overdamped circuits, the choke and capacitor are chosen so the discharge of the capacitor through the choke will back bias an SCR for about 15 μsec with the C40 series.



Square-Wave Inverter Using C. T. Choke
Figure 9.36

The circuit of Figure 9.37 is a bridge version of Figure 9.36 and includes diodes to feedback the reactive load current to the supply. The bridge circuit eliminates the need for a center-tapped supply.



Square-Wave Bridge Inverter
Figure 9.37

9.3.4 A 400 Cycle Variable Pulse Width Inverter

To achieve regulation by varying the pulse width in the inverter itself means that the normal 180° conduction angle for each leg of the inverter can be shortened in accordance with the demands of the load to maintain regulation.

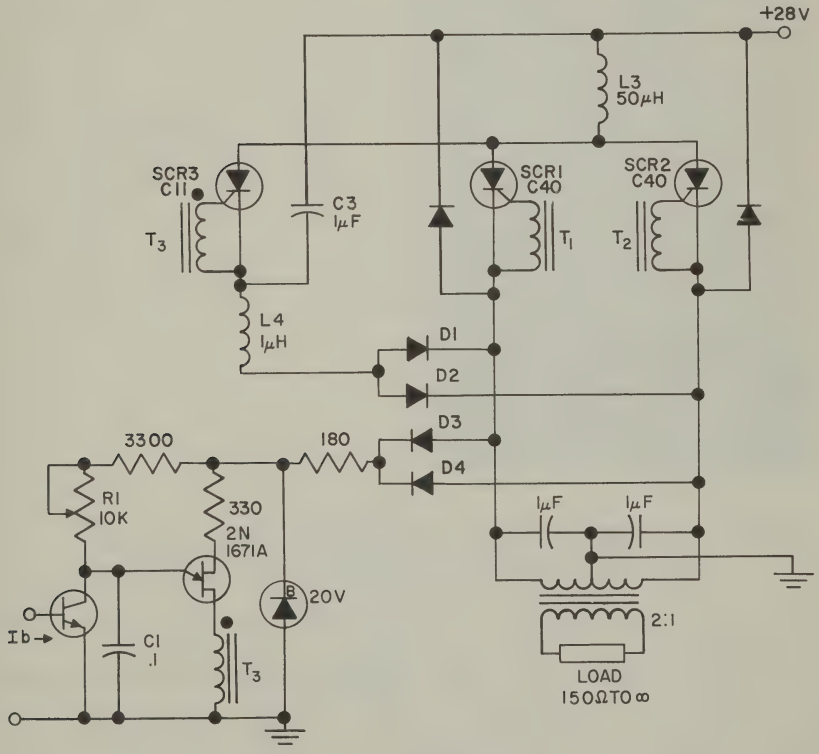
The circuit of Figure 9.38 uses a technique for varying the conduction time of SCR_1 and SCR_2 with only one extra SCR (#3) in conjunction with a small inductor and two conventional rectifiers. All of these components in the

turn-off circuit may have low power capabilities since they handle only the turn-off energy for SCR_1 and SCR_2. Transformer action in charging the commutating capacitor through D_1 and D_2 keeps the size of C_3 equal or less than that required for conventional parallel inverters.

With SCR_1 conducting, the lower plate of C_3 charges to approximately —170 volts, and also C_1 starts its charge period. The value of R_1 controls the relaxation oscillator frequency which determines the conduction time of SCR_1. The 2N1671A triggers SCR_3 which accomplishes turn-off of SCR_1 by connecting the negatively charged plate of C_3 to the anode of SCR_1 and also in parallel with L_3. A resonant negative pulse is developed across L_3 which reverse biases SCR_1, thus turning it off. The capacitor from SCR_1 cathode to ground clamps the cathode while the negative turn-off pulse is applied to the anode. Also this capacitor eliminates the switching transients from the load.

D_3 and D_4 provide the supply voltage to the relaxation oscillator circuit and provide synchronization so the start of the charging period for C_1 coincides with the start of conduction for SCR_1 or SCR_2.

SCR_3 turns off SCR_2 in the same way that SCR_1 is turned off. SCR_3 conducts for only a very short period since it is turned off when the current reverses in the resonant circuit of L_3 and C_3. An important feature for successful

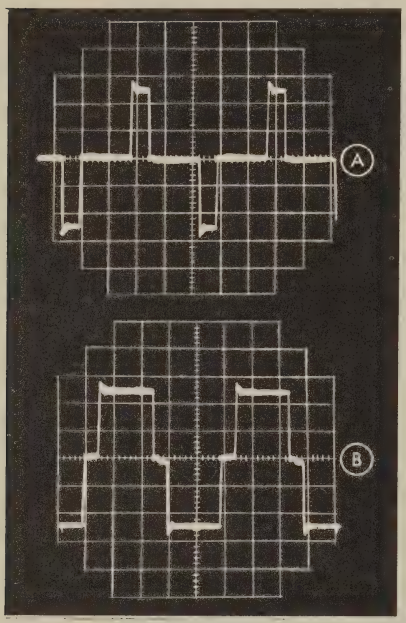


400 cps Variable Pulse Width Inverter
Figure 9.38

operation of the circuit depends on selecting a value of inductance for L_4 which will keep the current through it to a low value until SCR_3 is turned off by the reversal of the L_3-C_3 resonant current.

The basic circuit of Figure 9.38 without the SCR_3 turn-off feature is a square wave inverter as described in Section 9.3.1.

Varying R_1 or I_b changes the pulse width over the range indicated in Figure 9.39. With feedback circuitry to control I_b, it would be a regulated inverter with an output waveshape which is favorable for shaping to a sinewave. The Figure 9.38 circuit is supplied with short duration trigger pulses to T_1 and T_2. For reactive loads, the trigger pulse width must be extended in time for the duration of reactive current flow. The maximum pulse width at the gate cannot exceed the inverter pulse width; therefore for large reactive loads the trigger pulse width must follow the changing inverter pulse width. This varying trigger pulse width can be obtained by varying the symmetry of a multivibrator as a function of the inverter pulse width.



400 ~ Variable Pulse Width Inverter
(Vert. Scale—20V/cm)
(Hor. Scale—500 μsec/cm)
Figure 9.39

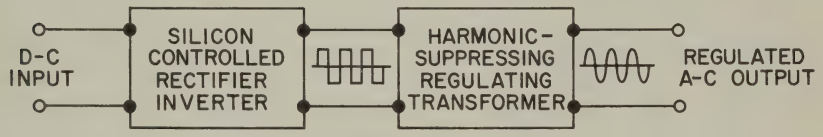
9.3.5 A Voltage Regulated SCR Inverter with Sinewave Output and Current Limiting

The designers of DC to AC inverters have the following problems which must be solved:

1. Maintaining a constant output voltage in spite of variations of load current or input voltage.
2. Instantaneous and steady-state protection against short-circuit conditions.
3. Production of a low distortion sinewave output waveform.
4. Proper operation with a wide variety of power factor loads.

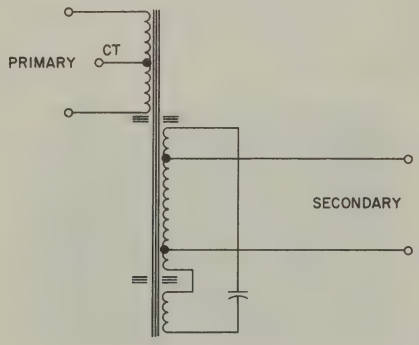
The silicon controlled rectifier is ideal for use in inverters since it can carry large currents after once being triggered, and the voltage drop in the conducting state is only about one volt. One major drawback of this type of device, however, is that there is no inherent current limit as there is in a transistor since, once triggered, the current is limited only by the external circuit.

The block diagram of a system to accomplish most of these objectives is shown in Figure 9.40. It consists essentially of a square-wave inverter driving a harmonic-suppressing regulating transformer. The inverter output is essentially a square wave. The transformer converts the square waves to sinewaves, provides short-circuit protection, and some regulating action.



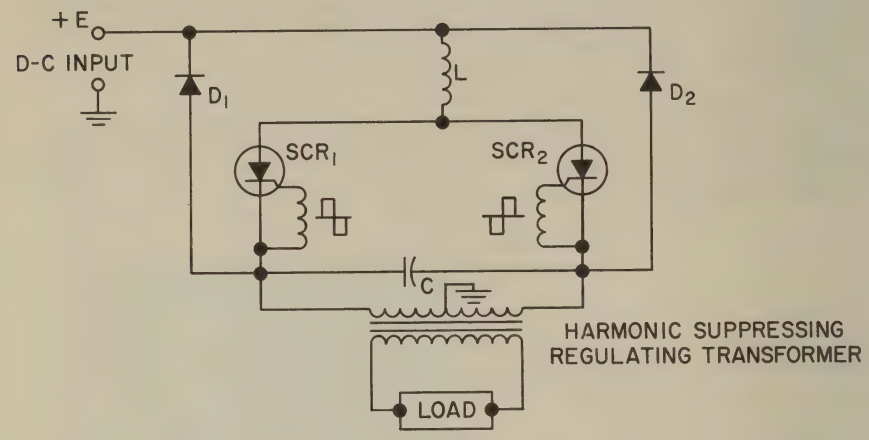
Block Diagram
Regulated DC to AC Inverter
Figure 9.40

The harmonic-suppressing regulating transformer is well known and is shown by the schematic diagram of Figure 9.41. It consists of a transformer to which a magnetic shunt has been added so that all of the secondary flux does not link with the primary. With a capacitive load on the secondary, the magnetizing flux and secondary flux will add, thus keeping the secondary magnetic path in the saturated portion of the magnetization curve, but the primary is in the linear portion of the magnetization curve. The compensating winding gives additional regulation against line or load variations. The harmonic neutralizing winding is arranged to develop a voltage in opposition to the harmonics contained in the input voltage which would otherwise appear at the output terminals. Since the primary of the transformer is always operated in the linear portion of the magnetization curve, the primary current is still limited to a maximum value even if the secondary is short-circuited.



Harmonic-Suppressing Regulating Transformer
Figure 9.41

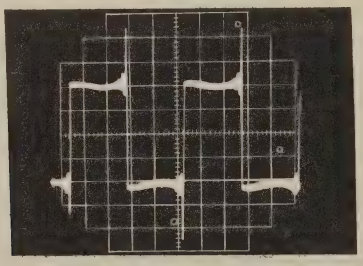
As might be expected, the effective load seen at the input to the harmonic-suppressing regulating transformer will vary quite widely in power factor and magnitude and it is necessary to drive this transformer with an SCR inverter that is extremely tolerant of load conditions. A circuit to accomplish this is shown in Figure 9.42. This is basically the square wave inverter discussed earlier.



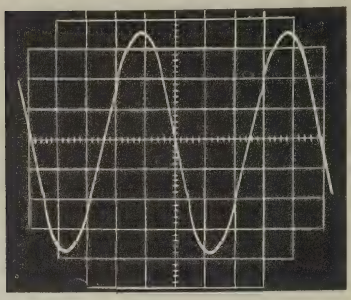
SCR Inverter for Sinewave Output
Figure 9.42

One advantage of the particular circuit configuration of Figure 9.42 is that the anodes of the SCR's are at the same electrical potential. Since the mounting stud of the SCR is the anode, this means that both SCR's can be mounted on the same heatsink. The feedback diodes in this configuration also have their cathodes at the same electrical potential so they can be mounted with their studs on a common heatsink.

The waveform at the output of the inverter is shown by Figure 9.43. It will be noted that the inverter output is a square wave except for the sharp spike and ringing at the leading edge caused by the discharge of the commutating capacitor. The output of the magnetic regulator is an excellent sinewave, Figure 9.44, having a total harmonic distortion under full load of about 3%.

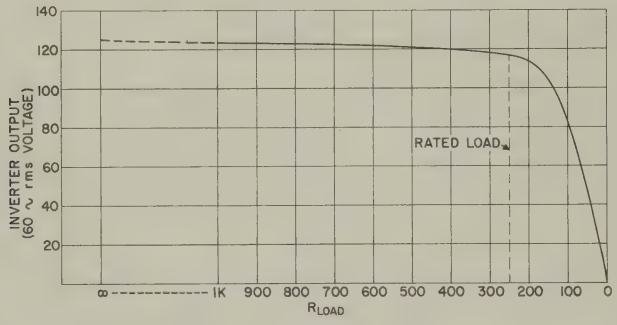


Inverter Output Waveform
(Vert. Scale—20V/cm)
Figure 9.43

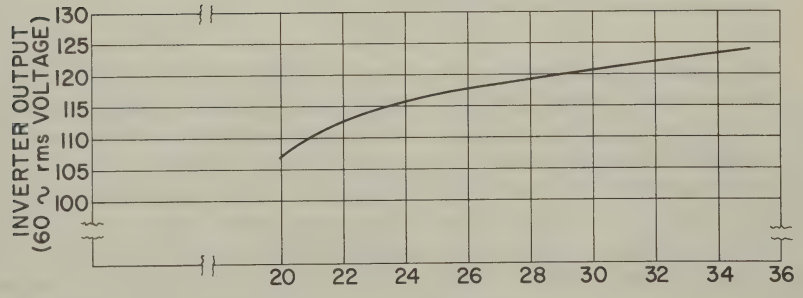


Secondary Voltage Waveform
Across Resistance Load
115 v.r.m.s., 60 cps
total harmonic distortion ≈ 3%
Figure 9.44

Figure 9.45 shows the variation of output voltage with load resistance for a small inverter-transformer combination. The open-circuit output voltage of 125.7 RMS dropped to 117 at full load. The current into the SCR inverter circuit reached a maximum at 130 ohms load. With the secondary of the regulating transformer short-circuited, the DC current in the SCR inverter was actually less than at rated load conditions. During the worst condition, the DC current handled by the SCR's was 140% of the full load current. This current limiting makes it possible to choose a commutating capacitor and heatsink that will allow the equipment to work into a full or partial short-circuit without exceeding the ratings of the SCR's or diodes.



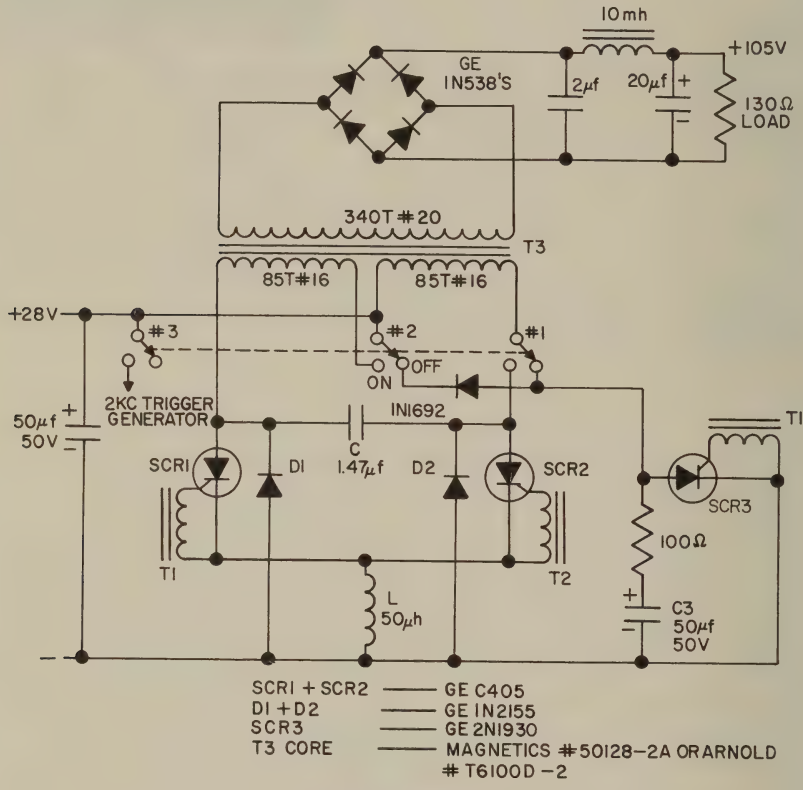
Inverter Output vs. Load
(DC Input Constant)
Figure 9.45



Inverter Input—DC
Figure 9.46

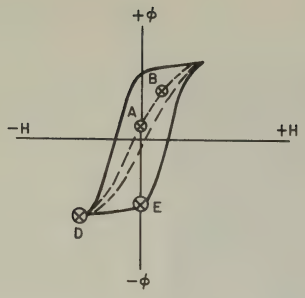
9.3.6 A DC to DC Parallel Converter

Many of the DC to DC conversion requirements for missile and aircraft applications use circuitry similar to Figure 9.47. This 28 VDC to 105VDC converter operates at approximately 2.0 Kc. It may be desirable to use a higher frequency to achieve size and weight reduction of the transformer and filter components, but the increased commutation losses may offset the anticipated size and weight reductions.



DC to DC Converter
Figure 9.47

The above circuit uses a square wave inverter with a square loop core transformer and core reset circuitry. The previous general practice for this circuit and other parallel inverters has been to use a transformer core with an air gap to give a low value of residual flux (ϕ). This is represented by the dashed hysteresis loop in Figure 9.48. This latter type of core is selected with a volt-second capability of 2 or 3 times the circuit requirement. This means that the core is operated at ½ to ⅓ its maximum flux density to avoid core saturation which would cause the circuit to malfunction. Typically, this type of operation might traverse the dashed loop from "A" to "B" during the first half-period of operation.



Typical Transformer Hysteresis Loop
Figure 9.48

This type of operation causes the core to be used inefficiently and the transformer size is considerably increased for a given power capability compared to a transformer with a square loop core as shown by the solid curve in Figure 9.48. The square loop core also gives improved transformer efficiency.

The advantages of the square loop core can be realized if it can be operated at higher flux densities and at the same time avoid saturation at start up in the initial half-period. This requires that the core flux at start-up be in the opposite direction to that at which it was last operated.

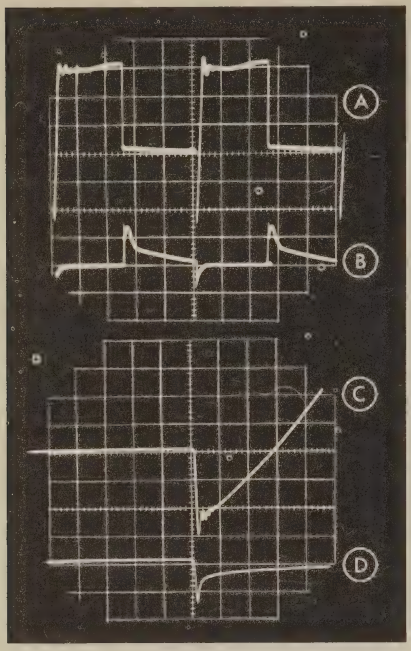
The core reset circuit shown in Figure 9.47 always sets the core at position "E" on the square loop after the circuit is turned off. Then the trigger circuit is arranged so that the first trigger pulse after the circuit is turned on goes to T_1 which fires SCR_1 and SCR_3. SCR_1 conduction causes current in the transformer to flow in the direction which causes the core flux to change from position "E" toward positive saturation at the opposite end of the square loop. SCR_3 conduction discharges the capacitor, C_3, so it will be ready to draw the transformer reset current when the circuit is switched off. When the reset current peaks, the core flux is at position "D" on the hysteresis loop. When the circuit is first turned off, C_3 has no charge; therefore, all the supply voltage appears across the transformer winding. Then, as the capacitor C_3 charges, the supply voltage shifts to the capacitor until the full supply voltage appears across C_3 at the end of the charging period.

For proper operation, the three-pole switch in Figure 9.47 should be arranged so that the sequence of closing the contacts in the ON position is in the order #1, #2, and #3.

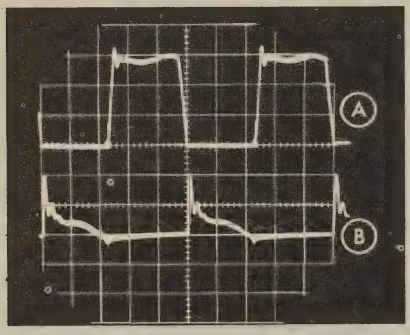
The core of transformer T_3 is actually large enough for 1 Kc inverter operation with adequate safety in flux density. The core flux actually reaches saturation at a frequency of about 400 cycles in this circuit. This is in agreement with the transformer design using the "Tape Wound Core Calculator and Instruction Book" by Magnetics, Inc. The following data is taken at 2 Kc operation.

The output at the load in Figure 9.47 is 105 VDC with less than ½ volt peak-to-peak ripple. This 4 Kc ripple could easily be reduced further with increased filtering. The overall DC to DC efficiency for this circuit is about 70% with 85 watts output and 120 watts input.

Figure 9.49 shows the SCR waveforms in the 2 Kc inverter and Figure 9.50 shows the waveforms of the feedback diodes.



SCR Waveforms in 2 Kc Inverter
Figure 9.49



Feedback Diode Waveforms
Figure 9.50

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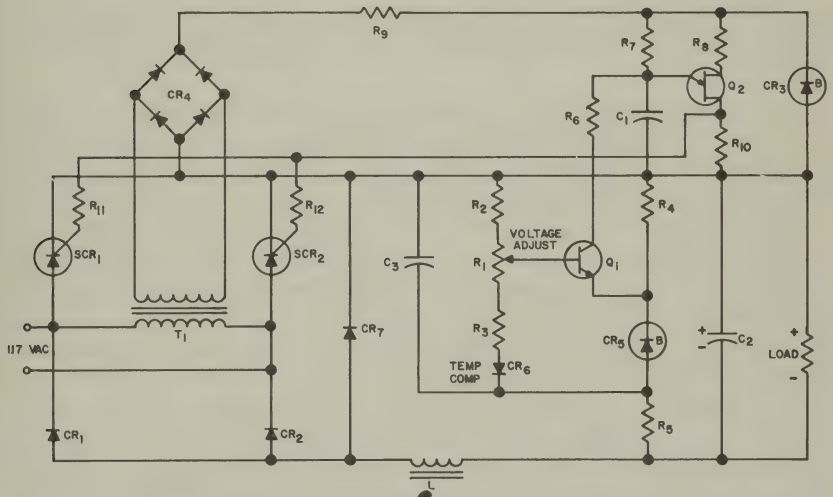
2. McMurray, W., and Shattuck, D. P. "A Silicon Controlled Rectifier Inverter with Improved Commutation," *AIEE Paper 60-1346.*
3. Corey, P. D., and Wellford, A. L. "A Controlled Rectifier Static Inverter for Intermittent Aircraft Duty," 1960 AIEE Fall General Meeting, *CP 60-1306.*

DC REGULATED POWER SUPPLIES

The SCR can be readily used as the active element in regulated power supplies to maintain constant voltage, constant current, or a combination of both. Since the switching action of the SCR is inherently quite stable, many times a more reliable supply will result with an SCR as compared to a power transistor. With the SCR there is no problem of low beta and poor starting at low temperature or high I_{co} and transformer saturation at high temperature.

10.1 PHASE-CONTROLLED REGULATED POWER SUPPLY

Figure 10.1 shows a typical phase-controlled constant voltage power supply using the 2N1847 or 2N686 SCR's.



R_1	10K, LINEAR POT	R_9	3.3K, 2 WATT	CR_3	IN1527
R_2	2.2K, 1/2 WATT	R_{10}	47 OHM, 1/2 WATT	CR_4	(4) G-E IN1695
R_3	10K, 1/2 WATT	R_{11}, R_{12}	25 OHM, 1/2 WATT	CR_5	IN468
R_4	330, 1 WATT	C_1	0.2 MFD	CR_6	G-E IN1692
R_5	2.2K, 5 WATT	C_2	15,000 MFD, 75 VOLT ELECTROLYTIC	Q_1	G-E 2N335
R_6	4.7K, 1/2 WATT	C_3	2000 MFD, 15 VOLT ELECTROLYTIC	Q_2	G-E 2N1671A
R_7	3.3K, 1/2 WATT	SCR_1, SCR_2	G-E 2N1847 OR 2N686	T_1	117/117 V ISOLATION TRANSFORMER 50 MA
R_8	330, 1/2 WATT	CR_1, CR_2, CR_7	G-E IN2156	L	10 MH, 20 AMPS.

Phase Controlled Constant Voltage Power Supply
Figure 10.1

It is designed to maintain a constant 50 volt DC output as the line voltage and line current vary over a wide range. Rated output is ½ kilowatt, although power levels up to 1½ KW at this voltage level (using 2N686's) are practical with additional filtering. With a 4 to 1 load current change and line voltage variations of ±20% around 117 volts, this circuit will hold output voltage within ±½%.

SCR_1 and SCR_2 are phase-controlled elements in a single phase bridge operating directly from the 117 VAC line. Diode rectifiers CR_1 and CR_2 form the other two legs of the bridge. The two SCR's are fired by gate signals from a common source, UJT Q_2, which operates as a relaxation oscillator synchronized by its interbase voltage supply in a manner similar to that described in Section 8.2 on the Phase Controlled AC Switch. If the feedback circuit through R_6 to the emitter of Q_2 is opened, Q_2 will fire within ten degrees of the beginning of each half cycle of the supply voltage. At this minimum firing angle, the SCR's will deliver maximum voltage to the load.

By means of Q_1 operating in the shunt transistor mode of UJT control as described in Section 4.15.2, the firing angle can be controlled electrically. The feedback signal to Q_1 is an error voltage developed from comparing a voltage on the base of Q_1 which is proportional to the output voltage, to the reference voltage across breakdown diode CR_5. If the load voltage tries to rise, more base current flows through Q_1. The resultant increase in collector current in Q_1 diverts charging current from C_1 and lengthens the time required to reach the peak point voltage of Q_2. This retards the firing angle and returns the load voltage to normal. If the load voltage starts to drop, the reverse action takes place.

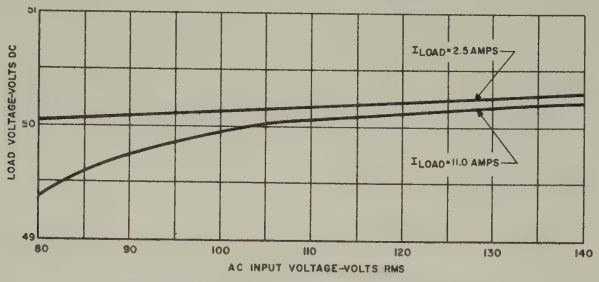
For optimum control of a constant voltage system operating on a single phase supply, the ratio of nominal input AC voltage to the regulated value of DC load voltage should be approximately 2.2. In order for the circuit to operate stably, a large value of filter capacitance C_2 is required across the load. If the ripple voltage across this capacitor becomes greater than approximately 0.1 volt, the circuit has a tendency to hunt from one-half cycle to the next. This can lead to non-symmetrical conduction during the alternate half cycles. At the expense of system response, stability can be achieved by adding capacitance C_3 in the relatively high impedance feedback circuit. For optimum response and stability, all filtering should be incorporated in the main load circuit only.

The variation of forward voltage drop with temperature in CR_6 compensates for the temperature effects on the base to emitter voltage of Q_1. If a germanium transistor is used for Q_1, a 1N91 should be used for CR_6. CR_7 acts as a free-wheeling diode to maintain current in the load and filter choke when the SCR's are both blocking. It contributes to overall circuit stability.

A voltage supply of at least 100 volts is desirable for the output of CR_4. Accordingly, when lower AC supply voltages are used, the transformer ratio of T_1 should be chosen so that its secondary voltage is approximately 117 volts.

The voltage regulating performance of the circuit in Figure 10.1 is shown in Figure 10.2 at two levels of load current. Output ripple voltage with the indicated filter parameters is less than one volt under the worst combination of high input voltage and heaviest load. Additional filtering or the addition of a

power transistor stage in series with the load could be expected to improve both the ripple and regulation characteristics if this is necessary. At 10 amperes load and 110 volts AC line input, overall circuit efficiency is 85%.

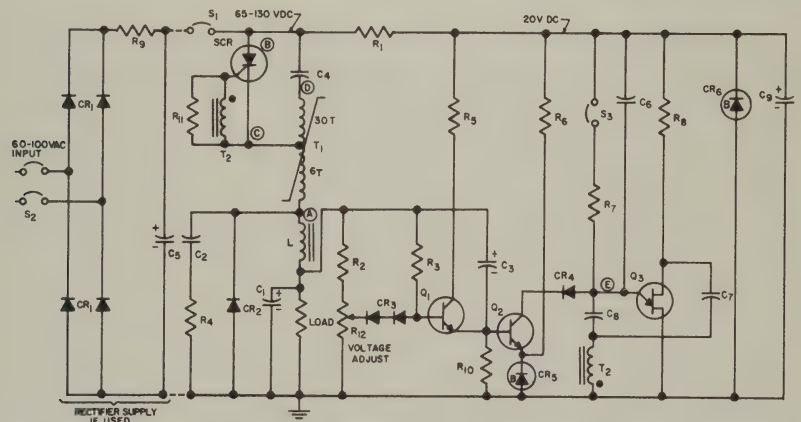


Regulation Curves of Constant Voltage Power Supply
Figure 10.2

A simple overcurrent protection scheme for this type of circuit is discussed in Section 11.8.

10.2 CHOPPER-CONTROLLED REGULATED POWER SUPPLY

Figure 10.3 shows the circuit of a power supply based on the Morgan chopper arrangement.



R_1 — 1500Ω, 10W	C_1 — 12000 mfd, 40V ELECTROLYTIC	CR_2 — G.E. IN2158
R_2 — 250Ω, 2W	C_2 — 0.1mfd, 200 VDC	CR_3 — G.E. IN91 (TWO REQUIRED)
R_3 — 20K, .5W	C_3 — 16mfd, 250 VDC ELECTROLYTIC	CR_4 — G.E. IN536
R_4 — 25Ω, 10W	C_4 — 4mfd, 200 VDC, EXTENDED FOIL, G.E. 28F612	CR_5 — IN469-6V BREAKDOWN DIODE (200mw)
R_5 — 2200Ω, .5W	C_5 — 1400mfd, 250 VDC ELECTROLYTIC	CR_6 — IN1527—20V BREAKDOWN DIODE (1W)
R_6 — 1200Ω, 1W	C_6 — 0.15mfd, 200 VDC	Q_1, Q_2 — G.E. 2N635
R_7 — 2700Ω, .5W	C_7 — 0.2 mfd, 200 VDC	Q_3 — G.E 2N1671A
R_8 — 330Ω, .5W	C_8 — 0.1mfd, 200 VDC	T_1 — MAGNETICS, INC. 50001-2A ORTHONOL CORE WITH TWO WINDINGS OF #14AWG. WIRE AS INDICATED ON DIAGRAM
R_9 — .05Ω, 10W	C_9 — 50 mfd, 50 VDC ELECTROLYTIC	T_2 — SPRAGUE 31Z204 PULSE TRANSFORMER
R_{10} — 4700Ω, .5W	SCR — G.E. C40C	L — 10 mh, 10 amp. CHOKE
R_{11} — 47Ω, .5W	CR_1 — G.E. 4JA621ICBIABI	
R_{12} — 250Ω, 2W LINEAR POT.		

28 VDC 10 Amp Regulated Power Supply
Figure 10.3

It is capable of operating directly from a DC line, or from an AC supply through use of a rectifier and rough filter as shown on the left hand side of the diagram. This circuit has several advantages over the AC phase controlled circuit discussed previously in addition to being able to operate from a DC source. It is capable of operating stably over a wide range of frequency of the AC input. Because the chopping circuit operates in the 500 to 2000 cps range, this circuit also has inherently faster response than a phase-controlled circuit operating at normal line frequencies. Filter requirements are less, and the AC supply sees essentially a unity power factor load with little distortion effects on the line voltage as compared to phase-controlled circuits.

Basic operation of this circuit is as follows: SCR is connected across the DC bus in series with the load, a saturating current transformer T_1, and filter choke L. The bus receives its power either directly from a DC system or from an AC source through rectifier CR_1 and filter C_5. SCR acts as a switch in series with the load, applying pulses of approximately constant width to the load. The repetition rate of these pulses is controlled by the feedback circuit on the right hand side of the diagram and thus regulates the average voltage being applied to the load. Choke L, in conjunction with capacitor C_1 and free-wheeling diode CR_2, filter the pulses so that essentially pure DC current flows through the load. Since the power control device (SCR) is operating in a switching mode, this is basically a "lossless" method of regulating power although some losses do exist due to the forward conduction drop through SCR and the filter choke and due to switching and control losses. Efficiency is inherently high compared to variable resistance techniques using tubes or transistors in series with the load.

The switching action of SCR in the Morgan circuit is discussed in Chapter 9, Section 9.20. When SCR is fired by a gate pulse from T_2, power is delivered to the load, and the bottom plate of C_4 is charged positive with respect to its top plate by the autotransformer action of T_1. When T_1 saturates, the voltage on C_4 is applied to SCR in the inverse direction, reverse biasing it for a period of time dependent on the load current and the value of C_4. This interrupts the flow of current from the DC supply until SCR is again triggered. In the interim, however, current continues to flow in the load through CR_2 due to the inductive effect of choke L and the energy stored in C_1.

Waveshapes across the major elements in the power circuit are shown in Figure 10.4 at a DC bus voltage of 90 volts and an average load current of 1.4 amperes. The time interval t_o indicated on the voltage waveform across SCR is the turn-off time. Under no circumstances must this time interval become less than 12 microseconds or so-called "shoot-through" may result. "Shoot-through" occurs when an SCR is not reverse biased for a sufficient time to recover its forward blocking ability after having conducted load current. In this event SCR will remain turned on, since T_1 will not be reset and C_4 will not build up a negative commutating voltage. The SCR will remain on indefinitely, thereby applying the full supply voltage to the load. By using the component values indicated in Figure 10.3, an ample safety factor in turn off time is available up to 10 amperes load current and under all likely load variations and switching conditions. Overcurrent protection schemes of the type described in Chapter 11

gate circuits. Because they are rated for 120-volt and 240-volt line operation, triacs are readily adaptable for the control of power to any equipment being operated directly from ac power lines. When used for ac power control, triacs add new functions to many designs, improve performance, and provide maximum efficiency and high reliability. This Note describes triac operating characteristics and provides guidance in the use of triacs for specific applications.

Principal Voltage-Current Characteristic Diagram

Fig. 1 shows the principal voltage-current characteristic of a triac. This curve shows the current through the triac as a function of the voltage applied between main terminals Nos. 1 and 2. In quadrant I, the voltage on main terminal No. 2 is positive with respect to main terminal No. 1; in quadrant III, the voltage on main terminal No. 2 is negative with respect to main terminal No. 1. When a positive voltage is applied to main terminal No. 2, as shown by the curve in quadrant I, a point is reached, called the breakover voltage V_{BO}, at which the device switches from a high-impedance state to a low-impedance state. The current can then be increased through the triac with only a small increase in voltage across the device. The triac remains in the ON state until the current through the main terminals drops below a value, called the holding current, which cannot maintain the breakover condition. The triac

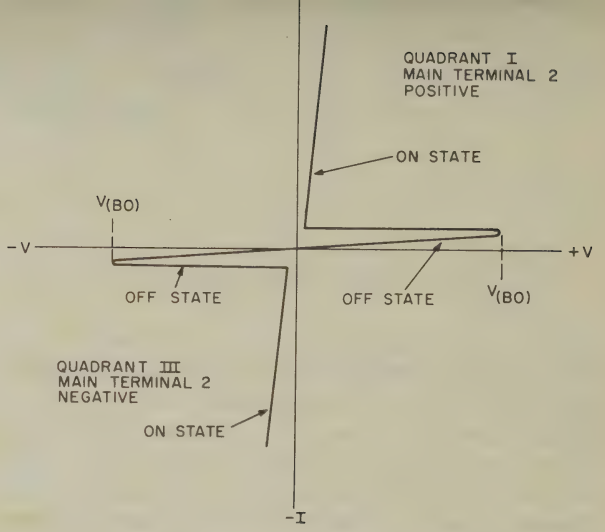


Fig. 1 — Triac principal voltage-current characteristics.

Gate Characteristics

When a trigger current is applied to the gate terminal of a triac, the breakover voltage is reduced. After the triac is triggered, the current flow through the main terminals is independent of the gate signal and the triac remains in the ON state until the principal current is reduced below the

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RCA Application Note

AN-3697

TRIAC POWER-CONTROL APPLICATIONS

by

J. V. YONUSHKA

In the control of ac power by means of semiconductor devices, emphasis has been placed upon limiting the complexity of the circuits involved, the cost of the system, and the over-all package size. With the development of the bidirectional triode thyristor, commonly known as the triac, all of these goals can be achieved. A triac can perform the functions of two SCR's for full-wave operation and can easily be triggered in either direction to simplify gate circuits. Because they are rated for 120-volt and 240-volt line operation, triacs are readily adaptable for the control of power to any equipment being operated directly from ac power lines. When used for ac power control, triacs add new functions to many designs, improve performance, and provide maximum efficiency and high reliability. This Note describes triac operating characteristics and provides guidance in the use of triacs for specific applications.

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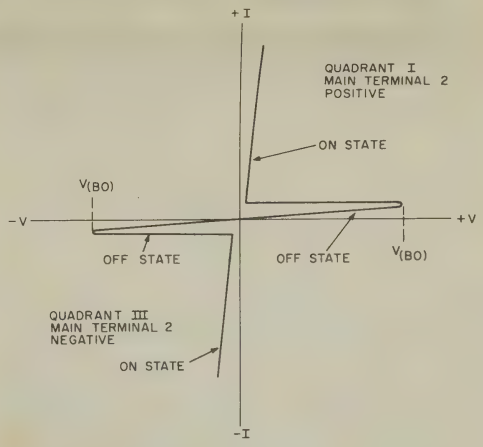


Fig. 1 — Triac principal voltage-current characteristics.

Gate Characteristics

When a trigger current is applied to the gate terminal of a triac, the breakover voltage is reduced. After the triac is triggered, the current flow through the main terminals is independent of the gate signal and the triac remains in the ON state until the principal current is reduced below the

holding-current level. The triac has the unique capability of being triggered by either a positive or a negative gate signal regardless of the voltage polarity across the main terminals of the device. Fig. 2 illustrates the triggering mechanism and current flow within a triac. The gate trigger polarity is always referenced to main terminal No. 1. The potential difference between the two terminals is such that gate current flows in the direction indicated by the dotted arrow. The polarity symbol at main terminal No. 2 is also referenced to main terminal No. 1. The semiconductor materials between the various junctions within the pellet are labeled p and n to indicate the type of majority-carrier concentrations within the material.

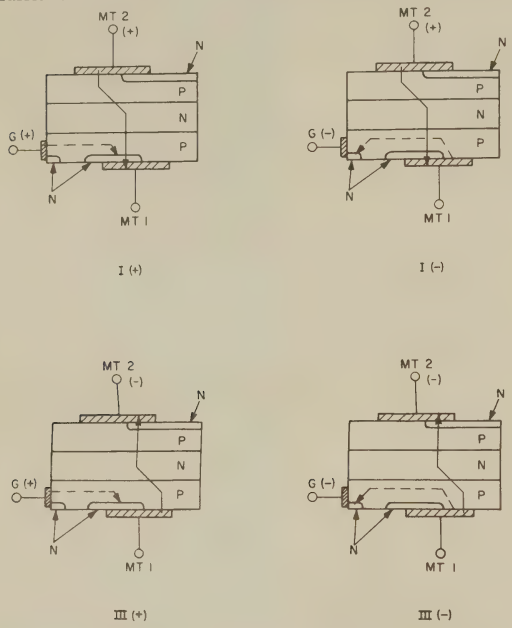


Fig. 2 — Current flow in a triac.

For the various operating modes, the polarity of the voltage on main terminal No. 2 with respect to main terminal No. 1 is given by the quadrant in which the triac operates, (either I or III) and the polarity of the gate signal used to trigger the device is given by the proper symbol next to the operating quadrant. For the I (+) operating mode, therefore, main terminal No. 2 and the gate are both positive with respect to main terminal No. 1. Initial gate current flows into the gate terminal, through the p-type layer, across the junction into the n-type layer, and out main terminal No. 1, as shown by the dotted arrow. As gate current flows, current multiplication occurs and the regenerative action within the pellet switches the triac to its ON state. Because of the polarities indicated between the main terminals, the principal current flows through the pnpn structure as shown by the solid arrow. Similarly, for the other three operating modes, the initial gate current flow is shown by the dotted arrow, and principal current flow through the main terminals is shown by the solid arrow.

Because the principal current influences the gate trigger current, the magnitude of the current required to trigger the triac differs for each mode. The operating modes in which the principal current is in the same direction as the gate current require less gate trigger current, while modes in which the principal current is in opposition to the gate current require more gate trigger current.

Like many other semiconductor parameters, the magnitude of the gate trigger current and voltage varies with the junction temperature. As the thermal excitation of carriers within the semiconductor increases, the increase in leakage current makes it easier for the device to be triggered by a gate signal. Therefore, the gate becomes more sensitive in all operating modes as the junction temperature increases. Conversely, if the triac is to be operated at low temperatures, sufficient gate trigger current must be provided to assure triggering of all devices at the lowest operating temperature expected in any particular application. Variations of gate trigger requirements are given in the data sheets for individual triacs.

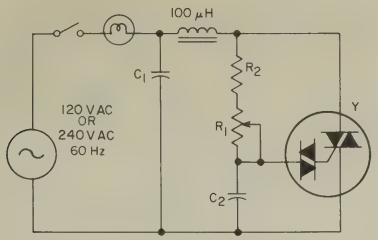
Light Control

Because the light output of an incandescent lamp depends upon the voltage impressed upon the lamp filament, changes in the lamp voltage vary the brightness of the lamp. When ac source voltages are used, a triac can be used in series with an incandescent lamp to vary the voltage to the lamp by changing its conduction angle; i.e., the portion of each half cycle of ac line voltage in which the triac conducts to provide voltage to the lamp filament. The triac, therefore, is very attractive as a switching element in light-dimming applications.

To switch incandescent-lamp loads reliably, a triac must be able to withstand the inrush current of the lamp load. The inrush current is a result of the difference between the cold and hot resistance of the tungsten filament. The cold resistance of the tungsten filament is much lower than the hot resistance. The resulting inrush current is approximately 12 times the normal operating current of the lamp.

The simplest circuit that can be used for light-dimming applications is shown in Fig. 3 and uses a trigger diode in series with the gate of a triac to minimize the variations in gate trigger characteristics. In applications where space is premium the RCA-40431 or RCA-40432 may be used because it combines both functions in a single package. Changes in the resistance in series with the capacitor change the conduction angle of the triac. Because of its simplicity, this circuit can be packaged in confined areas where space is at a premium.

The capacitor in the circuit of Fig. 3 is charged through the control potentiometer and the series resistance. The series resistance is used to protect the potentiometer by limiting the capacitor charging current when the control potentiometer is at its minimum resistance setting. This resistor may be eliminated if the potentiometer can withstand the peak charging current until the triac turns on. The trigger diode conducts when the voltage on the capacitor reaches the diode breakover voltage. The capacitor then discharges through the trigger diode to produce a current pulse of sufficient amplitude and width to trigger the triac. Because the triac can be triggered with either



	120VAC, 60Hz	240VAC, 60Hz
R_1	200kΩ, ½W	250kΩ, 1W
R_2	3.3kΩ, ½W	4.7kΩ, ½W
C_1	0.1μF, 200V	0.1μF, 400V
C_2	0.1μF, 100V	0.1μF, 100V
Y	RCA 40431	RCA 40432

Fig. 3 — Single-time-constant light-dimmer circuit.

polarity of gate signal, the same operation occurs on the opposite half-cycle of the applied voltage. The triac, therefore, is triggered and conducts on each half-cycle of the input supply voltage.

The interaction of the RC network and the trigger diode results in a hysteresis effect when the triac is initially triggered at small conduction angles. The hysteresis effect is characterized by a difference in the control potentiometer setting when the triac is first triggered and when the circuit turns off. Fig. 4 shows the interaction between the RC network and the trigger diode to produce the hysteresis effect. The capacitor voltage and the ac line voltage are shown as solid lines. As the resistance in the circuit is decreased from its maximum value, the capacitor voltage reaches a value which fires the trigger diode. This point is designated A on the capacitor-voltage wave-shape. When the trigger diode fires, the capacitor discharges and triggers the triac at an initial conduction angle θ_1. During the forming of the gate trigger pulse, the capacitor voltage drops suddenly. The charge on the capacitor is smaller than when the trigger diode did not conduct. As a result of the different voltage conditions on the capacitor, the breakover voltage of the trigger diode is reached earlier in the next half-cycle. This point is labeled point B on the capacitor-voltage waveform. The conduction angle θ_2 corresponding to point B is greater than θ_1. All succeeding conduction angles

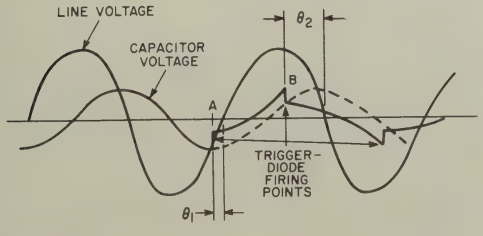
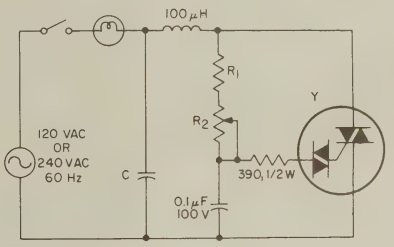


Fig. 4 — Waveforms showing interaction of control network and trigger diode.

are equal to θ_2 in magnitude. When the circuit resistance is increased by a change in the potentiometer setting the triac is still triggered, but at a smaller conduction angle. Eventually, the resistance in series with the capacitance becomes so great that the voltage on the capacitor does not reach the breakover voltage of the trigger diode. The circuit then turns off and does not turn on until the circuit resistance is again reduced to allow the trigger diode to be fired. The hysteresis effect makes the voltage load appear much greater than would normally be expected when the circuit is initially turned on.

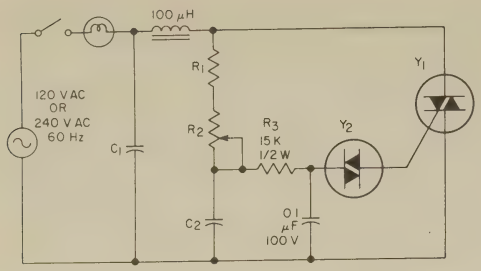
The hysteresis effect can be reduced by use of a resistor in series with the trigger diode and gate, as shown in Fig. 5. The series resistor slows down the discharge of the capacitor through the trigger diode. Consequently, the capacitor does not lose as much charge while triggering the triac, and produces a smaller hysteresis effect. As a result of the slower capacitor discharge through the trigger diode, however, the peak magnitude of the gate trigger current pulse is reduced. The size of the trigger capacitor may have to be increased to compensate for the reduction of the gate trigger current pulse.



	120VAC, 60Hz	240VAC, 60Hz
R_1	3.3kΩ, ½W	4.7kΩ, ½W
R_2	200kΩ, ½W	250kΩ, 1W
C	0.1μF, 200V	0.1μF, 400V
Y	RCA 40431	RCA 40432

Fig. 5 — Single-time-constant light-dimmer circuit with series gate resistor.

The double-time-constant circuit in Fig. 6 improves on the performance of the single-time-constant control circuit. This circuit uses an additional RC network to extend the phase angle so that the triac can be triggered at small conduction angles. The additional RC network also minimizes the hysteresis effect. Fig. 7 shows the voltage waveforms for the ac supply and the trigger capacitor of the circuit of Fig. 6. Because of the voltage drop across R_3, the input capacitor C_2 charges to a higher voltage than the trigger capacitor C_3. When the voltage on C_3 reaches the breakover voltage of the trigger diode, the diode conducts and causes the capacitor to discharge and produce the gate current pulse to trigger the triac. After the trigger diode turns off, the charge on C_3 is partially restored by



	120VAC, 60Hz	240VAC, 60Hz
R_1	2.2kΩ, ½W	3.3kΩ, ½W
R_2	100kΩ, ½W	200kΩ, 1W
C_1 C_2	0.1μF, 200V	0.1μF, 400V
Y_1	RCA 40485 } or 40431	RCA 40486 } or 40432
Y_2	RCA 40583 }	RCA 40583 }

Fig. 6 — Double-time-constant light-dimmer circuit.

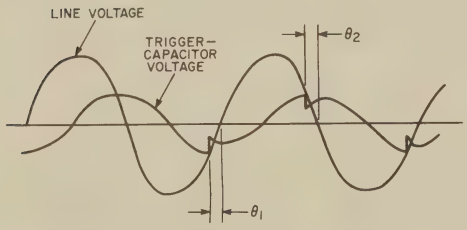
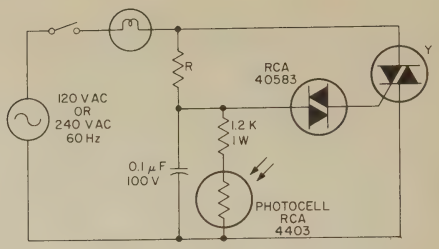


Fig. 7 — Voltage waveforms of double-time-constant control circuit.

the charge from the input capacitor C_2. The partial restoration of charge on C_3 results in better circuit performance with a minimum of hysteresis.

Light-Activated Control

For applications requiring a light-activated circuit, such as outdoor lights or indoor night lights, the circuit shown in Fig. 8 can be employed. Although this circuit functions in the same manner as the light-dimming circuit, the photocell controls its operation. When the light impinges on the surface of the photocell, the resistance of the photocell becomes low and prevents the voltage on the trigger capacitor from increasing to the breakover voltage of the trigger diode. The circuit is then inoperative. When the light source is removed, the photocell becomes a high resistance. The voltage on the trigger capacitor then increases to the breakover voltage of the trigger diode and causes the diode to fire. The trigger pulse formed by the capacitor discharge through the trigger diode makes the triac conduct and operates the circuit. The triac continues to be triggered on each half-cycle and supplies power to the load as long as the resistance of the photocell is high. When light again impinges on the surface of the photocell

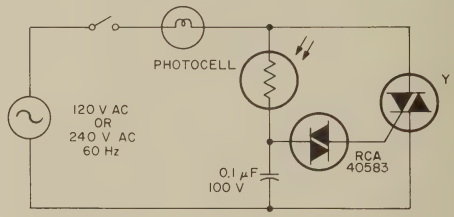


	120VAC, 60Hz	240VAC, 60Hz
R	15kΩ, 2W	30kΩ, 3W
Photocell	RCA 4403	RCA 4453
Y	RCA 40485	RCA 40486

Fig. 8 — Light Controlled Turn-Off Circuit.

and reduces its resistance, the voltage on the capacitor can no longer reach the breakover voltage of the trigger diode, and the circuit turns off.

For applications requiring operation when light impinges on the surface of the photocell, the circuit of Fig. 9 is recommended. In this circuit, low resistance of the photocell allows the triac to be triggered on. When light is removed from the photocell the increased resistance of the photocell prevents the triac from being triggered and renders the circuit inoperative.



	120VAC, 60Hz	240VAC, 60Hz
Photocell	RCA 4403	RCA 4453
Y	RCA 40485	RCA 40486

Fig. 9 — Light Controlled Turn-On Circuit.

Radio Frequency Interference

The fast switching action of triacs when they turn on into resistive loads causes the current to rise to the instantaneous value determined by the load in a very short period of time. This fast switching action produces a current step which is largely composed of higher-harmonic frequencies that have an amplitude varying inversely as the frequency. In phase-control applications, such as light dimming, this current step is produced on each half-cycle of the input voltage. Because the switching occurs many times a second, a noise pulse is generated into frequency-sensitive devices

such as AM radios and causes annoying interference. The amplitude of the higher frequencies in the current step is of such low levels that they do not interfere with television or FM radio.

There are two basic types of radio-frequency interference (RFI) associated with the switching action of triacs. One form, radiated RFI, consists of the high-frequency energy radiated through the air from the equipment. In most cases, this radiated RFI is insignificant unless the radio is located very close to the source of the radiation.

Of more significance is conducted RFI which is carried through the power lines and affects equipment attached to the same power lines. Because the composition of the current waveshape consists of higher frequencies, a simple choke placed in series with the load slows down the current rise time and reduces the amplitude of the higher harmonics. To be effective, however, such a choke must be quite large. A more effective filter, and one that has been found adequate for most light-dimming applications is shown in Fig. 10. The LC filter provides adequate attenuation of the high-frequency harmonics and reduces the noise interference to a low level.

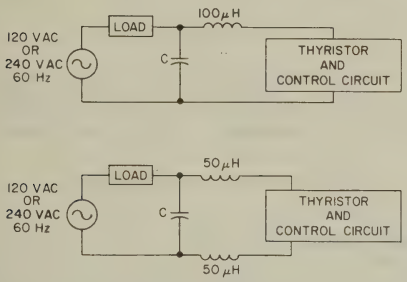


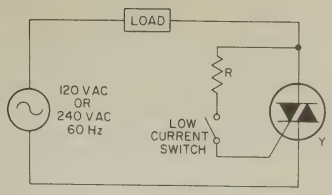
Fig. 10 — RFI-suppression networks: at 120 VAC, C = 0.1 μF, 200 V; at 240 VAC, C = 0.1 μF, 400 V.

Motor Control

Triacs can be used very effectively to apply power to motors and perform such functions as speed control, reversing, full power switching, or any other desired operating condition that can be obtained by a switching action. Because most motors are line-operated, the triac can be used as a direct replacement for electro-mechanical switches. In proper control circuits, triacs can change the operating characteristics of motors to obtain many different speed and torque curves.

A very simple triac static switch for control of ac motors is shown in Fig. 11. The low-current switch controlling the gate trigger current can be any type of transducer, such as a pressure switch, a thermal switch, a photocell, or a magnetic reed relay. This simple type of circuit allows the motor to be switched directly from the transducer switch without any intermediate power switch or relay.

For dc control, the circuit of Fig. 12 can be used. By use of the dc triggering modes, the triac can be directly triggered from transistor circuits by either a pulse or continuous signal.



	120VAC, 60Hz	240VAC, 60Hz
R	1kΩ, ½W	2kΩ, ½W
Y	RCA 40429	RCA 40430

Fig. 11 — Simple Triac Static Switch.

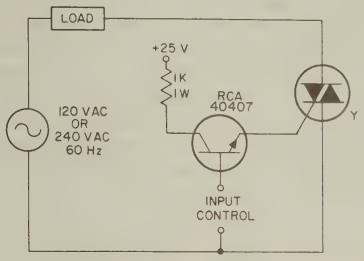
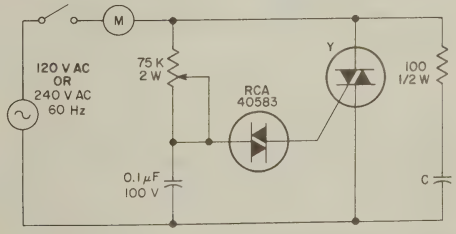


Fig. 12 — AC Triac Switch Control From DC Input: at 120 VAC, Y = RCA 40429; at 240 VAC, Y = RCA 40430.

Induction Motor Controls

Fig. 13 shows a single-time-constant circuit which can be used as a satisfactory proportional speed control for some applications and with certain types of induction motors, such as shaded pole or permanent split-capacitor motors, when the load is fixed. This type of circuit is best suited to applications which require speed control in the medium to full-power range. It is specifically useful in applications such as fans or blower-motor controls, where a small change in motor speed produces a large change in



	120VAC, 60Hz	240VAC, 60Hz
C	0.22μF, 200V	0.22μF, 400V
Y	RCA 40429	RCA 40430

Fig. 13 — Induction motor control.

air velocity. Caution must be exercised if this type of circuit is used with induction motors because the motor may stall suddenly if the speed of the motor is reduced below the drop-out speed for the specific operating condition determined by the conduction angle of the triac. Because the single-time-constant circuit cannot provide speed control of an induction motor load from maximum power to full off, but only down to some fraction of the full-power speed, the effects of hysteresis described previously are not present. Speed ratios as high as 3:1 can be obtained from the single-time-constant circuit used with certain types of induction motors.

Because motors are basically inductive loads and because the triac turns off when the current reduces to zero, the phase difference between the applied voltage and the device current causes the triac to turn off when the source voltage is at a value other than zero. When the triac turns off, the instantaneous value of input voltage is applied directly to the main terminals of the triac. This commutating voltage may have a rate of rise which can retrigger the triac. The commutating dv/dt can be limited to the capability of the triac by use of an RC network across the device, as shown in Fig. 13. The current and voltage waveshapes for the circuit are shown in Fig. 14 to illustrate the principle of commutating dv/dt.

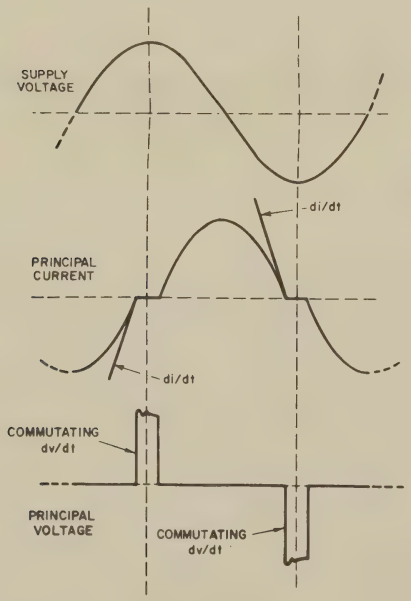
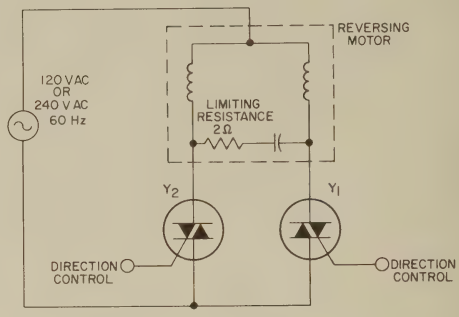


Fig. 14 — Waveshapes of commutating dv/dt characteristics.

Reversing Motor Control

In many industrial applications, it is necessary to reverse the direction of a motor, either manually or by means of an auxiliary circuit. Fig. 15 shows a circuit which uses two triacs to provide this type of reversing motor control. The reversing switch can be either a manual switch or an electronic switch used with some type of sensor to reverse the direction of the motor. A resistance is added in series with the capacitor to limit capacitor discharge current to a safe value whenever both triacs are conducting simultaneously. Simultaneous conduction can easily occur because the triggered triac remains in conduction after the gate is disconnected until the current reduces to zero. In the meantime, the nonconducting-triac gate circuit can be energized so that both triacs are ON and large loop currents are set up in the triacs by the discharge of the capacitor.

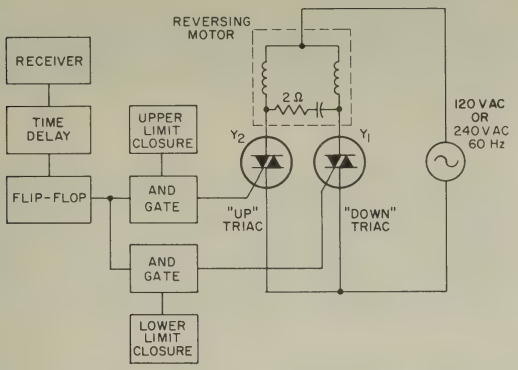


	120VAC, 60Hz	240VAC, 60Hz
Y_1	RCA 40485	RCA 40486
Y_2	RCA 40485	RCA 40486

Fig. 15 — Reversing motor control.

Electronic Garage-Door System

The triac motor-reversing circuit can be extended to electronic garage-door systems which use the principle of motor reversing for garage-door direction control. The system contains a transmitter, a receiver, and an operator to provide remote control for door opening and closing. The block diagram in Fig. 16 shows the functions required for a complete solid-state system. When the garage door is closed, the gate drive to the DOWN triac is disabled by the lower-limit closure and the gate drive to the UP triac is inactive because of the state of the flip-flop. If the transmitter is momentarily keyed, the receiver activates the time-delay monostable multivibrator so that it then changes the flip-flop state and provides continuous gate drive to the UP triac. The door then continues to travel in the UP direction until the upper-limit switch closure disables gate drive to the UP triac. A second keying of the transmitter provides the DOWN triac with gate drive and causes the door to travel in the DOWN direction until the gate drive is disabled by the lower limit closure. The time in which the monostable multivibrator is active should override normal transmitter keying for the purpose of eliminating erroneous firing. A feature of this system is that, during travel, transmitter keying provides motor reversing independent of the upper- or lower-limit closures. Additional features, such as obstacle obstructions, manual control, or time delay for overhead garage lights can be achieved very economically.

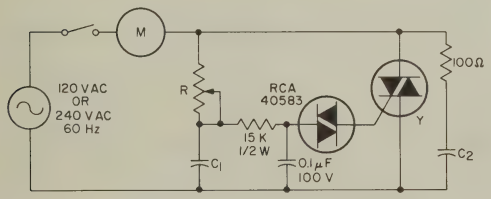


	120VAC, 60Hz	240VAC, 60Hz
Y_1	RCA 40485	RCA 40486
Y_2	RCA 40485	RCA 40486

Fig. 16 — Block diagram for remote-control solid-state garage-door system.

Universal Motor Speed Controls

In applications in which the hysteresis effect can be tolerated or which require speed control primarily in the medium to full-power range, a single-time-constant circuit such as that shown in Fig. 13 for induction motors can also be used for universal motors. However, it is usually desirable to extend the range of speed control from full-power ON to very low conduction angles. The double-time-constant circuit shown in Fig. 17 provides the delay necessary to trigger the triac at very low conduction angles with a minimum of hysteresis, and also provides practically full power to the load at the minimum-resistance position of the control potentiometer. When this type of control circuit is used, an infinite range of motor speeds can be obtained from very low to full-power speeds.



	120VAC, 60Hz	240VAC, 60Hz
R	100kΩ, ½W	200kΩ, 1W
C_1	0.1μF, 200V	0.1μF, 400V
C_2	0.22μF, 200V	0.22μF, 400V
Y	RCA 40429	RCA 40430

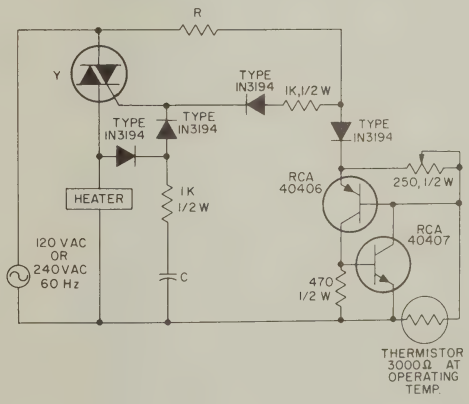
Fig. 17 — Universal Motor Speed Control.

Heat Control

There are three general categories of solid-state control circuits for electric heating elements: on-off control, phase control, and porportional control using integral-cycle synchronous switching. Phase-control circuits, such as those used for light dimming are very effective and efficient for electric heat control except for the problem of RFI. In higher-power applications, the RFI is of such magnitude that suppression circuits to minimize the interference become quite bulky and expensive.

An on-off circuit for the control of resistance-heating elements is shown in Fig. 18. The circuit also provides synchronous switching close to the beginning of the zero-voltage crossing of the input voltage to minimize RFI. The thermistor controls the operation of the two-transistor regenerative switch, which, in turn, controls the operation of the triac. When the temperature being controlled is low, the resistance of the thermistor is high and the regenerative switch is OFF. The triac is then triggered directly from the line on positive half-cycles of the input voltage. When the triac triggers and applies voltage to the load, the capacitor is charged to the peak value of the input voltage. The capacitor discharges through the triac gate to trigger the triac on the opposite half-cycle. The diode-resistor-capacitor "slaving" network triggers the triac on negative half-cycles of the ac input voltage after it is triggered on the positive half-cycle to provide integral cycles of ac power to the load.

When the temperature being controlled reaches the desired value as determined by the thermistor, the transistor regenerative switch conducts at the beginning of the positive input-voltage cycle to shunt the trigger current away from the triac gate. The triac does not conduct as long as the resistance of the thermistor is low enough to make the transistor regenerative switch turn on before the triac can be triggered.



	120VAC, 60Hz	240VAC, 60Hz
R	2.2kΩ, 5W	3.9kΩ, 5W
C	0.5μF, 200V	0.5μF, 400V
Y	RCA 40575	RCA 40576

Fig. 18 — Synchronous switching on-off heat controller.

Proportional Integral-Cycle Control

On-off controls have only two levels of power input to the load. The heating coils are either energized to full power or are at zero power. Because of thermal time constants, on-off controls produce a cyclic action which alternates between thermal overshoots and undershoots with poor resolution.

This disadvantage is overcome and RFI is minimized by use of the concept of integral-cycle proportional control with synchronous switching. In this system, a time base is selected and the on-time of the triac is varied within the time base. The ratio of the on-to-off time of the triac within this time interval depends upon the power required to the heating elements to maintain the desired temperature. Fig. 19 shows the on-off ratio of the triac. Within the time period, the on-time varies by an integral number of cycles from full ON to a single cycle of input voltage.

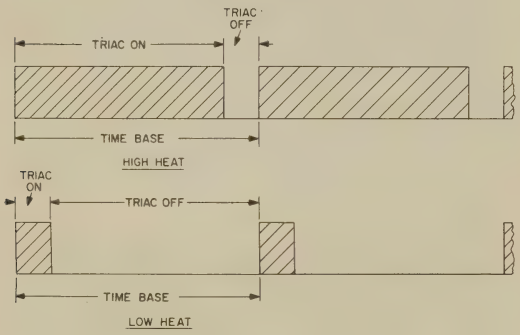


Fig. 19 — Triac duty cycle.

One method of achieving integral cycle proportional control is to use a fixed-frequency sawtooth generator signal which is summed with a dc control signal. The sawtooth generator establishes the period or time base of the system. The dc control signal is obtained from the output of the temperature-sensing network. The principle is illustrated in Fig. 20. As the sawtooth voltage increases, a level is reached which turns on power to the heating elements. As the temperature at the sensor changes, the dc level shifts accordingly and changes the length of time that the power is applied to the heating elements within the established time.

When the demand for heat is high, the dc control signal is high and little power is supplied continuously to the heating elements. When the demand for heat is completely satisfied, the dc control signal is low and no power is supplied to the heating elements. Usually a system using this principle operates continuously somewhere between full ON and full OFF to satisfy the demand for heat.

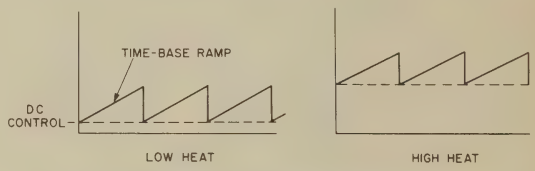
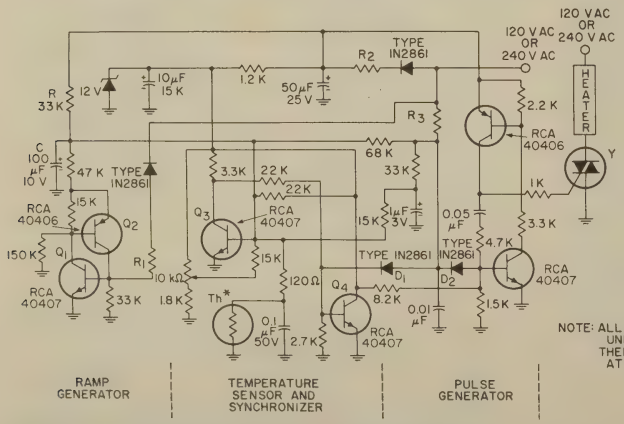


Fig. 20 — Proportional-controller waveshapes.

A proportional integral-cycle heat control system is shown in Fig. 21. The ramp voltage is generated by charging of capacitor C through resistor R for approximately 2 seconds for the values shown. The length of the ramp is determined by the voltage magnitude required to trigger the regenerative switch consisting of Q_1 and Q_2. The temperature sensor consisting of Q_3 and Q_4, together with the controlling thermistor Th, establishes a voltage level at the base of Q_3 which depends upon the resistance value of the thermistor. Q_3 and Q_4 form a bistable multivibrator. The state of the multivibrator depends upon the base bias of Q_3. When Q_3 is conducting, Q_4 is cut off. The pulse generator is energized and generates pulses to trigger the triac. The output of the pulse generator is synchronized to the line voltage on the negative half-cycle by D_2 and R_3 and on the positive half-cycle by D_1 and R_3. The pulses are, therefore, generated at the zero-voltage crossings and trigger the triacs into conduction at only these points.



NOTE: ALL RESISTORS 1/2 W, ±10% UNLESS OTHERWISE SPECIF. THERMISTOR APPROX. 3000 Ω AT OPERATING TEMP.

	120VAC, 60Hz	240VAC, 60Hz
R_1	60kΩ, ½W	120kΩ, ½W
R_2	3.3kΩ, 2W	5.6kΩ, 2W
R_3	33kΩ, ½W	57kΩ, ½W
Y	2N5441 or 2N5444	2N5442 or 2N5445

Fig. 21 — Proportional integral-cycle heat controller.

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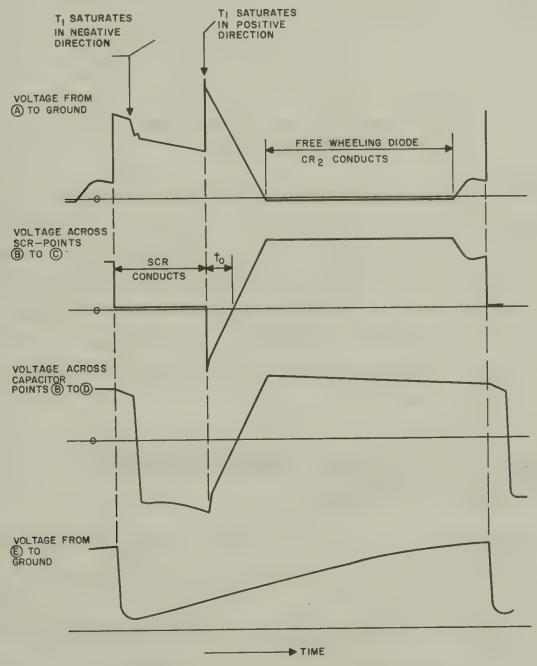
can be incorporated if there is a possibility of short circuits or overloads.

The feedback control of the output voltage relies on a UJT relaxation oscillator Q_3 to develop firing pulses for the gate of SCR. These pulses are coupled to the gate through T_2, the primary of which is in series with the emitter capacitor C_8 of the UJT oscillator. With the voltage adjust pot, R_{12}, at its bottom position, no feedback signal is present. Under these conditions, the UJT oscillates at its maximum rate, approximately 2 Kc per second, and maximum voltage is applied to the load. As the arm of R_{12} is moved up so that its portion of the load voltage exceeds the reference voltage of CR_5, transistors Q_1 and Q_2 will start to conduct and part of the current flowing down through R_7 is then diverted from C_8 through CR_4 and the collector of Q_2. C_8 then takes longer to charge to the peak point voltage of Q_3, and the repetition rate of the UJT oscillator and SCR decreases. Load voltage is thereby decreased also. For a given setting of R_{12} so that the load voltage is at or near the design objective of 28 volts, the feedback circuit will regulate the repetition rate so as to maintain load voltage constant with variations in supply voltage and load current.

The control circuit derives its 20 volt supply from the main DC supply through dropping resistor R_1 and breakdown diode GR_6. C_3 transmits a supplementary feedback signal which is a function of the rate of change of load voltage. This signal stabilizes the overall performance and increases the speed of response. It also reduces the supply frequency ripple content of the voltage across the load.

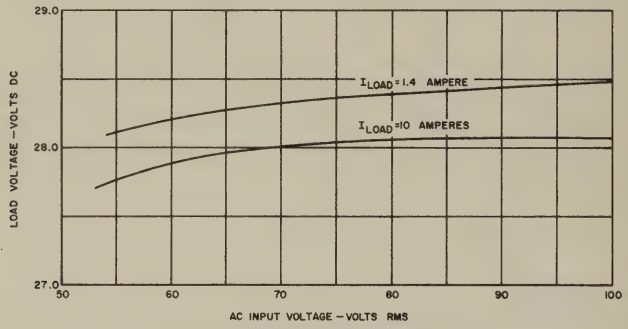


Voltage Waveforms in Regulated Power Supply
Figure 10.4

The two diodes, CR_3, compensate for temperature variations in the base to emitter voltage drop of Q_1 and Q_2. If silicon transistors are used instead of germanium for Q_1 and Q_2, CR_3 should consist of two 1N1692 diodes.

R_9 is a surge resistor designed to protect CR_1 against excessive inrush current to C_5 when the AC line switch is closed. If an equivalent impedance already exists in the AC line, this resistor can be omitted. Starting and stopping of the circuit can be accomplished either by operating switch S_1, S_2, or S_3.

Regulation performance of this circuit is indicated in Figure 10.5. Output voltage is maintained within ±1% with a 7 to 1 load current change and input voltage variation from 60 to 100 VAC. Maximum ripple voltage across the load over this range was 70 millivolts RMS. With 70v RMS input and a load of 10 amps, the efficiency of the inverter (including control but not the rectifier supply) was 86%. At 1.4 amp. load at the same voltage input, efficiency was 61%. Overall performance on a pure DC bus was equal or superior to the above figures.



DC Voltage Regulator Performance
Figure 10.5

On an abrupt change of load from 1.4 to 10 amperes, the load voltage dipped approximately 0.2 volt and returned to normal within 20 milliseconds. An abrupt drop from 10 to 1.4 amperes caused an overshoot of approximately 1 volt and a return to normal within 50 milliseconds. Load voltage variation over a two-hour period was less than 0.2 volt. All tests were made at 25°C. An AIEE Conference Paper by Stuart Jackson, referenced at the end of this chapter, will prove useful in designing the filter required to meet specific ripple requirements across the load.

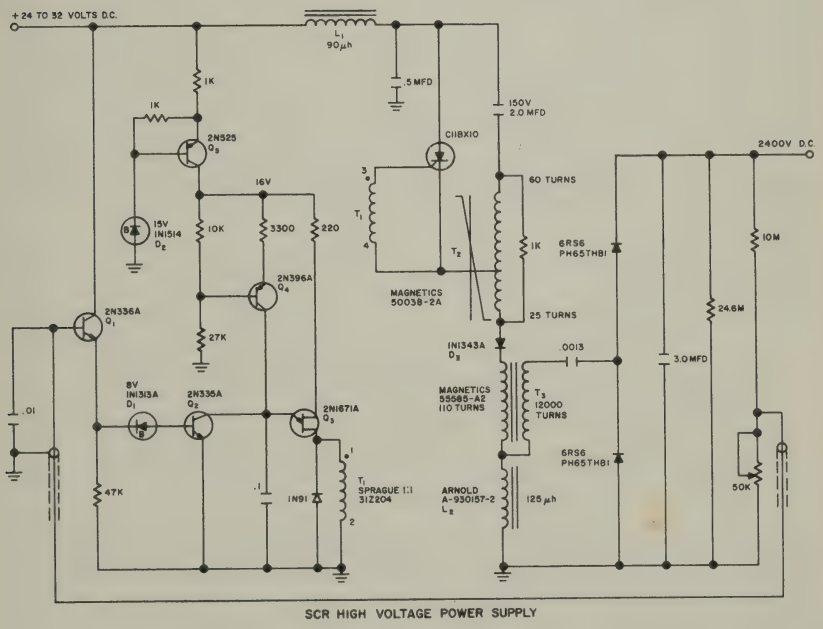
10.3 HIGH VOLTAGE REGULATED POWER SUPPLY

Another power supply utilizing the Morgan chopper and quite similar to Figure 10.3 is shown in Figure 10.6. Here the load is replaced by the primary of a step-up transformer and since it is desirable that the transformer "ring" in order to reset itself, the free-wheeling diode and associated filter components have been omitted. Series diode D_3 keeps the transformer "ringing" voltages out of the commutating circuit and choke L_2 insures successful commutation under heavy or shorted output conditions.

A half-wave doubler circuit is used to rectify the high voltage in order that both polarities of voltage across the secondary are loaded. Filtering is accomplished by the 3 MFD capacitor which is also the main load on the supply. A portion of the output voltage is selected by a voltage divider and fed to the input of the feedback regulator, emitter follower Q_1. It is then compared to zener D_1, amplified by Q_2, and used to vary the UJT frequency in the shunt mode described previously (Sec. 4.15.2).

Transistor Q_4 provides constant current charging of the UJT timing capacitor. This insures a linear sawtooth of voltage across the capacitor and hence better noise immunity when the UJT frequency needs to be varied over a very wide range. Otherwise at low frequencies the capacitor would be charged to very nearly the UJT firing voltage for relatively long periods of time and any noise or hum could cause "jitter" in the repetition rate. In most supplies, the required frequency change is small enough that Q_4 can be replaced by a resistor.

A "lock-out" circuit is provided by transistor Q_5. Whenever the main B+ drops to too low a value to insure commutation of the SCR, Q_5 will withhold voltage from the UJT trigger circuit and the SCR will not be fired. This precaution is necessary only when the DC supply is apt to vary over an unusually wide range, or when the DC is turned on at zero volts and slowly increased to the operating range. On a nominal 28 volt system, commutation was successful



SCR High Voltage Power Supply
Figure 10.6

down to 14 volts, so in the usual case a lock-out circuit for low voltage is not required. The regulated 16 volt supply generated by Q_5 is not necessary for proper operation of the trigger circuit.

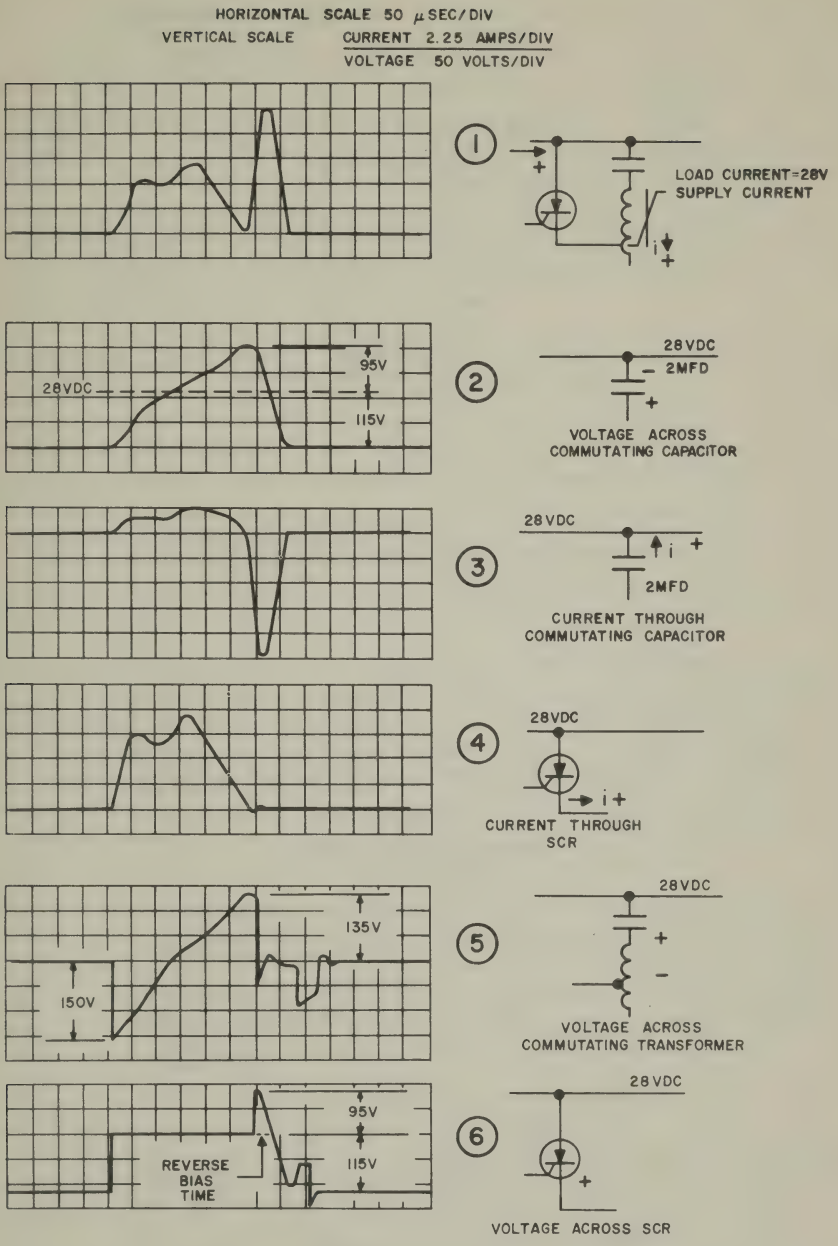
Choke L_1 and the adjacent .5 MFD capacitor suppress RF energy from being conducted back into the DC supply. As shown, the supply will readily exceed the requirements of MIL-I-6181B. Interference and its suppression in SCR circuits is further discussed in Chapter 13.

Temperature compensation is readily attained as the switching action of the SCR is inherently quite stable. "On" time of the chopper power pulse is a function of the commutating transformer, commutating capacitor, and the load. None of these components is particularly temperature sensitive, with the result that "on" time is fairly constant with temperature. Repetition rate, or frequency, is determined by the regulator except during the initial charging of the 3 MFD capacitor when the UJT runs at a maximum frequency determined by the timing R and C. By using stable R and C in the emitter timing circuit and proper selection of R_2 in base 2 (General Electric Transistor Manual, 5th Ed., page 141) maximum frequency can easily be held constant over the temperature range. A frequency of 2 to 3 KC is usually satisfactory for the maximum rate.

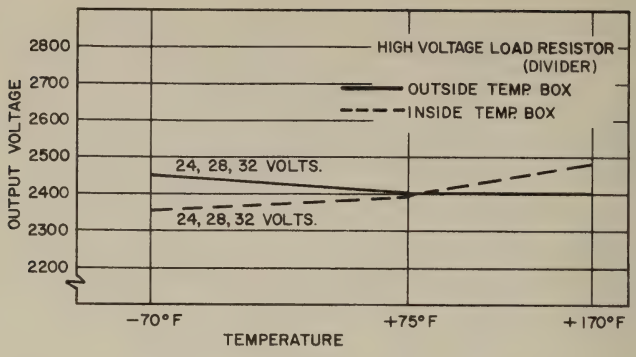
Approximately 2 seconds after turn on, the output is up to the design value of 2400 volts and the SCR firing rate is reduced from 2 KC to less than 100 cycles. The magnitude of the output voltage and its temperature characteristics are dependent on only a very few components, namely the voltage divider, the emitter base diodes of Q_1 and Q_2 and zener diodes D_1. Q_1, Q_2 and D_1 are directly in series and may be self compensated as follows: Q_1 and Q_2 input diodes will each change a negative 2 mV/°C for a total of 4 mV/°C, while D_1 will change a positive 4 mV/°C. The temperature coefficient of a zener diode is a strong function of its zener voltage; below 6 volts it is negative, above 6 volts it is positive. Since all changes in the amplifier are linear, compensation will track over the temperature range. The voltage divider must provide a constant ratio as temperature varies. Compensation of the divider can take many forms:

1. Break up the 10 meg resistor into several smaller resistors which have temperature coefficients more nearly equal to the potentiometer.
2. Addition of various series, parallel combinations of thermistors.
3. Use of a higher voltage zener at D_1 to "tilt" the amplifier characteristic opposite to the divider characteristic.

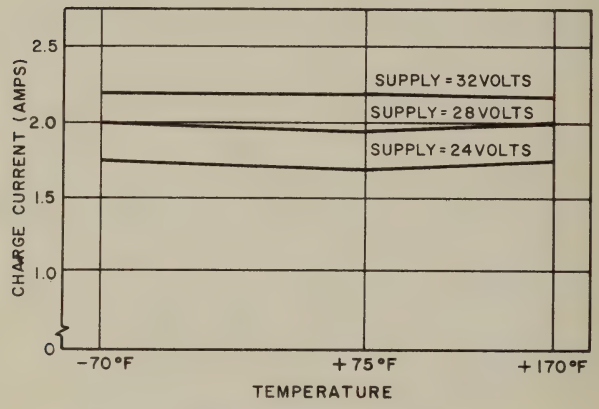
Voltage and current waveshapes at various points in the circuit are shown in Figure 10.7 and performance curves vs. temperature are shown in Figures 10.8-10.10. Output voltage regulation vs. input voltage (curve not shown) exhibited no discernible change over a range of 20 to 38 volts. While not directly measured, the over-all system was observed to have fast transient response with no tendency to overshoot, undershoot, hunt or oscillate.



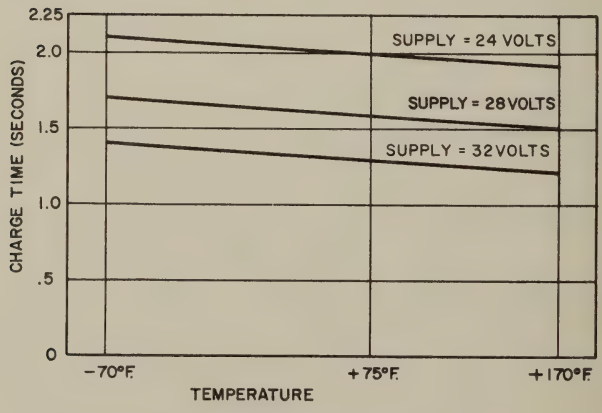
Oscillograms
Figure 10.7



Output Voltage
High Voltage Load Resistor (Divider)
Figure 10.8



Charge Current (Amps)
Figure 10.9



Charge Time (Seconds)
Figure 10.10

10.4 CHOPPER (MORGAN CIRCUIT) TRANSFORMER DESIGN

An experimental procedure that will produce a satisfactory chopper transformer is given below.

1. Select the desired "on" time of the power pulse, consistent with the repetition rate. In the preceding design, the "on" time is approximately 300 μsec. Although frequencies to 20 Kc are possible, switching losses become appreciable and therefore two to three kilocycle rates are more common. Since regulation is obtained by varying the frequency, the maximum frequency will be used to supply the heaviest load at minimum input voltage. A potentiometer may be used for the timing resistor in the unijunction trigger circuit for flexibility of maximum frequency during design.

2. Select a favorable commutating voltage. A lower voltage will permit use of a more economical SCR, but will necessitate a larger capacitor to provide sufficient current and reverse bias time for commutation. An extended foil capacitor should be used of the type described in technical bulletin GEZ-3279, available from the G-E Capacitor Section, Hudson Falls, N. Y. The commutating voltage chosen here is 95 volts. A lower voltage and/or a smaller capacitor would probably have been possible if a larger inductance had been used in series with the load transformer. Then the charge on the capacitor would be maintained for a longer period and the reverse bias time on the SCR lengthened. Or, stated another way, the added inductance would lower the resonant frequency of the circuit.

At the first instant, the capacitor discharge current will go back up through the SCR until it blocks in the reverse direction. The duration and magnitude of reverse current are direct functions of the forward current immediately before commutation. Once the SCR blocks, usually after a few microseconds, the remainder of the capacitor charge will go through the load to ground. The reverse voltage time across the SCR is then determined by the series resonance of the capacitor, the saturated inductance of the chopper transformer, and the reactance in the load circuit. See Oscillogram #6, Figure 10.7.

3. Turns ratio may now be estimated. Rigorous solution for the turns ratio would require the complete transient solution of the entire commutating and load circuits. Many times a faster solution can be obtained by using the approximation shown below and then winding an experimental transformer with a few taps either side of the calculated values. For transformers with N_S/N_P less than about 5:1;

$$\frac{N_S}{N_P} = \frac{\text{commutating voltage}}{(K)\ \text{supply voltage}}$$

K will vary from approximately 1 when the load is mostly resistive to approximately 1.6 when the load is quite inductive. In this design, $K \approx 1.4$, so that:

$$\frac{N_S}{N_P} = \frac{95}{1.4 \times 28} = 2.4$$

4. Now the total number of turns on the chopper transformer may be calculated. Total turns and cross-sectional area of the core may be traded for

one another over a broad range of values with very little effect on the circuit operation. The more turns used, the smaller the core may be. As described previously, the Morgan circuit need not go to negative saturation for proper operation. In fact, it has been found that the circuit will operate stably over a wider range of input voltage, temperature, and frequency if the core never goes to negative saturation.

Since the turns and the area are interchangeable, select the core area deliberately on the large side. This mean fewer turns on the experimental transformer and hence easier winding. Also, any circuit misbehavior is much less with too large a core as compared to too small a core. "ON" time of the power pulse has been selected at 300 μsec and commutating voltage at 95 volts. Construct the following figures.

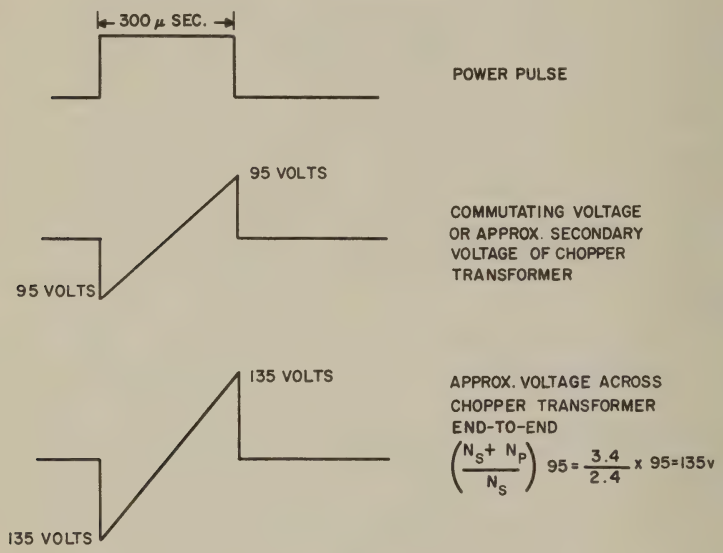


Figure 10.11

$$\text{Total flux (In one direction)} = \frac{\text{volt time area (in one direction)}}{\text{total turns}}$$

$$\text{Flux } \phi = \frac{\text{volts} \times 10^8 \times \text{sec.}}{\text{turns}}$$

$$\text{In this case } \phi = \frac{135 \times 10^8 \times 150 \times 10^{-6} \times \frac{1}{2}}{\text{turns}} \text{ maxwells}$$

$$\phi = \frac{1.01 \times 10^6}{\text{turns}} \text{ maxwells}$$

$$\frac{\phi \text{ (maxwells)}}{\text{A (cm}^2\text{)}} = \text{B gauss (flux density)}$$

Maximum flux density for Orthonol or Deltamax is 14000 gauss. Select a large core from the manufacturer's catalogue, here a 50038-2A from Magnetics, Inc., with an area of .685 cm^2. The total change possible from positive to negative saturation is 28000 gauss. To insure that negative saturation is not reached, use two-thirds of 28000 or approximately 18000 gauss.

$$18000 \text{ gauss} \times .685 \text{ cm}^2 = 12{,}300 \text{ maxwells}$$
$$12300 \text{ maxwells} = 1.01 \times 10^6/\text{turns}$$
$$\text{turns} = 1.01 \times 10^8/.0123 \times 10^6 = 82$$
$$\text{Primary turns} = 82/3.4 = 24$$
$$\text{Secondary turns} = 82 - 24 = 58$$

Once the circuit is successfully switching, the voltage across the commutating transformer may be viewed with an oscilloscope. By careful observation of the voltage amplitude, the time, and the waveshape, appropriate corrections to the transformer can be made according to the volt-sec/turn relationships given earlier.

The commutating capacitor will generally be between 1 and 10 mfd, the larger size used for lower power supply voltages and heavier load currents. Here again it is better to be on the large side initially. A good approximation may be obtained from the formulas given in Section 7.6.

REFERENCES

1. "An All-Solid-State Phase Controlled Rectifier System," F. W. Gutzwiller, AIEE Paper CP 59-217, American Institute of Electrical Engineers, New York, N. Y., 1959.
2. Morgan, R. E., "A New Power Amplifier Using a Single Controlled Rectifier and a Saturable Transformer," AIEE, Conference Paper #60-410 (copies available from AIEE, 33 W. 39th St., New York 18, N. Y.).
3. "Silicon Controlled Rectifier High Voltage Power Supply," G. E. Snyder, Application Note 610.5, available from General Electric Co., Rectifier Components Dept., Auburn, N. Y.
4. "30V 10A Regulated Power Supply using the Variable Output Transistor Oscillator with Current Transformer," Stuart P. Jackson, AIEE Conference Paper 61-717, available from AIEE, New York, N. Y.

CHAPTER 11

PROTECTING THE SCR AGAINST OVERLOADS AND FAULTS

Satisfactory operation of SCR circuits and the equipment in which they operate often depends heavily on the ability of the system to survive unusual overcurrent conditions. One obvious answer to this requirement, although not usually an economical one, is to design the system to withstand the worst fault currents on a steady-state basis. This requires semiconductors and associated components that are rated many times the normal load requirements. Where this approach is not possible because of economics or other factors, an adequate overcurrent protective system is usually used.

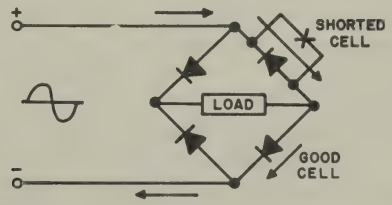
11.1 WHY PROTECTION?

According to the AIEE Subcommittee on Electronic Converter Circuits,[1] the functions of an overcurrent protective system are any or all of the following:

1. To limit the duration of overloads and the frequency of application of overloads.
2. To limit the duration and magnitude of DC short circuits.
3. To limit the duration and magnitude of fault currents due to shorted cells.

The objective of these functions is to safeguard not only SCR's and diodes but also the associated electrical devices and buswork in the rectifier equipment from excessive heating and magnetic stresses. The trend toward high capacity systems feeding electronic converter equipment often results in extremely high available fault currents. Since both heating and magnetic stresses in linear circuit elements respond to the square of the current, the importance of adequate protection in "stiff" systems is self-evident.

Elaborating on function No. 3 above, SCR's as well as diode rectifiers may fail by shorting rather than by opening. In all power rectifier circuits except the simple half-wave circuit, such a cell fault results in a direct short from line to line through the low forward resistance of the good cells in adjacent circuit



Arrows Indicate Flow of Fault Current Through Good Cell After Adjacent Leg Has Shorted. Load Resistance Does Not Limit Current
Figure 11.1

legs during at least part of the cycle. See Figure 11-1 where the diode symbol is used to represent both SCR's and diodes for the sake of generalization. Under these circumstances, a protective system functions either to shut the entire supply down, or to isolate the shorted cell in order to permit continuity of operation. This will be discussed at greater length later.

It is difficult to make broad recommendations for overcurrent protection since the concept of satisfactory operation means different levels of reliability in different applications. The selection of a protective system should be based on such individual factors as:

1. The degree of system reliability expected.
2. The need or lack of need for continuity of operation if a semiconductor fails.
3. Whether or not good rectifier cells are expendable in the event of a fault.
4. The possibility of DC bus faults.
5. The magnitude and rate of rise of available fault current.

Depending upon the application, these various factors will carry more or less weight. As the investment in semiconductors increases for a specific piece of equipment, or as an increasing number of parallel cells in a circuit increases the possibility of a single cell failure, or as continuity of operation becomes more essential, more elaborate protective systems are justified. On the other hand, in a low cost circuit where continuity of operation is not absolutely essential, the semiconductors may be considered expendable and a branch circuit fuse in the AC line may be all that is needed, or justified, for isolation of the circuit on faults.

It is therefore reasonable that each circuit designer rather than the semiconductor component manufacturer decide precisely what level of protection is required for a specified circuit. Once the specific requirements are determined the component manufacturer can recommend means of attaining these specific objectives. This chapter is prepared to assist the circuit designer in determining his protection requirements, and then to select satisfactory means of meeting these requirements.

11.2 OVERCURRENT PROTECTIVE ELEMENTS

The main protective elements can be divided into two general classes. One class consists of those devices which protect by interrupting or preventing current flow, and the other class consists of those elements which limit the magnitude or rate of rise of current flow by virtue of their impedance.

Among the elements in the first class are:

1. The AC circuit breaker or fuse which disconnects the entire circuit from the supply.
2. The cell fuse or breaker which isolates faulted cells.
3. DC breakers or fuses which isolate load faults from the rectifier or a faulted rectifier from DC feedback from the load or parallel converter equipments.
4. Current limiting fuses and SCR circuit breakers.
5. Gate blocking of SCR's to interrupt overcurrent.

Among the elements of the second class which limit magnitude or rate-of-rise of current are:

1. Source impedance.
2. Transformer impedance.
3. Inductance and resistance of the DC circuit.

Throughout this discussion it is well to bear in mind that circuit interrupting devices that are tripped by magnetic circuits, such as solenoids in fast-acting breakers and interrupting devices that are tripped by thermal means, such as fuses or breakers with thermal overloads, all react to the RMS value of the current. The semiconductor itself reacts essentially to heating, but having a non-linear resistance, it heats proportional to a current value somewhere between the RMS and average value. The considerable difference that may occur between these respective values of current in rectifier circuits is of particular importance in co-ordinating protective elements with one another and with the semiconductors.

11.3 CO-ORDINATION OF PROTECTIVE ELEMENTS

Depending upon their complexity and the degree of protection desired, converter circuits include one or more of the various interrupting devices listed above. Functioning of these devices must be co-ordinated with the semiconductor and with each other so that the overall protection objectives are met. Fuses or breakers must interrupt fault currents before semiconductor cells are destroyed. In isolating defective cells from the rest of the equipment, only the fuse or breaker in series with a defective cell should open. Other fuses and breakers in the circuit should remain unaffected. On the other hand, when a DC load fault occurs, main breakers or fuses should function before any of the cell-isolating fuses or breakers function. This fault discriminating action is often referred to as selectivity. In addition, the voltage surges developed across SCR's and diode rectifiers during operation of protective devices should not exceed the transient PRV rating of these cells. More complex protective systems require meeting additional co-ordinating criteria. The example of a protection system and its associated co-ordination chart described later in this discussion illustrates some of the basic principles of co-ordination for both overloads and stiff short circuits.

The magnitude and waveshape of fault and overload currents vary with the circuit configuration, the type of fault, and the size and location of circuit impedances. Fault currents under various conditions can generally be estimated by analytical means. References 1, 2, and 3 show analytical methods for calculating fault currents for generally encountered rectifier circuits.

For overloads on rectifier or inverter circuits where the current is limited to a value which the semiconductors can withstand for roughly 50 milliseconds, conventional circuit interrupting devices like circuit breakers and fuses can usually be used satisfactorily for protection. This type of overload can be expected where a sizeable filter choke in the load or a "weak" line limits the magnitude or rate of rise of current significantly. By placing the circuit breaker or fuse in the line ahead of the semiconductors, the protective device can be

designed to isolate the entire circuit from the supply source whenever the line current exceeds a predetermined level which approaches the maximum rating of the semiconductors for that duration of fault.

For time intervals greater than approximately 0.001 second after application of an overload, the SCR rating for co-ordination purposes is determined by the methods discussed in Section 3.5.1. If the overload being considered is of a type that is expected only rarely (no more than 100 times in the life of the equipment), additional SCR rating for overload intervals of one second and less can be secured by use of the surge curve and I^2t rating for the specific device being considered.

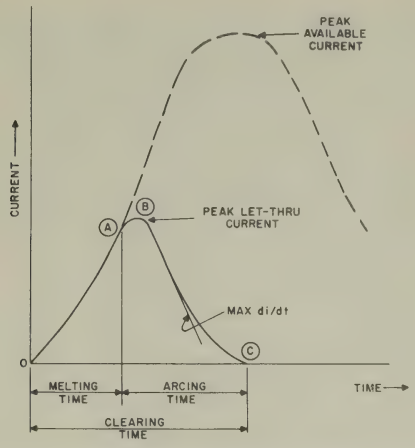
The surge characteristic is expressed as the peak value of a half-sine wave of current versus the number of cycles that the semiconductor can handle this surge concurrent with its maximum voltage, current, and junction temperature ratings. In circuits that do not impose a half-sine wave of fault current on the semiconductors, the surge curve can be converted into current values that represent the particular waveshape being encountered. The surge curve for the semiconductor can be converted to different waveshapes or different frequencies in an approximate, yet conservative, manner for this time range by maintaining equivalent RMS values of current for a specific time interval. For example, the peak half-sine wave surge current rating of the 2N681 SCR for 10 cycles on a 60 cps base is shown on the spec sheet to be 88 amperes. For a half-sine waveshape, the RMS value of current over the complete cycle is one-half the peak value, or 44 amperes. To convert this to average cell current in a three phase bridge feeding an inductive load (120 degree conduction angle), divide this RMS value by $\sqrt{3}$ ($44 \div \sqrt{3} = 25.4$ amps). To determine the total load current rating for a bridge using this cell, multiply the average cell current by 3 ($25.4 \times 3 = 76.2$ amps).

11.4 PROTECTING CIRCUITS OPERATING ON STIFF POWER SYSTEMS

Conventional circuit breakers and fuses can be designed to provide adequate protection when fault currents are limited by circuit impedance to values within the semiconductor ratings up to the time when these protective devices can function. However, circuits requiring good voltage regulation or high efficiency will usually not tolerate high enough values of series impedance to limit fault currents to such low values. When a fault occurs in a circuit without current limiting impedance, current will develop in a shape similar to the dashed line in Figure 11.2. Its rate of rise is limited by the inductance inherent in even the stiffest practical systems. If the peak available current substantially exceeds the semiconductor ratings, and if it is permitted to flow in the circuit, the semiconductor would be destroyed before the current reaches this first peak. Conventional circuit breakers and fuses will not function quickly enough. Instead, so-called "current limiting" fuses which melt extremely fast at high levels of current are used. Alternately, "electronic circuit breakers" of the type discussed in Section 7.8 can be designed for this purpose.

The action of a typical current limiting fuse is indicated in Figure 11.2. Melting of the fuse occurs at point A. Depending on the fuse design and the

circuit, the current may continue to rise somewhat further to point B, the peak let-thru current. Beyond this point the impedance of the arcing fuse forces the



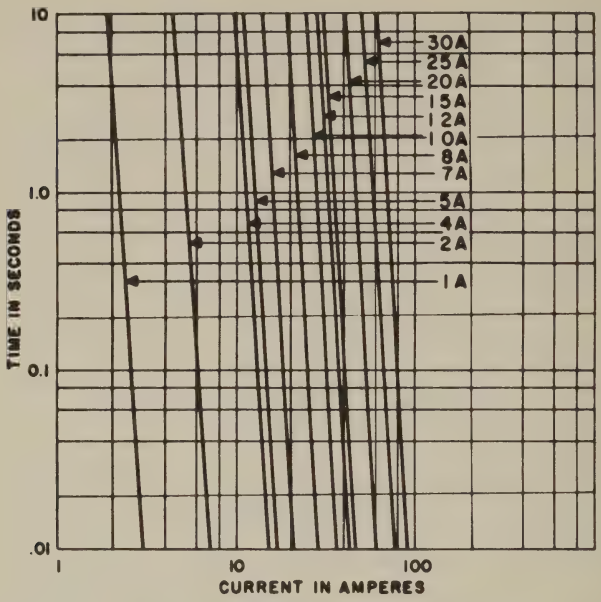
Limiting Action of Current Limiting Fuse
Figure 11.2

fault current down to zero at some point C. A satisfactory current limiting fuse will have an arcing time approximately equal to the melting time. If the fuse interrupts fault current too quickly, the high rate of change of current (di/dt) will induce levels of transient voltage in the circuit inductances that can destroy rectifier cells. For this same reason, it is not wise to use any higher voltage fuse rating than is required by the supply voltage. Surplus voltage rating of a fuse over the circuit voltage can lead to unnecessarily abrupt arc-quenching with resultant destructive voltage transients. However, the current interrupting rating of the fuse should be ample for the maximum available current to be expected.

Since the buildup of current is so rapid and since the current amplitude is so high in a circuit with low impedance, additional phases and circuit legs usually help very little in increasing the fault current capacity of a circuit because permanent damage may be done before commutation to another leg can occur. For conservative design, all fault current on stiff faults should be considered to flow through only one leg, dividing only between the parallel cells in that particular leg.

Both current limiting fuses[4,5] and semiconductors with uniform current distribution across their junctions[6,7] exhibit ability to withstand essentially constant$\int i^2dt$ below approximately one cycle (i = instantaneous current, t = time). This fortunate circumstance provides a simple tool for co-ordinating current limiting fuses and semiconductors in this difficult-to-define area below one cycle. The necessity of calculating fault currents in this region for co-ordination purposes is thereby largely eliminated. If the interrupting or clearing I^2t rating of a fuse is lower than the I^2t rating of the cell in series with it, the fuse will interrupt fault current before the cell fails regardless of current magnitude or rate of rise in the sub-cycle region.

Some fuses are rated for their maximum clearing I^2t.[8] However, fuse manufacturers do not usually publish I^2t ratings as such for their current limiting



Form 101 Amp-Trap Characteristic Curves, Melting Time vs. Current 1 to 30 Ampere Cartridge Size 250 Volt—Type 1
Figure 11.3

fuses. In the latter circumstance, the clearing I^2t to melting can be approximated from the melting time-current characteristic of the fuse. Figure 11.3 illustrates the characteristics of a line of current limiting fuses manufactured by the Chase-Shawmut Company, Newburyport, Massachusetts. The melting I^2t of the 30 ampere fuse, for example, can be approximated by squaring the current value at 0.01 second and multiplying it by the time ($90^2 \times .01$ second = 81 amp^2-seconds). If the fuse co-ordination is critical in a particular application, the manufacturing tolerance should be factored into the current or time values used to determine melting I^2t.

The arcing I^2t of satisfactory current limiting fuses will not exceed twice the melting I^2t, and total clearing I^2t will therefore not exceed three times the melting I^2t. In the above example, maximum clearing I^2t will not exceed $3 \times 81 = 243$ ampere^2-seconds for the 30 ampere Form 101 Amp-Trap fuse. It should be emphasized that this type of approximation should only be used when specific I^2t data is not available from the fuse manufacturer.

The minimum I^2t rating of the semiconductor cell is specified by the manufacturer. Depending on the cell design, the I^2t rating may vary with initial junction temperature and may depend on whether or not reverse voltage is impressed on the cell following the current surge.

Several companies manufacture current limiting fuses in various voltage, current and speed ratings. Their literature indicates the following ratings:

Fuse Manufacturer	*Current Limiting Fuse Designation and Rating*
General Electric Co. Philadelphia, Pa.	CLF fuses 6 to 200 amps, DC, 250 volts 6 to 200 amps, DC, 600 volts 6 to 600 amps, AC, 250 volts 6 to 1200 amps, AC, 600 volts 1600 to 4000 amps, AC, 480 volts
Chase-Shawmut Co. Newburyport, Mass.	Amp-Trap fuses, Form 101 1 to 1000 amps, AC-DC, 130 volts 1 to 5000 amps, AC-DC, 250 volts Amp-Trap fuses, Form 101CK 100 to 600 amps, AC-DC, 600 volts Amp-Trap fuses, Form 208 400 to 6000 amps, AC-DC, 250 volts Amp-Trap fuses, Form 480 400 to 6000 amps, AC, 600 volts
Bussman Mfg. Co. St. Louis, Mo.	Buss ANL Aircraft fuses 50 to 500 amps, AC-DC, 32 volts Buss Limitron fuses 1 to 1000 amps, AC-DC, 130 volts (KAA-KAH) 1 to 600 amps, AC-DC, 250 volts (KAB) 1 to 600 amps, AC-DC, 600 volts (KAC-KAJ)

For data on the melting time-current characteristics of these fuses, the designer should refer to the curves or other data published by the fuse manufacturer.

When a current limiting fuse in the primary of a transformer must be co-ordinated with a semiconductor cell in the secondary, their respective I^2t's can be compared by the following equation:

$$I^2t_{fuse} \leqq \left(\frac{V_{sec.}}{V_{prl.}}\right)^2 \times I^2t_{cell}$$

where $V_{sec.}$ = rated secondary voltage of transformer.

$V_{prl.}$ = rated primary voltage of transformer.

In similar manner, the clearing I^2t of a fuse being fed by a group of N parallel semiconductor cells should be no greater than N^2 times the I^2t rating of the individual cells if all the parallel cells share current equally. If the cells are derated for parallel operation to compensate for inequalities in current sharing, the relationship between clearing I^2t of the fuse and the I^2t rating of the individual cell can be expressed as follows:

$$I^2t_f \leqq I^2t_c\,[N(1 - S) + S]^2$$

where I^2t_f = clearing I^2t of fuse

I^2t_c = I^2t rating of semiconductor cell

N = number of parallel rectifier cells

S = derating factor for parallel cell operation (usually 0.20)

11.5 INTERRUPTED SERVICE TYPE OF PROTECTION

By inserting the protective device in the AC lines feeding the SCR's and diode rectifiers, protection can be provided both against DC faults and semiconductor cell faults if there is no possibility of DC feed into faults of the semiconductor cells themselves. DC feed into cell faults will occur in single-way circuits when other power sources feed the same DC bus or when the load consists of CEMF types of loads such as motors, capacitors, or batteries. The following is an example of this type of AC line protection in a circuit without current limiting impedance. Upon functioning of the protective system, the circuit is interrupted and shut down.

11.6 EXAMPLE OF FAULT PROTECTION (NO CURRENT-LIMITING IMPEDANCE)

Application: — 117 V RMS AC supply, 60 cps

— Single phase bridge employing two 2N686 SCR's for phase control in two legs and two 1N2156 diode rectifiers in the other two legs. See Figure 11.4.

— Maximum continuous load current = 12 amperes.

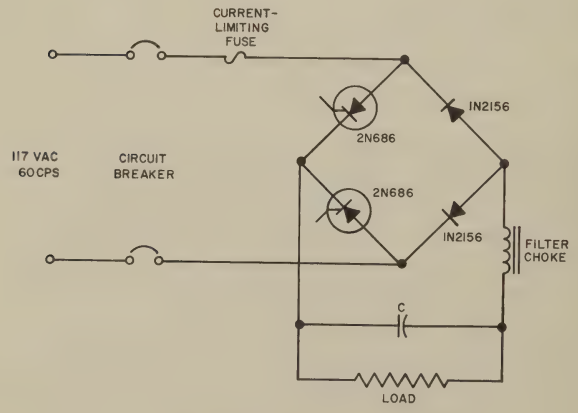
— Choke input filter.

— Line impedance negligible. Peak available fault current in excess of 1000 amperes.

— Maximum ambient = 55°C free convection. Each semiconductor mounted to a 4" x 4" painted copper fin 1/16" thick.

Requirements for Protective System:

— Protection system must be capable of protecting SCR's and diodes against overloads, DC shorts, and shorting of individual semiconductors. System can be shut down when any of these faults occur.



Circuit for Example of Fault Protection
Figure 11.4

Solution: — Since the current rating of the 1N2156 is higher than the 2N686 both at steady-state and under overload, the protection, if properly co-ordinated with the 2N686, will be ample for protecting the 1N2156 also.

Using the data for a 2N686 on a 4" x 4" fin given in Figure 3.4 and the fifth section of Fig. 3.5 for the square wave of current characteristic of a single phase rectifier circuit with inductive load,

$$P_o = \frac{125 - 55}{\frac{.0083 \times 5.1}{.0167} + \left(1 - \frac{.0083}{.0167}\right) 0.6 - 0.47 + 0.3}$$

$= 26.1$ watts maximum steady-state heating allowable per SCR

From the specifications for the 2N686, this level of heating will be developed by 19 amperes peak or 9.5 amperes average load current at 180 degree conduction angle. With inductive load, the conduction angle is 180 degrees regardless of the firing angle of the SCR's, and the steady-state RMS line current is equal to the average current value $= 2 \times 9.5$ amps/cell $=$ 19 amps.

Assuming that faults and overloads will be superimposed on the steady-state equipment rating, the semiconductor overload rating can be calculated from the sixth section of Fig. 3.5.

$$P_{OL} = \frac{T_J - T_A - P_{CD}R_T}{r_T} + P_{CD}$$

For example, for 10 seconds the SCR can dissipate the following power without its junction exceeding 125°C:

$$P_{OL} = \frac{125 - 55 - 7 \times 5.1}{2.2} + 7 = 22.6 \text{ watts/cell}$$

Average current rating per cell $= 14.9$ amps (from specification sheet).

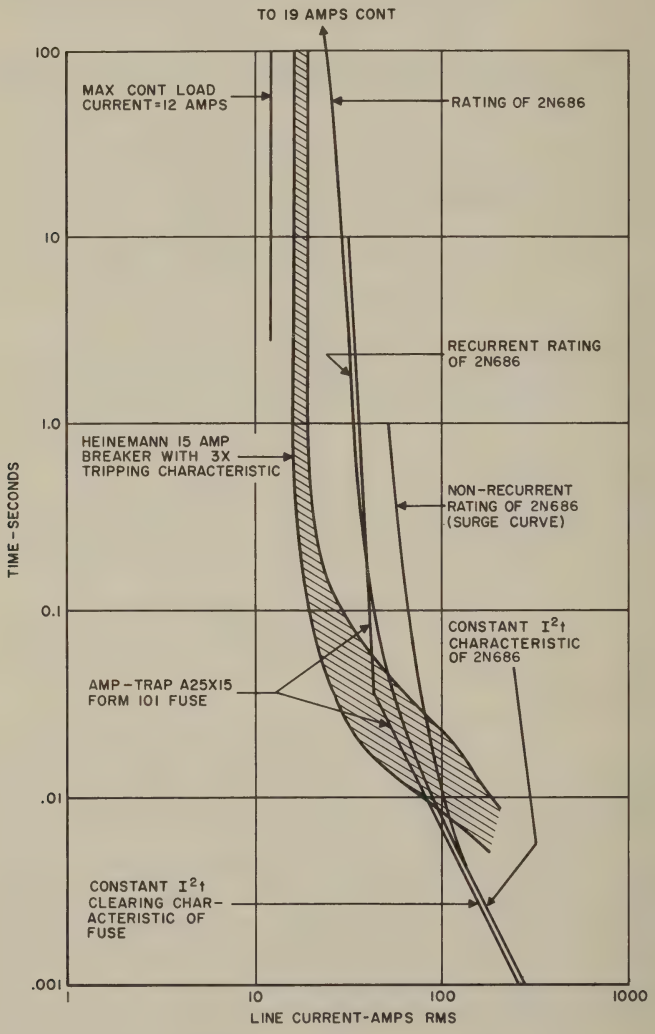
Rated bridge output current $= 2 \times 14.9 = 29.8$ amps RMS.

This point and others calculated by the same means are plotted on the co-ordination chart of Figure 11.5. Overload ratings achieved by this technique limit junction temperature to 125°C.

For non-recurrent types of overload as typified by accidental short circuits and failure of filter capacitors, the SCR is able to withstand considerably higher overloading as specified in the I^2t and surge current ratings. A typical point of this kind can be calculated as follows. At 0.1 second, a time which is equivalent to 6 cycles on the surge curve, the peak surge current rating of the 2N686 is 92 amperes. The RMS bridge rating is $92 \div \sqrt{2} = 65$ amperes. This curve blends into ratings determined from the I^2t rating below approximately 50 milliseconds. The I^2t rating of the 2N686 is 75 amp^2-sec. At .001 second, the current rating of the SCR is $\sqrt{75 \text{ amp}^2\text{-sec.}/.001 \text{ sec.}} = 274$ amps. Below ½ cycle,

the rating of the SCR and the rating of the bridge are identical. Thus, at .001 second, the bridge is rated 274 amps RMS also.

To afford protection against short circuits of the load and shorted semiconductors in this type of circuit, a current limiting fuse is required. The fuse must carry the steady-state line current without melting. An Amp-Trap A25X15 Form 101 fuse rated at 15 amperes continuous current should handle the 12 amperes RMS steady-state line current satisfactorily. Melting characteristics of this fuse are shown in Figure 11.3, and are plotted directly on the co-ordination curve of Figure 11.5 since both curves are in RMS terms. The fuse melting



Co-ordination Curve for Example of Fault Protection of SCR's
Figure 11.5

characteristic below 0.01 second can be determined on the basis of constant I^2t as described earlier. The maximum fuse I^2t is (46 amp. plus 5% tolerance)^2 × 0.01 second = 23.3 amp^2-sec. Melting currents for time intervals less than 0.01 second can be approximated by dividing the I^2t rating by the time in seconds and extracting the square root similar to the method for determining the cell rating for this time interval. For example, at 0.001 second the maximum melting current is $\sqrt{23.3/.001}$ = 152 amp RMS. To determine the clearing time-current characteristic of the fuse in this region, the time for melting is multiplied by 3. The co-ordination chart in Figure 11.5 shows a fuse interrupting characteristic which is based on this approach and made very conservative by extending the straight line of the interrupting characteristic all the way up to its intersection with the published fuse characteristic at a time substantially greater than 0.01 second.

From the co-ordination curve, it can be seen that the current limiting fuse in the line will protect the SCR's for any type of fault of sufficient magnitude to blow the fuse in 0.2 second or less since the fuse rating is to the left of the cell rating.

The curves also indicate that, for times longer than 0.2 second, the SCR's are likely to fail before the fuse blows. In order to provide protection for the SCR's for these lower current faults, a circuit breaker is used. The co-ordination chart shows the tripping characteristic of a Heinemann 15 ampere molded case circuit breaker using the Type 3X time-delay characteristic.

The co-ordination curve reveals that the circuit breaker will trip on any faults under 42 amperes RMS, but above 18 amperes RMS. Between 42 amperes and 85 amperes, the fuse and/or the breaker will function. Above 85 amperes, the fuse only should blow. Under no circumstances should good SCR's fail.

11.7 NON-INTERRUPTED SERVICE UPON FAILURE OF SCR

In the foregoing discussion and example, the SCR's are protected against overloads and short circuits of the output and also against the fault currents that occur if another SCR or diode rectifier in the circuit should short. Protection is afforded by disconnecting the entire rectifier from its supply voltage.

In some types of service such as high reliability military systems and continuous industrial processes, a service interruption due to a semiconductor failure cannot be tolerated regardless of how remote this possibility may be. To maintain service under these conditions requires redundancy of semiconductors and a means of disconnecting faulty cells whenever failure of a semiconductor occurs. It has been observed that, when failures of SCR's have occurred, they could be classified into three main categories:

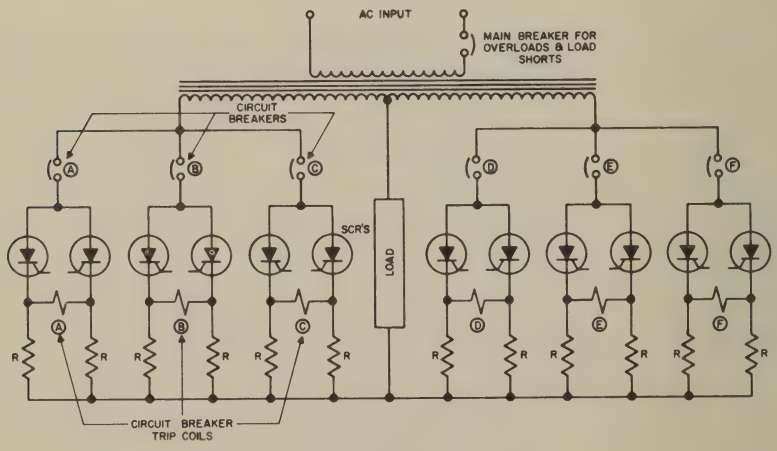
1. Loss of PRV or reverse blocking ability. In rectifier circuits this generally causes a high fault current to flow.
2. Loss of V_{BO} or forward blocking ability. In a rectifier circuit, this will generally result in loss of control of output voltage, the SCR remaining in the forward "on" state.
3. Failure to fire or switch into the forward conduction state. This will

also result in loss of control of output voltage since the SCR will remain in the "off" state.

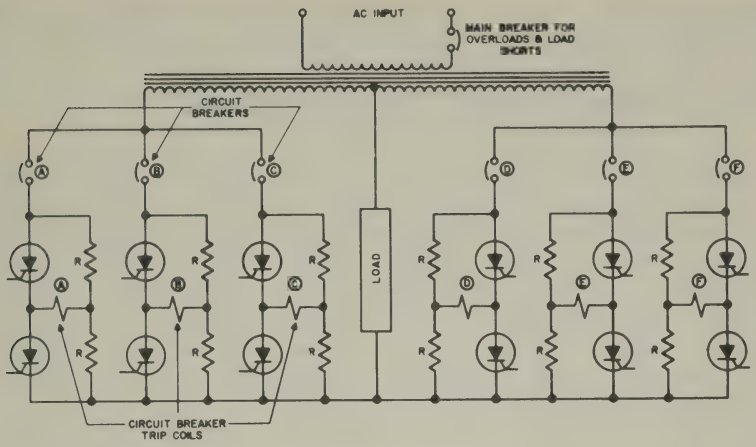
(Conditions 1 and 2 may be combined in a short circuited device.)

Figures 11.6 and 11.7 suggest two of several possible methods of detecting and isolating defective SCR's from the circuit without interrupting the flow of controlled power to the load. Figure 11.6 illustrates a single phase centertap phase-controlled power supply in which the SCR's in each leg of the circuit are grouped into pairs of parallel-matched cells. A low value of resistance R is connected in series with each SCR. The value of R is selected to limit fault current through good SCR's if one SCR loses its reverse blocking ability. The contacts of an isolating circuit breaker are connected in series with each pair of SCR's. The trip coil of each breaker or the coil of a pilot relay is connected across the bridge formed by the pair of SCR's and their respective series resistors. When both SCR's of a pair are functioning properly and therefore identically, the instantaneous currents through the SCR's and their series resistors are essentially equal and therefore no current flows through the circuit breaker trip coil. If either SCR in a pair fails in any one or more of the three modes enumerated above, unequal currents will flow for at least part of each cycle through the SCR's. Current will flow through the trip coil associated with that SCR pair, tripping the series circuit breaker and isolating the pair from the main circuit. As long as the remaining SCR's in that leg of the circuit are capable of handling the full load current, the circuit will be capable of continuing operation indefinitely. The circuit breakers can be used to actuate an alarm or annunciator scheme to warn the equipment operator of the failure so that he can replace the faulty SCR during a scheduled maintenance shutdown of the equipment.

The circuit shown in Figure 11.7 is more economical than Figure 11.6 for circuits requiring high output voltages rather than high currents. In this circuit the SCR's are grouped in series-connected pairs for the purpose of handling higher voltages. A resistor R is connected in shunt with each SCR to assist in



Parallel SCR Pairs for Non-Interrupted Service
Figure 11.6



Series SCR Pairs for Non-Interrupted Service
Figure 11.7

voltage sharing and to provide in conjunction with the pair of SCR's a bridge across which to connect the circuit breaker trip coil. When both SCR's are functioning properly, only the difference in leakage currents between the two SCR's flows through the trip coil. When either SCR in a pair malfunctions for one of the reasons cited earlier, a substantial current will flow for at least part of the cycle through the trip coil, thus opening the circuit breaker and isolating that pair of SCR's from the circuit. In order that the trip coil will reliably discriminate between the normal leakage balancing current of the SCR's and the unbalance current resulting from a faulty SCR, it may be necessary to reduce the value of each resistor R somewhat below the value otherwise adequate for forcing voltage sharing between the SCR's.

Proper functioning of the type of protection shown in Figures 11.6 and 11.7 requires that:

1. None of the circuit breakers in series with the SCR's should trip on DC overloads or faults. Separate protection in the AC or DC lines should disconnect the load from the supply voltage for this type of fault.
2. Adequate SCR and circuit breaker capacity should be provided to handle the maximum load current with one of the parallel paths removed from the circuit by operation of a breaker.
3. In isolating a pair of SCR's, the circuit breaker must cut off the current at a slow enough rate so that induced voltage (L di/dt) does not exceed the transient voltage rating of the SCR's in parallel with that pair. If they occur, excessive transient peaks may be reduced to tolerable levels by means of transient suppression techniques (Chapter 12).

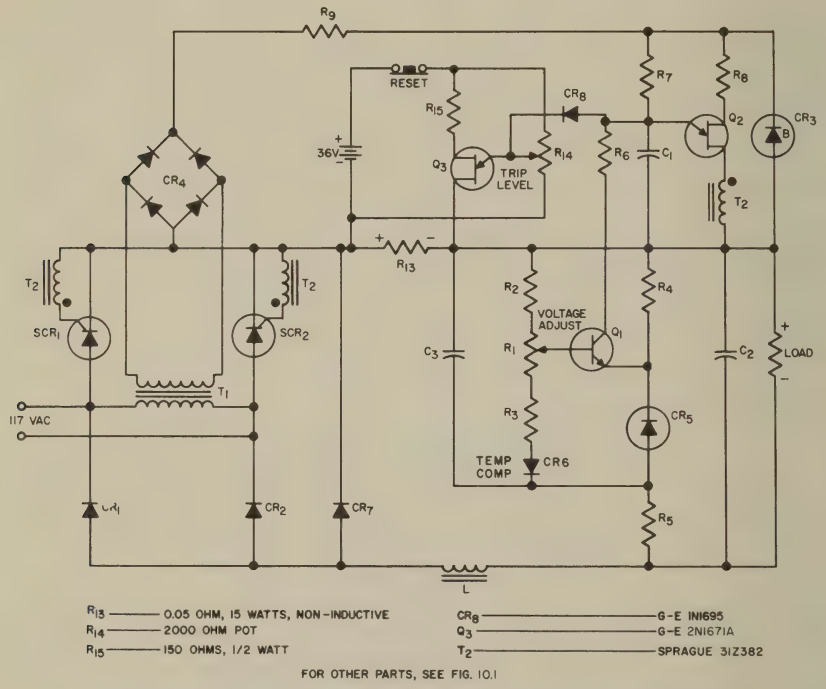
In some applications it may suffice to provide protection only against the possibility of SCR's and rectifier diodes failing by losing their reverse voltage blocking ability (shorting). In this event, the protective scheme can use current limiting fuses in simple parallel paths in a manner identical to that used for protecting diode rectifier circuits.[12] This type of protection presupposes that

satisfactory operation can take place at least on a temporary basis with SCR's still in the circuit that have failed either by failure mode 2 or 3 above.

11.8 OVERCURRENT PROTECTION USING GATE BLOCKING

In many phase-controlled and inverter type circuits, the SCR's and other circuit components can be protected against overcurrent conditions by removing the gate firing signal from the SCR's as soon as excessive current is detected in the circuit. In a phase-controlled system, this will result in fault interruption within one-half cycle after the gate signal has been interrupted since the line voltage reversal will commutate or turn-off the fault current. In an inverter type of circuit operating from DC without line commutation, the gate signal must be interrupted while the fault current is still low enough to be commutated by the circuit parameters.

Figure 11.8 illustrates a typical gate blocking circuit as applied to the phase controlled voltage regulator discussed earlier in Figure 11.8 in Section



Phase Controlled Voltage Regulator with Overcurrent Trip
Figure 11.8

10.1. Under normal operations UJT Q2 develops firing pulses which are coupled to the gates of SCR1 and SCR2 through pulse transformer T2. The firing angle and therefore the average load voltage are controlled by the feedback action of Q1. It diverts charging current from C1, thereby regulating the charging rate

of this capacitor and the firing angle of Q2. UJT Q3, a current sensing resistor R13, and associated components are added to the basic voltage regulator to provide the overcurrent protection feature. Q3 operates from a higher voltage DC supply than Q2 and has a higher standoff ratio than Q2. Q3 therefore fires at a higher emitter voltage than Q2. The voltage between the emitter and Base 1 of Q3 is composed of the voltage developed by the dividing action of R14 and the voltage developed by the flow of load current through the "looking" resistor R13. With no load current flowing, R14 should be adjusted so that the voltage on the emitter of Q3 is higher than the peak point voltage V_P required to fire Q2. Thus until Q3 fires, CR8 will be reverse biased and the normal regulating action of Q2 will occur.

If excessive current now flows in the load circuit, the emitter voltage of Q3 will rise with respect to Base 1 to the point where this UJT fires. Capacitor C1 will discharge through Q3 without developing a gate signal on the SCR's. The resistance between the emitter of Q3 and its positive voltage supply is low enough that Q3 will remain in conduction and keep C1 from charging up again. Under these conditions, Q2 will deliver no firing signal to the SCR's and the load will be disconnected from the AC supply. If the "Reset" button is depressed, Q3 will return to its blocking state, and normal operation will resume provided the overcurrent condition has disappeared. If the fault still remains, Q3 will once more fire, thereby disconnecting the load from the supply, and preventing harm to the SCR's or other circuit components.

Similar gate blocking circuits for protective purposes can be devised for other types of SCR applications where the rate of rise of fault current is not excessive and where means for commutating this current are available.

11.9 SCR SWITCHES AND CURRENT-LIMITING CIRCUIT BREAKERS

SCR switches and circuit breakers may also be used for overcurrent protection systems. Several circuits that can be used for this purpose are discussed in Sections 7.1 to 7.9.

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CHAPTER 12

VOLTAGE TRANSIENTS IN SCR CIRCUITS

In comparison with vacuum and gas tubes, semiconductor devices generally have lower voltage handling capabilities. This applies to SCR's as well as semiconductor diode rectifiers. Because of the sharp transition of their dynamic reverse resistance from a very high value to a very low value in the region of avalanche breakdown, and because of their low thermal capacity, these devices usually have little margin between the value of voltage which they can block satisfactorily in the reverse direction on a continuous basis, and the transient overvoltage which will destroy a cell by shorting in a matter of microseconds. SCR's manufactured by General Electric Co. carry a ¼ cycle non-recurrent transient PRV rating that varies between 20 and 50% above the recurrent PRV rating, depending on the type. This additional PRV capacity is a valuable tool in designing reliable circuits.

As discussed in Section 3.7.4 the forward blocking characteristic of an SCR is usually self-protected by switching into the highly conductive state when V_{BO} is exceeded. However, SCR's with very high values of forward breakover voltage may be damaged before anode voltage reaches V_{BO}.

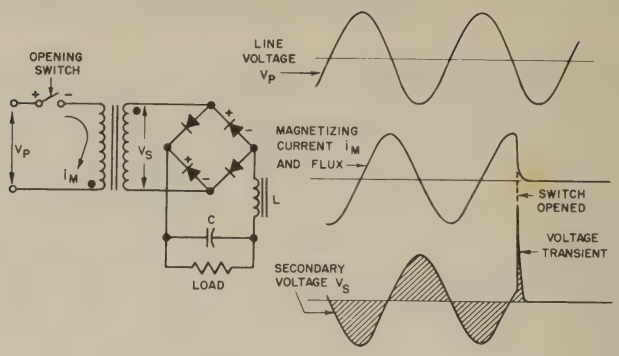
The likelihood and the severity of trouble-making voltage transients tend to be greater in SCR circuits than in simple power diode circuits because of the extremely fast switching action and the high commutating duty possible with SCR's. An understanding of the sources of transient voltages in circuits and the means of reducing them is therefore essential if optimum use of the ratings of SCR's and diode rectifiers is to be achieved.

12.1 WHERE TO EXPECT VOLTAGE TRANSIENTS

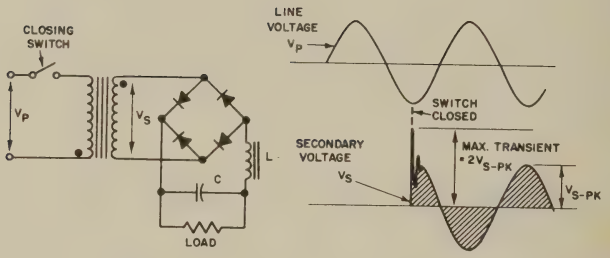
In the following discussion transients are considered to be those voltage levels which exceed the normal repetitive peak voltage applied to the SCR's. In the more common rectifier circuits operating from an AC source, the repetitive PRV applied to the semiconductors is equal to the peak line-to-line voltage feeding the circuit. In inverter circuits and other types of DC switches, the repetitive peak voltage applied to the SCR's is a function of the particular circuit and must be analyzed on an individual basis. Either or both forward and reverse voltage may change widely in normal circuit operation as load current, conduction angle, load power factor, etc., are varied.

In general, the effect of transient voltages on SCR's is similar to their effect on conventional silicon rectifiers, but it should be kept in mind that the SCR is capable of acting as a high resistance in the forward direction as well as the reverse. In some instances, this blocking action will prevent transient energy from being delivered to and dissipated in the load unless the SCR first breaks over in the forward direction.

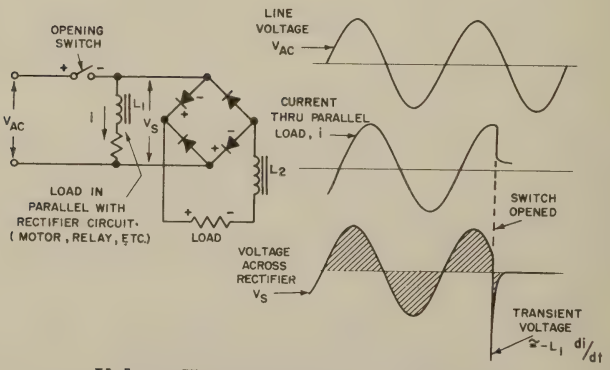
In addition to random line disturbances such as lightning, transient voltages across SCR circuits may be generated by occurrences such as those described in figures 12.1 through 12.8. The indicated diodes may be conventional rectifiers or SCR's.



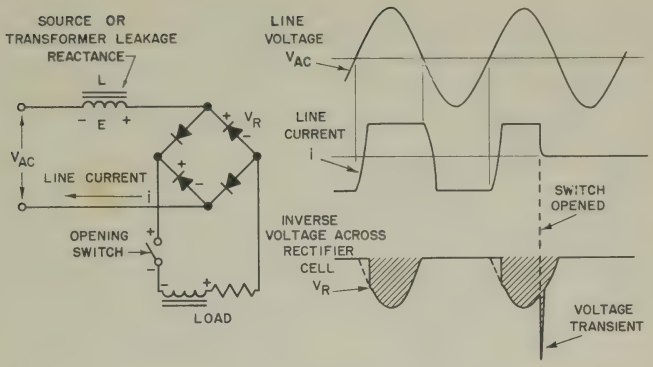
Voltage Transient due to Interruption of Transformer Magnetizing Current
Figure 12.1



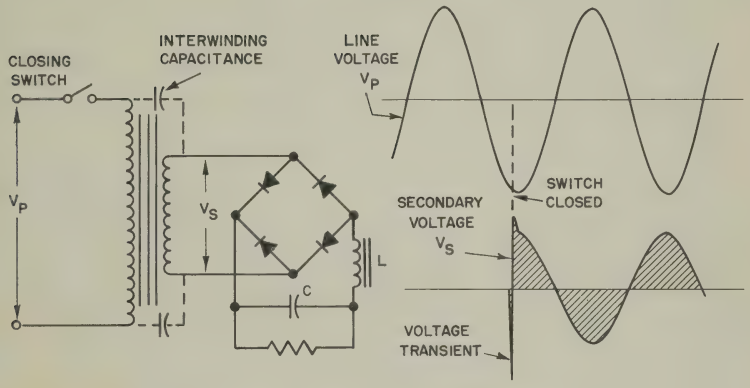
Voltage Transient due to Energizing Transformer Primary
Figure 12.2



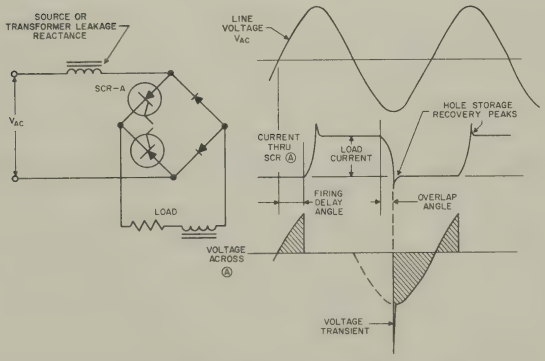
Voltage Transient due to Switching Rectifier with Inductive Load Across Input
Figure 12.3



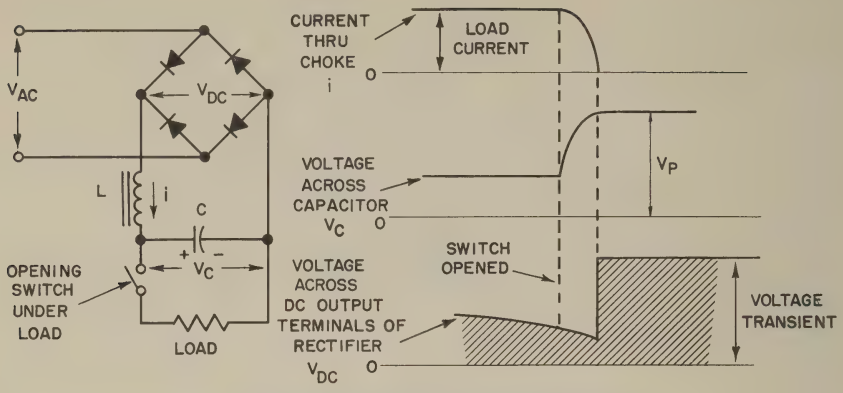
Voltage Transient due to Load Switching
Figure 12.4



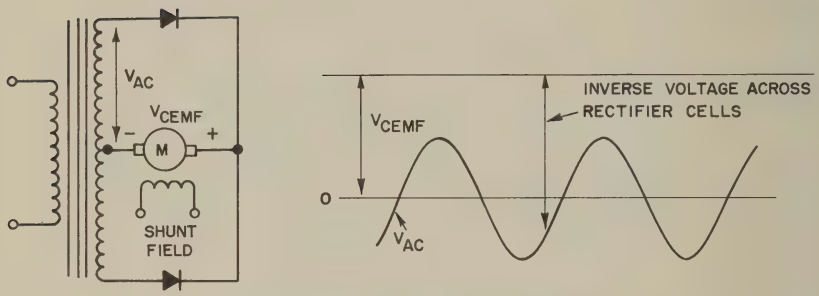
Voltage Transient due to Energizing Step-Down Transformers
Figure 12.5



Cyclical Voltage Transients due to Hole Storage Recovery Phenomena
Figure 12.6



Voltage Transient due to Dropping Load From El-Type Filter with High L/C Ratio
Figure 12.7



Overvoltage due to Regenerative Load
Figure 12.8

Further details on these sources of voltage transients may be found in Reference 7 or in "Rectifier Voltage Transients: Their Generation, Detection and Reduction," Publication 200.11, available on request from General Electric Company, Auburn, New York.

12.2 HOW TO FIND VOLTAGE TRANSIENTS

Only too often the presence of excessive voltage transients in a rectifier circuit is first suspected because of a rash of semiconductor failures in the prototype equipment in the laboratory. Worse yet, these first symptoms sometimes wait until the first equipment is shipped into the field where operating conditions may depart quite radically from the near-ideal conditions that had been successfully passed in the laboratory. When these failures occur at very light loads or immediately following circuit switching, voltage transients should be suspected as the culprit.

Since the search for, and measurement of, possible voltage transients in a circuit may destroy or at least permanently harm SCR's and diodes in the circuit, the anode supply voltage should be reduced to about ¼ or ½ the normal level initially and then gradually increased as measurements indicate the absence or reduction of transients to levels that the semiconductors can withstand.

AC switching transients are usually worst at no load. Therefore, it may be desirable to test the circuit for this type of transient at no load with SCR's and diodes of a lower current rating substituted for the main cells in order to reduce the cost of cells that may be destroyed in the course of the test. Also, the higher blocking resistances of lower current cells will aggravate voltage transients and thus will generally make measurements and corrective measures conservative.

12.2.1 Meters

Except for very slow high energy transients, instruments with moving coils as their detecting and indicating means are almost useless in measuring transient voltages because of their high inertia and low input impedance. Of the several transient voltage problems discussed earlier, this type of meter may be useful only in measuring the amplitude of regenerative voltage transients such as those generated by a hoist motor being driven by an overhauling load.

12.2.2 Oscilloscopes

A high speed oscilloscope with long persistence screen is probably the most useful single tool for analysis of voltage transients. For significant results in detecting and measuring all the types of transients that may cause rectifier failure, the oscilloscope should have a transient response of at least 0.1 microsecond rise-time and be capable of writing rates in excess of ten million inches per second. The Tektronix 530 and 540 series meet this specification. A practical screen material is the P11 phosphor. The Hughes Memoscope, although it is handicapped by its relatively slow writing speed and rise-time, is very useful for recording the longer duration types of transients.

For looking at cyclical transients such as those due to recovery from hole storage effects as discussed in Figure 12.6, the use of a scope is straightforward. In this case, the sweep should be repetitive and synchronized with the power line. However, for non-recurrent types of transients due to switching, more careful precautions are necessary. The scope should be equipped with a hood and for visual inspection the room should be darkened if possible and the eyes of the operator permitted to become accustomed to a low light level. For checking the amplitude of voltage transients visually, it is sometimes more effective not to use a horizontal sweep, but to use instead only the vertical deflection of the trace. Thus, the eyes can be focused on the precise part of the scope face where the transients will appear if and when they occur.

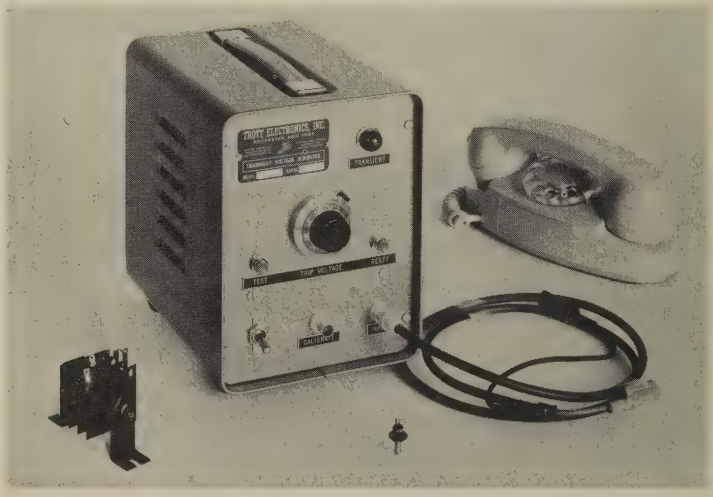
When a sweep is employed, it can be triggered by the transient itself or by some external means such as an extra contact or interlock on the circuit switch. By this latter means, the sweep can be initiated before the transient occurs and any doubt about missing an early part of the transient is eliminated

The objectiveness of studying and measuring non-cyclical types of transients is enhanced if a photographic record is secured in addition to the fleeting image recorded in the mind by the human eye. In many cases, fast film such as Polaroid Pola-Pan Type 42 or 44 (exposure index 200 and 400, respectively) will catch traces that are not perceptible to the eye.

Circuits should be checked for possible destructive voltage transients by connecting the scope input directly across the SCR to be checked.

12.2.3 Peak Recording Instruments

Electronic peak recording instruments with a memory can be very useful in checking for transients when their occurrence is random and cannot be predicted. A simple, easy-to-build instrument of this type is described in a General Electric application note, "A Portable Transient Voltage Indicator for Semiconductor Circuits," 200.16, available upon request. A picture of this instrument is shown in Figure 12.9. This instrument is a "go-no go" type of device for indicating when a transient voltage exceeds the voltage level set on the dial. Accuracy is within 2% maximum setting for voltage pulses down to one microsecond duration. Battery operation increases flexibility of usage and provides continuous operation up to twelve days on one set of batteries. Variations of the basic unijunction-SCR circuitry of this Transient Voltage Indicator permit recording of the frequency of occurrence of voltage transients and the highest transient voltage over an extended interval. Ready-made instruments of this type can be purchased from manufacturers whose names will be furnished on request.



Transient Voltage Indicator
Figure 12.9

12.2.4 Spark Gaps

For high voltage systems, calibrated sphere spark gaps can be used to measure the crest values of transient voltages.[4,5] Current through the spark gap after

it has broken down should be limited by a non-inductive resistance (at least one ohm per volt of test voltage) in series with the gap on the grounded side. Suitable over-current protective devices should be used to interrupt the power follow-through after the voltage surge has passed.

12.3 WHAT TO DO ABOUT VOLTAGE TRANSIENTS

One of the obvious solutions to the transient voltage problem with semiconductors is to provide additional PRV capability by using cells with higher voltage ratings or additional cells in series. This alone is usually not the most economical answer. Normally the best solution will lie in a reasonable safety factor of cell PRV (2-3 times the repetitive circuit PRV) combined with suitable steps to reduce the amplitude of the transients to this rectifier rating. In circuits using SCR's, economical protection of the SCR reverse characteristic against transients can be achieved by inserting a conventional diode rectifier in series with the SCR. Where the leakage currents are comparable, no shunting resistors for voltage equalization are necessary. If the leakage currents are substantially different, suitable shunting resistors should be used. Their resistances should be in proportion to the rated PRV of the respective devices across which each is connected.

The elimination or reduction of voltage transients in rectifier circuits entails in one form or another slowing down the rate of dissipation of stored circuit energy across the rectifier cells. To accomplish this, one has a number of alternatives:

a. Changing the location of the switching elements or the sequence of switching.
b. Changing the speed of current interruption by the switching elements.
c. Providing additional energy storage or dissipation means in the circuit.

An example of the first alternative is to perform switching in the transformer secondary rather than in the primary or load circuits. Since the primary must ultimately be opened, it may be possible to interlock this operation so that the rectifiers are disconnected from the transformer before the primary is opened.

A switch or fuse that does not interrupt or chop current too abruptly will in itself tend to limit transients to lower levels. This is the second alternative. This type of interrupting device will dissipate the stored circuit energy in its arc. The following list can be used as a guide in selecting switches for low recovery voltage. The list is based on laboratory measurements on samples of each type of switch on a 115 volt 60 cycle circuit. The switches are listed in the order of increasing recovery voltage.

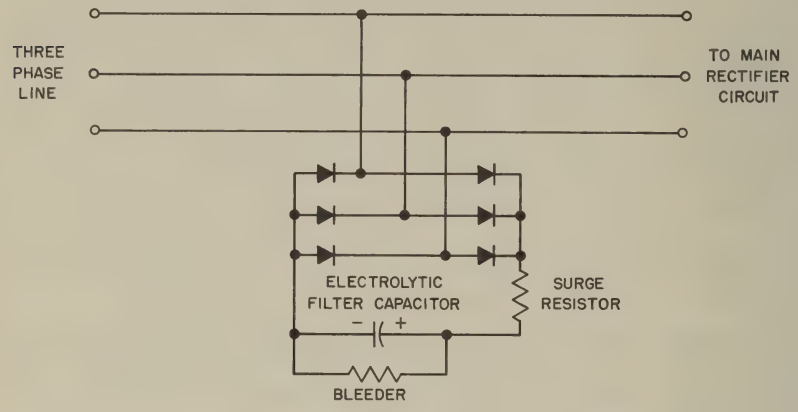
a. Relays (lowest transients)
b. Circuit-breakers
c. Snap switches (including microswitches)
d. Mercury switches
e. Vacuum switches (highest transients)

The third alternative entails any number of various schemes for storing and dissipating the circuit energy.

12.3.1 Capacitors

Capacitive filters are probably the most commonly used type of suppressor for low energy transients of the type shown in Figures 12.1 through 12.7. Filters of this type should be placed across the input lines to the rectifier circuit or across the rectifiers themselves.

Figure 12.10 illustrates how the ripple voltage on a filter capacitor in an AC system may be reduced. By connecting the capacitor behind a double-way rectifier as shown in this illustration, a single capacitor is effective in filtering



Use of Electrolytic Capacitors for Surge Suppression on AC Systems
Figure 12.10

transients that may occur between any of the lines in a three phase system. What would otherwise be 100% ripple voltage on the capacitor is reduced to approximately 5% and the economical energy storage capabilities of polarized electrolytic capacitors may be used to good advantage.

Filter capacitors over approximately .01 μfd may need series resistance to keep them from oscillating with distributed circuit inductance when shocked by a voltage wavefront. When capacitors are connected across the AC line this resistance should be in the order of 5 to 20 times the rated load resistance of the circuit. Final selection of resistance should be based on experimental optimization. Series damping resistance is particularly required in so-called "snubbing" circuits across SCR's for reducing hole storage recovery transients. For capacitors on the DC side of the rectifier, the series resistance should be large enough to protect the semiconductors against the inrush charging current to the capacitor when the circuit is energized initially. The cell manufacturer usually provides surge resistor selection charts for capacitor input filters of this type. The minimum resistance requirement is a function of the capacitance, the supply voltage, and the semiconductor characteristics (I^2t).

Since any inductance in series with the filter capacitor will reduce its effectiveness in suppressing transient voltages, care should be taken in selecting resistors with minimum inductance. Carbon resistors are favored over wire wound types, and capacitors with low self-inductance should be used for the

same reason. Since the higher values of electrolytic capacitors may have considerable inductive reactance at high frequencies, it often is helpful to shunt this type with a high frequency type of capacitor (0.1-1.0 μfd) to handle these components of the transient.

The size of capacitor required for a particular suppression job is a function of many circuit parameters such as the load current level, the transformer characteristics, and the speed of interruption of switching. Thus it is difficult to predict with any degree of accuracy the optimum size of capacitance. As with the other means of energy storage and dissipation discussed in the following material, actual transient measurements on the prototype equipment will determine the optimum values of filter elements required.

The following equation has proved useful in selecting ample filter capacitance values for one of the most common and severe sources of transient voltages; opening the transformer primary under no load or with inductive load (Figure 12.1):

$$C = \frac{VA}{31\ f\ (V_{pk})^2}$$

where C = filter capacity in farads

VA = volt-ampere rating of transformer

f = supply frequency, cps

V_{pk} = peak transient voltage rating of each leg of the rectifier circuit

For evenly distributing the hole storage recovery voltage transient (Figure 12.6) across long series strings of SCR's and diodes, capacitors should be connected across individual cells. The required capacitor size depends on the difference in recovery time between rectifier cells. In any event, it need not exceed:

$$C = \frac{10\ I_r}{V}$$

where C = maximum capacitance to distribute recovery transient within cell PRV rating, microfarads

I_r = amperes flowing through cell immediately preceding commutation

V = maximum continuous PRV rating of the cell, volts

This value is conservative and can be reduced by experimental optimization.

Capacitors across individual rectifier cells in long series strings are also used to distribute the effects of steep voltage waveforms impressed on the circuit. Because of capacitance between cells and ground, voltages with steep rates of rise would otherwise tend to "crowd" across those cells furthest from ground electrically.[3]

12.3.2 Resistance

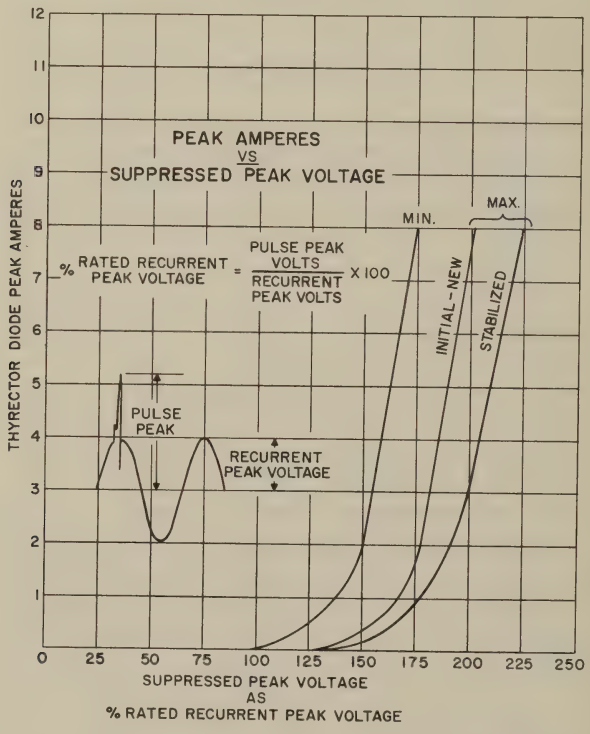
Ample resistive loading across individual legs of the rectifier circuit or across the AC input also provides a means for dissipating stored circuit energy

without driving the voltage up to intolerable levels. Care must be taken to keep inductive effects in the resistors to a minimum so that they may dissipate high frequency components as well as lower ones. The disadvantage of the resistance loading approach is the inefficiency that it introduces to the overall circuit since these resistors dissipate substantial energy at normal voltage levels as well as during transient occurrences.

In circuits where the rise-time of transient overvoltages is not excessive as in some regenerative types of load (Figure 12.8), a voltage sensitive relay may be used to connect a dynamic braking resistor when the DC bus voltage rises to a predetermined level, and to disconnect it when the overvoltage has subsided.

12.3.3 Thyrector Surge Voltage Suppressors

The recent introduction of Thyrector surge voltage suppressors by the General Electric Company has greatly reduced the transient voltage protection problem for power semiconductors. These compact non-linear resistances are essentially selenium "zener" diodes. In many applications they are far more economical and effective than the foregoing techniques of transient voltage suppression.


PEAK AMPERES
VS
SUPPRESSED PEAK VOLTAGE
MIN.
MAX.
% RATED RECURRENT PEAK VOLTAGE = PULSE PEAK VOLTS / RECURRENT PEAK VOLTS X 100
INITIAL - NEW
STABILIZED
PULSE PEAK
RECURRENT PEAK VOLTAGE
THYRECTOR DIODE PEAK AMPERES
SUPPRESSED PEAK VOLTAGE
AS
% RATED RECURRENT PEAK VOLTAGE
0 25 50 75 100 125 150 175 200 225 250
1 2 3 4 5 6 7 8 9 10 11 12

Thyrector Diode Characteristics at Ambient Temperature (−20°C to +100°C)
Figure 12.11

Figure 12.11 illustrates the voltage-current relationship of the one-inch square Thyrector diode in an AC circuit. Below rated recurrent peak voltage, the Thyrector surge suppressor draws negligible current. However, as the voltage rises above this point, as would be the case under a transient condition, the Thyrector diode current increases rapidly and dissipates the transient energy. When correctly applied, Thyrector suppressors will generally clip transient voltages at 150 to 200% of the recurrent peaks. The one-inch square Thyrector diode is rated 25 volts RMS continuous. Cells are available in compact series assemblies for any multiple of this voltage. Other Thyrector diode sizes are available for suppressing various transient energy levels. Application notes and specifications are available on request.

12.3.4 Miscellaneous Methods

Several other transient suppression means may be used to good advantage depending on the particular circumstances of the application. Spark gaps may be used in high voltage circuits provided the precautions outlined in Section 12.2 are maintained.[6] With the advent of higher power ratings in avalanche breakdown (Zener) diodes, many interesting possibilities using these devices suggest themselves, particularly in lower voltage circuits. Silicon diodes can be used as discharge paths for the energy stored in inductive circuit elements such as generator fields and magnetic brakes.

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CHAPTER 13

INTERACTION AND RADIO FREQUENCY INTERFERENCE IN SCR CIRCUITS

13.1 INTRODUCTION

Due to its inherently regenerative turning-on action, the SCR switches very rapidly. In common with other fast switching devices, the SCR tends to shock excite the supply line. Fast rates of rise of current cause voltages to be induced across the distributed inductance of the supply line; in the presence of distributed line capacitance, this causes a redistribution of charge on the supply line. Generally, the redistribution of charge will be oscillatory in nature and at a fundamental frequency determined by the parameters of the supply line. For common types of power distribution lines the fundamental frequency is usually between 250 kc and one or two megacycles per second. As such, the SCR may be considered as a generator of high frequency voltages which can give rise to radio interference or act upon other SCR circuits unless suitable steps are taken.

When acted upon by line disturbances, the SCR circuit may be considered as a receiver sensitive to high frequency voltages. Generally, these voltages act upon the anode of the device directly or they find their way into the trigger circuit and cause the SCR to fire spuriously. In either case the SCR may be acted upon by the operation of neighboring SCR circuits.

13.2 NATURE OF RADIO FREQUENCY INTERFERENCE (RFI)

Basically, two types of radio interference can be identified. One is conducted RFI and the other radiated RFI. In the former case, rf energy is transmitted along the power line and finds its way into other equipment. In the latter case, the equipment causing the interference acts as a small radio transmitter and "broadcasts" the interference which will interfere with other devices capable of "receiving" this energy (see Reference No. 1).

Another very common case related to conducted RFI, but appearing as radiated, is capacitive coupling into a conductor carrying rf energy. This latter form is particularly important where radios, including portable radios, are operated in an environment having rf carrying conductors in relatively close proximity. Residential applications are prime examples of this case.

The following military specifications set quantitative interference levels and give test procedures to which an equipment must be qualified if it is to conform to the specification:

Navy: Mil-I-16910A (14 kc to 1000 kc)
USAF: MIL-I-1681C (150 kc and up) and Mil-I-26600
Army Signal Corps: Mil-I-11748B (14 kc and up)

13.2.1 Suppression of RFI

RFI is an overall systems problem, and it stands to reason that no one step by itself will necessarily eliminate or even satisfactorily attenuate rf noise. The subject must be approached from a systems point of view in which the location of the components, the manner in which they are mounted, the location of wiring runs, etc., must all be taken into account. This subject therefore does not lend itself to the establishing of a few simple quantitative rules to solve every conceivable situation. However, the following will give some approaches which have been found to be successful.

There are two major cases of systems circuitry. In one case an rf ground is not available at the equipment. An example of this is most residential wiring in which the neutral, even if it can be made available, is not necessarily a good rf ground.

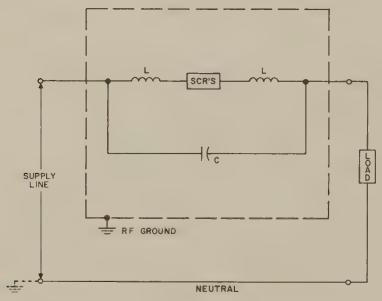
The other case is where an rf ground is readily available. For example, a military power supply may be self contained in a metal enclosure which in turn may be mounted in a metallic rack. Such a large expanse of metal can be considered an rf ground.

The basic approach, as far as the controlled rectifier is concerned, is to localize the initial high rate of rise of current to as small a section of the circuit as possible. This can be done by appropriately placing small inductances in the circuit between which this rate of rise of current is to be localized. Generally, a return path must be furnished for the high frequency component of this current. This path can easily be provided by a small non-inductive capacitor connected as shown in the next section.

13.2.2 Conducted RFI

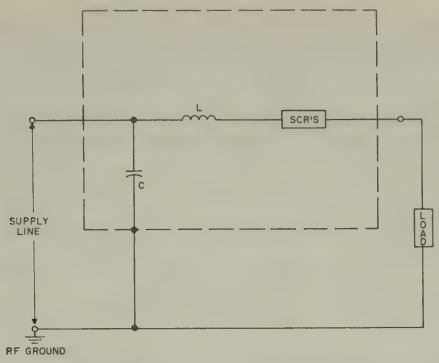
Figure 13.1 shows an RFI suppression approach in a system *not* having an rf ground accessible.*

Figure 13.2 shows an approach in which an rf ground *is* accessible.*



Conducted R.F.I. Suppression With RF Ground Inaccessible Figure 13.1

*These circuits were originally suggested by H. L. Gauper, Jr., of the General Electric Company.



Conducted R.F.I. Suppression With RF Ground Accessible Figure 13.2

The values of the components will depend upon the amount of suppression desired, the layout of the circuit, the nature of the supply line, the nature of the load, and generally the power level of the circuit. In a conventional 117 volt AC supply line and with a load under 1 kw the following values give a good starting point:

L = 60 μhenries (20 turns on Arnold A-930157-2 molybdenum permalloy core)

C = 0.01 μf (ceramic disc)

It may be noted that the inductance need be in the circuit for only the few microseconds of the turn-on switching interval. For this reason the size of the inductance, even in high capacity circuits, will be quite small since the inductance may be allowed to saturate after the turn-on interval.

It is also of interest that the nature of operation of the SCR is relatively unimportant in connection with the generation of RFI. In other words, the same general considerations in suppressing RFI are equally valid in a phase controlled system as they are in an inverter or chopper system. It is generally found that the more conducted RFI is suppressed, the greater will be the radiated RFI. For this reason, it is not advisable to limit conducted RFI below levels required by applicable specifications.

13.2.3 Radiated RFI

With regard to radiated RFI, the best approach to date has been electrostatic shielding. This is another good reason for confining the high rate of rise of current to as small a volume as practical. The dashed line in Figures 13.1 and 13.2 indicate the volume of the circuit that should be enclosed within the shielding. The shielding is then brought to a solid rf ground.

13.3 INTERACTION

Here the SCR system acts as a "receiver" of voltage transients generated elsewhere in the circuit. These transients act either (or both) on the SCR trigger circuit or directly on the anode of the SCR in the main power circuit.

Interaction will cause the SCR system acted upon to completely or partially follow, or track, another SCR system. Also, various types of partial turn on, depending on the nature of the trigger circuit, have been known to arise. Elimination of interaction phenomena must take total system layout into consideration. Section 13.5 gives some general design practices which should be followed to minimize possible sources of interaction. Beyond good design practice in the system as well as in triggering circuits very specific steps for decoupling can be taken as outlined below for UJT circuits.

13.3.1 Interaction Acting on Anode Circuit

When an SCR circuit is acted upon with its gate circuit disconnected (open gate or terminated per specification bulletin) the nature of the interaction is usually attributable to a rate of rise of forward voltage (dv/dt) phenomenon. When energizing the circuit, such as by a contactor or circuit breaker, applicable dv/dt specifications for the device must be met. This subject is discussed in detail in Chapter 3. Once the circuit is energized the SCR will sometimes respond to high frequencies superposed on the anode supply voltage. For example, a 1-megacycle oscillation having a peak amplitude of 10 volts would have an initial rate of rise in the order of 60 volts per microsecond. Applicable specifications for the SCR must meet this condition or steps should be taken to attenuate the rate of rise of voltage.

Due to the nature of anode circuit interaction it is rare that an SCR will track another SCR circuit over the full control range of phase control. Usually, it will tend to lock in over a very limited range near the top of the applied anode voltage half cycle where its sensitivity to dv/dt is greatest. The best means of suppressing this type of interaction is to increase the dv/dt withstand capability of the SCR or, conversely, to reduce the rate of rise of positive anode voltage. Negative gate bias, a small capacitor (not over .1μf) connected directly across the SCR, an RC network elsewhere in the circuit, or a combination of these steps is therefore recommended. The effect of negative bias on dv/dt withstand capability of an SCR is discussed in Chapter 3. When using capacitors in transient suppression work it must be borne in mind that only low inductance capacitors with very short lead lengths should be used. In addition, of course, good circuit layout and system practices should be observed as outlined in Section 13.5.

13.3.2 Interaction Acting on the Trigger Circuit

There are basically two cases to distinguish here:

1. The trigger circuit is acted upon from the supply line directly;
2. The trigger circuit is acted upon from the SCR gate circuit.

Both of these mechanisms may cause the trigger circuit to fire prematurely, giving rise either to spurious firing or complete or partial tracking of the SCR's in the circuit. The response of the trigger circuit to incoming transients will determine the degree of interaction, if any. There are no general rules for every type of firing circuit. However, in the design of a firing circuit it is well

to take the possibility of interaction into account. The designer will be in the best position to assess the transient susceptibility and stability of his circuit.

When using the unijunction transistor firing circuit there are a few relatively simple steps that can be taken to decouple these circuits against both supply voltage and SCR gate circuit transients. These methods are outlined in the following two sections.

13.4 DECOUPLING THE UJT CIRCUIT AGAINST SUPPLY TRANSIENTS

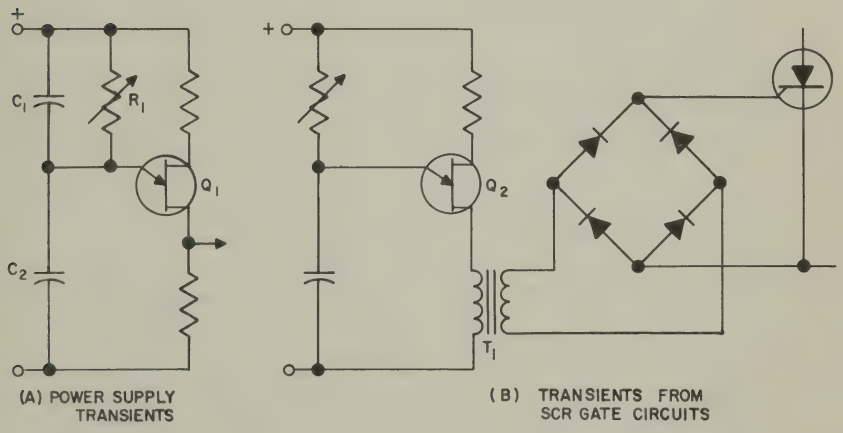
Depending on the nature of the particular circuit conditions, either one or a combination of the following will give effective decoupling against line voltage transients acting on the unijunction transistor firing circuit:

1. Use of control (isolation) transformer with an RF filter across its secondary, if necessary;
2. Use of "boot strap" capacitor between base two and the emitter of the unijunction transistor;
3. Use of a Thyrector diode connected across the supply to the unijunction circuit.

The value of the "boot strap" capacitor C_1 should be chosen so that the voltage divider ratio of C_1 and C_2 in Figure 13.3(A) is approximately equal to the intrinsic standoff ratio of the UJT, or:

$$\frac{C_1}{C_1 + C_2} = \eta \tag{13.1}$$

If this condition is met, positive or negative transients on the unijunction supply voltage will not fire the UJT.



Circuits for Elimination of Erratic Firing From Voltage Transients in UJT Circuits
Figure 13.3

13.5 DECOUPLING UJT CIRCUITS AGAINST SCR GATE TRANSIENTS

Negative voltage transients appearing between the gate and cathode of the SCR's when transmitted to the UJT can cause erratic firing. When transformer coupling is used, these transients can be eliminated by using a diode bridge in the gate circuit of the SCR as shown in Figure 13.3(B). Negative transients often arise in SCR gate circuits in impulse commutated circuits (see Chapter 9) and under certain conditions in AC phase control circuits.

13.6 GOOD DESIGN PRACTICES TO MINIMIZE SOURCES OF SCR INTERACTION

Radio frequency interference and interaction are both total system phenomena and no one step is necessarily the most effective in attaining the desired level of suppression. A combination of good system design practices, good circuit layout, good equipment layout, and, if necessary, a small amount of circuit filtering, as was outlined above, will suppress RFI to acceptable levels and eliminate various types of interaction phenomena.

When the following system considerations are met it is often unnecessary to take additional specific steps to filter either trigger or anode circuits:

1. Operate parallel and potentially interacting SCR circuits from a stiff (low reactance) supply line;
2. If supply line is soft (high reactance), consider using separate transformers to feed the parallel SCR branch circuits; each transformer should be rated no more than the required rating of the branch circuit load;
3. Avoid purely resistive loads operating from stiff lines—they give highest rates of current rise on switching;
4. Keep load moderately inductive—limiting rate of current rise on switching is in the direction of attenuating RFI and minimizing the possibility of interaction;
5. Keep both leads of a power circuit wiring run together—avoid loops that encircle sensitive control circuitry;
6. Arrange magnetic components so as to avoid interacting stray fields.

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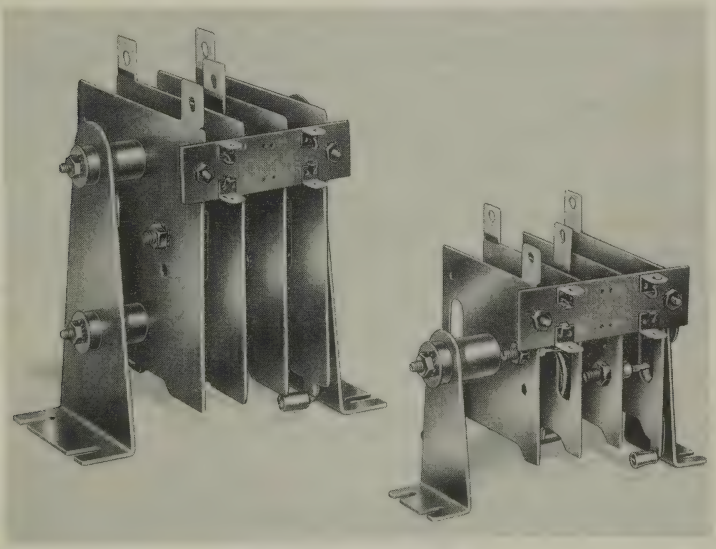
CHAPTER 14

COOLING THE SCR

Successful application of SCR's depends to a great extent on adequate cooling of these devices. If junction temperature of an SCR rises high enough, permanent damage may occur in its characteristics and the device may fail by melting and thermal runaway. Circuits may fail before melting or thermal runaway in the SCR occurs since insufficient cooling can reduce V_{BO}, increase SCR turn-off time, moving these and other SCR characteristics outside specifications sufficiently to induce circuit malfunction.

For these reasons, all SCR's and diode rectifiers are designed with some type of heat transfer mechanism to dissipate internal heat losses. In small lead-mounted semiconductors, such as the 2N1929 and 2N1595 series, temperatures are maintained by radiation and convection from the surface of the case and by thermal conduction down the leads. Higher rated units are manufactured with a cooling fin in order to increase dissipation by radiation and convection. Figure 14.1 shows typical examples of General Electric natural convection cooled SCR's assembled into stack assemblies. Various fin sizes and configurations provide conservative cooling of each SCR type in the General Electric line. Literally tens of thousands of pre-wired circuit combinations are available, and associated diode rectifiers can be assembled integrally in the same stack. Local General Electric sales engineers can provide more information about these SCR stack assemblies and how they can fit diversified application requirements.



Typical General Electric
Pre-wired SCR-Rectifier Stack Assemblies
Figure 14.1

Because of space restrictions and other unique considerations, some applications cannot conveniently use SCR factory-assembled cooling stacks. For these installations, the stud-mounted SCR is a particularly flexible component and has wide acceptance. This type of SCR uses a copper stud with a machine thread for making mechanical and thermal contact to a heatsink of the user's choosing. The heatsink itself may consist of a busbar, chassis, liquid cooling system, or a special cooling fin for dissipation of heat to the surrounding air.

14.1 MOUNTING THE STUD TYPE SCR

If the heatsink is to perform an optimum cooling job, the semiconductor stud must be mounted not only in a good location on the heatsink, but also in such a manner as to achieve low thermal resistance to heat flow from the stud to the heatsink. Proper mounting is not always a straightforward simple matter. Several precautions and considerations should be considered.

14.1.1 Selection of Heatsink Materials

Maximum cooling effectiveness calls for copper as the heatsink material because of its high thermal conductivity. However, cost considerations may dictate steel instead, and in some cases weight and ease of extrusion may bring aluminum into the picture. Two significant factors should be considered particularly for aluminum heatsinks.

Where moist or corrosive atmospheres will be expected, galvanic action between aluminum and the copper stud may lead to gradual deterioration of the joint, and an increase in thermal resistance. A good nickel or silver plate over the copper stud as provided on General Electric SCR's, combined with use of a corrosion inhibitor, such as Burndy-Penetrox A, Alcoa No. 2, or Penn-Union Cual-Aid, minimizes corrosion at this joint.

When mounting copper studs to an aluminum fin through a clearance hole by means of a nut on the backside, thermal ratcheting may cause the mounting to gradually loosen as the assembly is cycled through temperature extremes. This results from the unequal temperature coefficients of aluminum and copper. As the assembly heats up, the aluminum expands faster than copper and stresses beyond their elastic limits may be applied to the respective materials by the sandwiching action of the copper stud and its nut. This causes a permanent deformation in the materials. When the assembly is again cooled down, contact pressure between the surface will be less. Use of a pressure Belleville spring washer on the reverse side of the fin minimizes this effect by allowing the aluminum to expand against washer compression rather than against the copper.

14.1.2 Hole and Surface Preparation for Fin Mounting

When studs with machine threads are mounted to thin flat fins through a clearance hole, optimum heat transfer depends heavily on adequate contact between the two surfaces. Care should be taken to insure a flat fin, free of ridges or high spots, particularly around the hole. If the hole is punched, the fin

should be subsequently blanked. If the hole is drilled, the burr should be carefully removed. If the stud proper has a fillet where the thread meets the flat surface of the hex, the fin hole should be chamfered to prevent the stud from hanging up on this fillet. Before final assembly, the stud surface itself should be checked for removal of all burrs or peened-over corners that may have occurred during shipping and subsequent handling and that would otherwise cause reduced heat transfer across the surfaces.

14.1.3 Mounting Torque

Good thermal contact between the semiconductor and the heatsink requires adequate pressure between these two surfaces as applied by torque on the threads of the device. However, torque beyond a certain point no longer improves the thermal contact and may mechanically stress the SCR junction and materials soldered or brazed to the stud inside the housing. Permanent damage to the device characteristics may result. For this reason, precise adherence to the manufacturer's torque recommendations is necessary, and a torque wrench should *always* be used in mounting this type of semiconductor. Table 14.1 lists recommended mounting torques for the General Electric line of stud-mounted SCR's and diode rectifiers.

14.1.4 Lubrication of Joint

Any practical thermal joint will have trapped air pockets in the inevitable

Stud Size	Hex Size Across Flats	Typical Max. Recommended Torque (in lb.) (For exact values see spec sheets)	Effective Hex Diameter inches d	Stud Contact Thermal Resistance* °C/Watt			
				Metal to Metal		With 0.005" Mica Insulation	
				Dry	With Silicone Grease	Dry	With Silicone Grease
10-32 NF	7/16"	15	0.46	0.75	0.60	6.5	6.0
1/4"-28	9/16"	30	0.59	0.45	0.35	4.0	3.5
1/4" 28	11/16"	30	0.72	0.30	0.25	2.5	2.2
1/2"-20	11/16"	150	1.11	0.20	0.15	1.9	1.7

*Values apply for studs tightened down with maximum recommended torque to reasonably smooth, flat surfaces by means of nut and clearance hole mounting. Thermal resistance values are from stud to point on fin at diameter d.

Characteristics of Standard Stud Sizes
Table 14.1

depressions and voids between the surfaces. Since air is a relatively poor thermal conductor, the thermal transfer can be improved by applying a thin layer of silicone grease such as General Electric SS-4006 (Silicone Products Dept., Waterford, N. Y.) to the surfaces before joining. Table 14.1 indicates the improvement in thermal resistance that can be expected for typical stud sizes by use of silicone grease. Use of a tin/lead washer between stud and heatsink has also reportedly improved heat transfer and uniformity of this joint.

14.1.5 Electrical Insulation of Stud from Heatsink

In some applications it is desirable to electrically insulate the stud from the heatsink. Hardware kits for this purpose are available for stud-mounted semiconductors with machine threads in the low and medium power ratings. These kits generally employ a .003 to .005 inch thick piece of mica or bonded fiberglass to electrically isolate the two surfaces, yet provide a thermal path between the surfaces. As evidenced by the data in Table 14.1, the thermal resistance of the joint may be raised as much as ten times by use of this insulation. As in the direct metal-to-metal joint, some improvement in thermal resistance can be made by using silicone lubricant on each side of the mica.

14.2 COOLING FIN DESIGN

The most common means of cooling stud-mounted SCR's is to mount them to a metallic cooling fin. Heat losses at the junction of the semiconductor will then flow down through the stud, into the fin, and will then be dissipated to the ambient air by radiation and either free or forced convection heat transfer. Because the mechanisms of radiation and convection are of distinctly different nature, the so-called heat transfer coefficient (h) for each effect must be calculated separately and combined with the fin effectiveness (η) to determine

Symbol	Definition	Dimensions
A	Surface Area of Fin	$in.^2$
c	Thermal Capacity	watt-sec/lb.°C
h	Heat Transfer Coefficient	watts/$in.^2$°C
k	Thermal Conductivity	watts/°C-inch
L	Length of Fin (in specified direction)	inches
p	Rate of Heat Flow	watts
R_T	Thermal Resistance	°C/watt
T	Temperature	°C
T_S	Surface Temperature of Heatsink	°C
T_A	Ambient Temperature	°C
V	Air Velocity	ft./min.
ϵ	Radiation Surface Emissivity	-
η	Fin Effectiveness	-
θ	Temperature Difference	°C

Basic Thermal Units
Table 14.2

the overall heat transfer coefficient if any degree of confidence is to be placed in the analytical design. The rate of heat flow, p, from the fin to the ambient air can be expressed as follows:

$$p = hA\eta\Theta \tag{14.1}$$

where h = total heat transfer coefficient of the fin
A = surface area of the fin
η = fin effectiveness factor
Θ = temperature difference between hottest point on fin and ambient

Table 14.2 lists these and other symbols used in the following discussion together with their dimensions.

A short discussion on each of the major factors in Equation 14.1 will reveal the variables on which they depend. The examples cited all apply to the same size fin and temperature conditions so that the reader can compare the relative magnitude of each of the various mechanisms of heat transfer.

It should be emphasized that while the individual equations are quite accurate when the conditions on which they are based are fulfilled in detail, the practical heatsink design will depart from the conditions to some extent because of local turbulence in the air due to mounting hardware and leads, thermal conduction down the electrical leads and the mounting for the fin, nearby radiant heat sources, chimney cooling effects caused by other heated devices above or below the cooling fins, etc. Fortunately most of these additional effects enhance rather than reduce the heat transfer. Therefore, it is common practice to disregard these fringe effects in the paper design stages except where designs are being optimized to a high degree. Even in a highly optimized design, precisely calculated values may be subjected to substantial corrections when the design is actually checked in the prototype. The final measure of the effectiveness of the cooling fin will always be the stud temperature which should never be allowed to exceed the manufacturer's rating for a given load condition.

14.3 RADIATION

For stacked fins with surface emissivity of 0.9 or more and operating up to 200°C, the radiation coefficient (h_r) can be closely approximated by the following equation:*

$$h_r = 1.47 \times 10^{-10}\epsilon\ (1 - F)\left(\frac{T_S + T_A}{2} + 273\right)^3 \frac{\text{watts}}{\text{in.}^2\,^\circ\text{C}} \tag{14.2}$$

where ϵ = surface emissivity (see Table 14.3)
F = shielding factor due to stacking (F = 0 for single unstacked fins)
T_S = surface temperature of cooling fin (°C)
T_A = ambient temperature (°C)

Table 14.3 indicates the wide variation in emissivity for various surface finishes. In free convection cooled applications, the radiation component of the total heat transfer is substantial, and it is therefore desirable to maximize radiation heat transfer by painting or anodizing the fin surface.

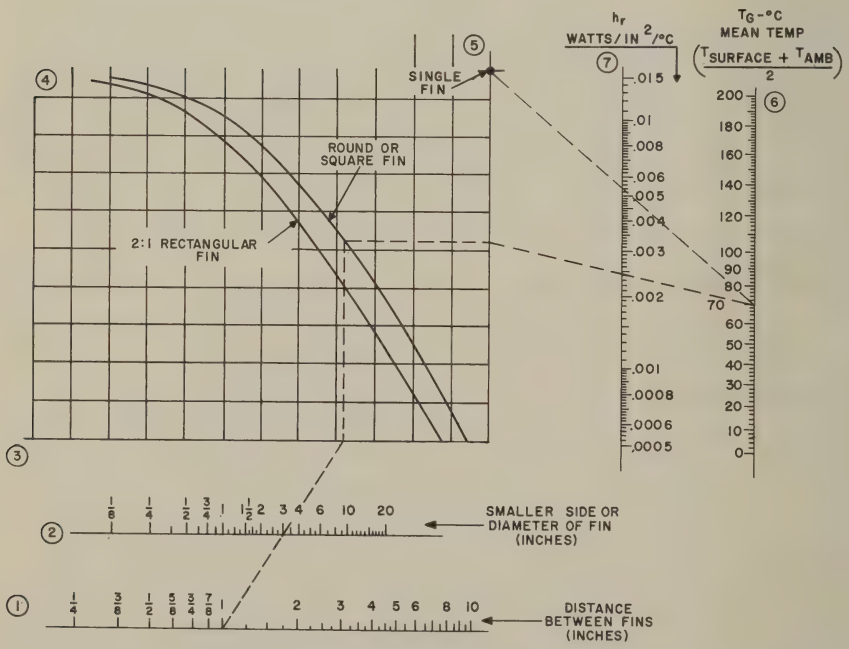
*This equation can be derived from Equations 31-3 and 31-90 in Reference 1.

Surface	Emissivity (ϵ)
Anodized Aluminum	0.7 - 0.9
Commercial Aluminum (Polished)	0.05
Aluminum Paint	0.27 - 0.67
Commercial Copper (Polished)	0.07
Oxidized Copper	0.70
Rolled Sheet Steel	0.66
Air Drying Enamel (any color)	0.85 - 0.91
Oil Paints (any color)	0.92 - 0.96
Lampblack in Shellac	0.95
Varnish	0.89 - 0.93

Emissivities of Common Surfaces
Table 14.3

Note that oil paints regardless of color improve surface emissivity to practically an ideal level (unity).

Figure 14.2 presents Equation 14.2 in the form of a nomogram which considers the detrimental effects of stacking cooling fins. As fin spacing is reduced, shielding effects become more marked, and radiation heat transfer is reduced.



Radiation Nomogram
Emissivity = 0.9
Figure 14.2

14.3.1 Example of Use of Radiation Nomogram

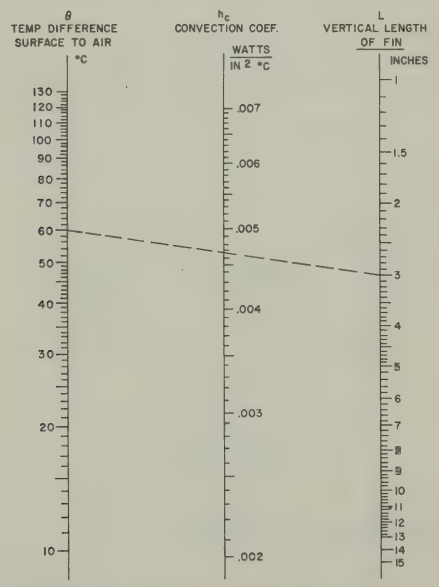
Given: — Stack composed of 3" x 3" square cooling fins
— 1" spacing between fins
— ambient temperature = 40°C
— fin surface temperature = 100°C

Problem: Determine coefficient of radiation heat transfer (h_r) and total radiation heat transfer (p_r) assuming fin effectiveness = 1. (See Section 14.6)

Solution:
$$T_G = \frac{T_S + T_A}{2} = \frac{100 + 40}{2} = 70°C$$

Following the dashed line sequence starting at 1 for the above conditions, $h_r = .0024$ w/in. ^{2}°C.
$p_r = h_r A\Theta =$ (.0024 watts/in. ^{2}°C) (3 x 3 in.^{2}) (2 sides) (100 — 40°C) = 2.6 watts per fin.
For single unstacked fins surrounded by 40°C ambient $h_r = .0054$ watts/in. ^{2}°C by the indicated line on the nomogram.
$p_r = h_r A\Theta =$ (.0054) (3 x 3 x 2) (100 — 40) = 5.8 watts per fin.

14.4 FREE OR NATURAL CONVECTION



Free Convection Nomogram
Vertical Fins — Sea Level Air
Figure 14.3

For vertical fins surrounded by air at sea level and at surface temperatures up to 800°C, the free convection heat transfer coefficient (h_c) can be approximated by the following equation which assumes laminar flow of the cooling medium:[2]

$$h_c = 0.00221\left(\frac{\theta}{L}\right)^{0.25} \quad \frac{\text{watts}}{\text{in.}\ ^{2}\text{C}} \tag{14.3}$$

where θ = temperature difference between surface and ambient air (°C)
L = vertical length of fin (inches)

This equation remains conservative for fin spacing down to approximately $\sqrt[4]{L}$ inch. Figure 14.3 presents Equation 14.3 in the form of a nomogram for convenience.

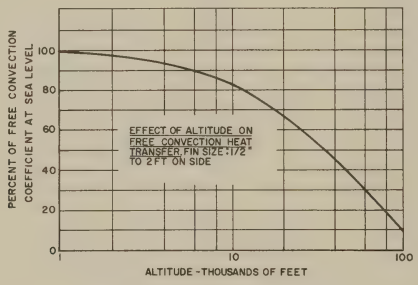
14.4.1 Example of Use of Free Convection Nomogram

Given: — 3" x 3" square cooling fin
— ambient temperature = 40°C
— fin surface temperature = 100°C

Problem: Determine free convection coefficient of heat transfer (h_c) and total convection heat transfer (p_c) assuming fin effectiveness = 1. (See Section 14.6.)

Solution: $\theta = T_S - T_A = 100 - 40 = 60°C$
$L = 3$ inches
As shown by dashed line on nomogram, $h_c = .00465$ watts/in. ^{2}°C.
$p_c = h_c A \theta =$ (.00465 w/in. ^{2}°C) (3 x 3 in.^{2}) (2 sides) (100 − 40°C)
= 5.02 watts.

Altitude derating factors for the free convection heat transfer coefficient are shown in Figure 14.4 for fins from ½ inch to 2 feet on a side.



Effect of Altitude on Free Convection Heat Transfer
Figure 14.4

14.5 FORCED CONVECTION

When air is moved over cooling fins by external mechanical means such as fans or compressors, heat transfer is improved and the convection heat transfer coefficient can be approximated by the following equation:*

*This is accurate within 1% of Equation 7.48, Reference 2, p. 149 for air properties up to 250°C.

$$h_c = 11.2 \sqrt{\frac{V}{L}} \times 10^{-4} \text{ watts/in.}^2 \text{°C} \qquad (14.4)$$

where V = free stream linear cooling air velocity across fin surface (ft./min.)

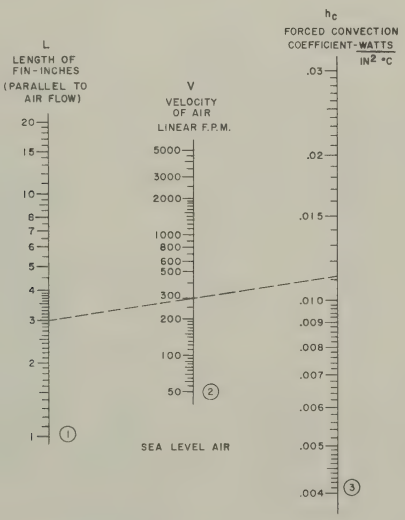
L = length of fin parallel to air flow (inches)

This equation is based on laminar (non-turbulent) air flow which exists for smooth fin lengths up to $L \cong C/V$, where C is a constant given in Table 14.4 for various air temperatures. for $L > C/V$, air flow becomes turbulent and heat transfer is thereby improved. Turbulent air flow and the resultant improvement in heat transfer may be achieved for shorter L's by physical projections from the fin such as wiring and the rectifier cell itself. However, turbulence increases the power requirements of the main ventilating system. Minimum fin spacing for the above is $B\sqrt{\frac{L}{V}}$ inches where B is also a constant given in Table 14.4

Air Temperature	B	C
25°C	3.4	37,000
55°C	3.8	45,000
85°C	4.1	52,000
125°C	4.5	63,000
150°C	4.7	70,000

Laminar Flow Limitations
Table 14.4

Figure 14.5 presents a nomogram for convenience in solving the forced convection equation, Equation 14.4 above.



Forced Convection Nomogram
Figure 14.5

14.5.1 Example of Use of Forced Air Convection Nomogram

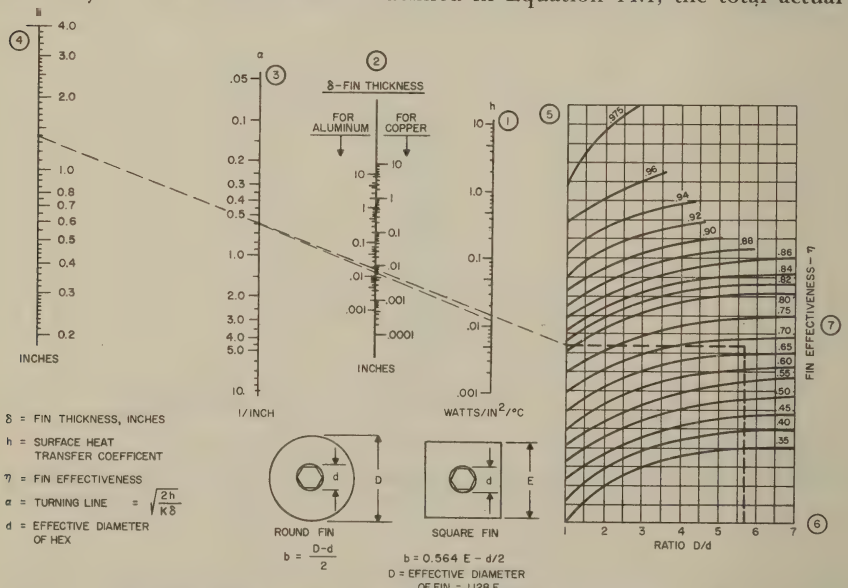
Given: — 3" x 3" square cooling fin
— air velocity = 300 linear FPM
— ambient air = 40°C
— fin surface temperature = 100°C

Problem: Determine forced convection heat transfer coefficient (h_c) and total convection heat transfer (p_c) assuming fin effectiveness = 1.

Solution: L = 3 inches, V = 300 LFPM
As shown on dashed line on nomogram, h_c = .011 watt/in. ^{2}°C.
$p_c = h_c A \Theta$ = (.011 watts/in. ^{2}°C) (3 x 3 in.^{2}) (2 sides) (100 − 40°C) = 11.9 watts.

14.6 FIN EFFECTIVENESS

For fins of thin material, the temperature of the fin decreases as distance from the heat source (the SCR) increases due to effects of surface cooling. Thus calculations of heat transfer, such as those above, which are based on the assumption that the fin is at a uniformly high temperature are optimistic and should be corrected for the poorer heat transfer which exists at the cooler extremities of the fin. The correction factor which is used is called fin effectiveness (η) . η is defined as the ratio of the heat actually transferred by the fin, to the heat that would be transferred if the entire fin were at the temperature of the hottest point on the fin. The hottest spot, of course, is adjacent to the stud of the SCR. The effectiveness depends on the length, thickness, and shape of the fin, on the total surface heat transfer coefficient h, and on the thermal conductivity k of the fin material. As defined in Equation 14.1, the total actual



Fin Effectiveness Nomogram For Flat, Uniform Thickness Fin
Figure 14.6

heat transfer may be calculated by multiplying the fin effectiveness factor by the total surface heat transfer (determined by adding the radiation and convection heat transfer as calculated in the examples above).

Fin effectiveness can be computed by means of the nomogram shown in Figure 14.6. The typical sequence of proceeding through the nomogram is indicated by the encircled numbers adjacent to the scales.

14.6.1 Example of Use of Fin Effectiveness Nomogram

Given:
- — Stack composed of 3" x 3" square painted aluminum fins, each 1/64 inch thick.
- — Effective stud hex diameter d = 0.59 inch.
- — 1 inch spacing between fins
- — 300 LFPM air velocity
- — Fin temperature at stud = 100°C.
- — Ambient air temperature = 40°C.

Problem: Determine total heat transfer of each fin.

Solution:

1st Step: Determine total heat transfer coefficient. Radiation heat transfer coefficient h_r = .0024 w/in. ^{2}°C per example in Section 14.3. Convection heat transfer coefficient h_c = .011 w/in. ^{2}°C per example in Section 14.5.
Total heat transfer coefficient = $h_r + h_c$ = .0024 + .011, h = .0134 w/in. ^{2}°C.

2nd Step: Determine fin effectiveness factor from nomogram.

$$b = 0.564E - d/2 = (0.564)\ (3)\ - \frac{0.59}{2} = 1.39''$$

$$D/d = \frac{1.128 \times 3}{0.59} = 5.64$$

For h = .0134 w/in. ^{2}°C and thickness δ = .0155 inch, α = 0.58 as indicated by the dashed line on the nomogram. Through b = 1.39 and α = 0.58, a line is extended to the graph where D/d = 1. Projecting horizontally on this graph to D/d = 5.64, η is found to be 0.67.

3rd Step: Determine total heat transfer.
Total heat transfer $p = hA\eta\Theta$
$p = (.0134 \text{ w/in.}^2\text{°C})\ (18 \text{ in.}^2)\ (0.67)\ (100 - 40\text{°C})$
$= 7.2$ watts per fin.

For fin materials other than copper or aluminum, use the "copper" scale on the nomogram by multiplying the actual fin thickness by the ratio of the thermal conductivity of the material being considered to the thermal conductivity of copper. Thus, for a ⅛ inch *steel* fin, enter axis 2 on the *copper* scale at 0.125 inch x 1.16/9.77 = 0.015 inch. Thermal conductivities of several commonly used fin materials are given in Table 14.5.

Material	Density (lbs/in. ^{3})	Heat Capacity (c) (watt-sec./lb. °C)	Thermal Conductivity (k) (watts/in. °C)
Aluminum	0.098	407	5.23
Brass (70 Cu, 30 Zn)	0.30	179	2.70
Copper	0.32	175	9.77
Steel	0.28	204	1.16

Thermal Properties of Heatsink Materials
Table 14.5

In general, it will be found that fin thickness should vary approximately as the square of the fin length in order to maintain constant fin effectiveness. Also, a multi-finned assembly will generally have superior fin effectiveness and will make better use of material and weight than a single flat fin.

14.6.2 Typical Example of Complete Fin Design

Given: — Four 2N681 SCR's with 9/16" hex and 1/4" — 28 thread are operated in a single phase bridge at 10 amperes DC maximum each. The specifications for this rectifier indicate that at this current level each SCR will develop 13 watts of heat losses at its junction and that for satisfactory service at this current level, the stud temperature should be maintained below 92°C. The maximum ambient temperature is 40°C and free convection conditions apply.

Problem: Design a stack of fins to adequately cool the four SCR's in this bridge circuit.

Solution:

1st Step: Determine maximum allowable fin temperature at radius of stud hex. From Chart 14.1, the thermal resistance from stud to fin for a joint with silicone lubricant is 0.35°C/watt maximum. The maximum fin temperature therefore must not exceed 92°C — (0.35°C/watt x 13 watts) = 87°C.

2nd Step: Estimate required fin designs based on space available: 6" x 6" painted vertical fins at one inch spacing. Material .08 inch thick steel. Assume all cell losses are dissipated by fin.

3rd Step: Determine surface heat transfer coefficient and fin effectiveness of estimated fin design:

Radiation (from Nomogram in Figure 14.2)

$$T_G = \frac{87 + 40}{2} = 64°C \qquad h_r = .00145 w/in.^2 °C$$

Free Convection (from Nomogram in Figure 14.3)

$$\theta = 87 - 40 = 47°C \qquad \frac{h_c = .0037 w/in.^2 °C}{h_{total} = .0052 w/in.^2 °C}$$

Fin Effectiveness (from Nomogram in Figure 14.6)
D = 1.128E = 1.128 × 6 = 6.768
d = 0.59 from Table 14.1

$$b = 0.564E - d/2 = 0.564 \times 6 = \frac{0.59}{2} = 3.089$$

$$D/d = \frac{6.768}{0.59} = 11.5; \; \delta \, Cu = (.08) \; \frac{1.16}{9.77} = .0095 \text{ in.}$$

Using these parameters in the nomogram, $\eta = 55\%$

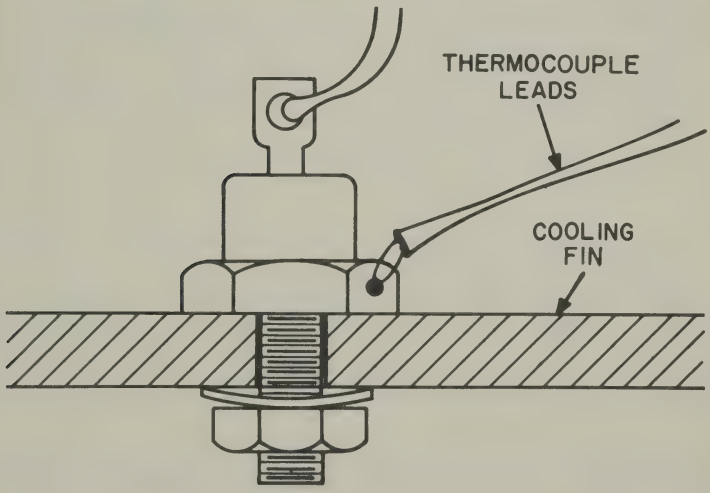
4th Step: Determine total heat transfer for estimated fin.

$p = hA\eta\theta$
$= (.0052)$ (6 x 6 in.^{2}) (2 sides) (0.55) (87 — 40°C)
$= 9.7$ watts

5th Step: Determine error in approximation. Re-estimate fin requirements, and recalculate total heat transfer. In this example, the capabilities of the initial fin design fell below the requirements of 13 watts. To sufficiently increase the heat transfer, the fin could be increased in thickness by approximately 2½ times, or, by using 0.08 inch thick copper instead of steel as fin material, a 5½ inch square fin would be sufficient.

14.7 MEASUREMENT OF STUD TEMPERATURE

Heatsink design should be checked in the prototype equipment. A 10 or 12 mil thermocouple wire should be used. A copper-constantan thermocouple junction is suggested. The thermocouple junction should be carefully soldered to the center of the flat surface on the stud hex as indicated in Figure 14.7. The temperature at this point closely approximates the temperature of the stud



Preferred Location for Mounting Thermocouple for Stud Temperature Measurements
Figure 14.7

immediately below the rectifier junction, which is inaccessible once the cell is mounted to a fin. The point of measurement on the stud should be shielded from any forced air which might cause localized cooling, and the leads should be kept out of any flow of cooling air since they can provide a heat flow path which will lower the temperature at the thermocouple junction.

Unless carefully calibrated leads and instruments are available, a thermocouple bridge rather than a pyrometer should be employed. Care should be taken to keep the thermocouple leads out of electric fields that might induce error voltages in the leads.

As an alternative to using a thermocouple, temperature indicating waxes and paints bearing such trademarks as "Thermocolors" (manufactured by Curtiss-Wright Research Corporation) and "Tempilaq" (manufactured by Tempil Corporation, New York City) can be used to indicate whether the stud exceeds a specific level of temperature. Careful attention should be given to the manufacturer's instructions for using this type of temperature indicator to prevent mis-application and errors. Temperature indicating paints and waxes are particularly useful in high electrical fields where substantial errors may occur in electrical measurement techniques or where the fin is inaccessible for thermocouple leads during the test, such as on the rotor of a rotating machine. Care must be taken in applying paints so their presence does not materially affect the emissivity of the surface.

Use of the foregoing procedures to produce a well-engineered cooling fin design for SCR's can pay big dividends in reliable operation, low material costs, and minimum space and weight requirements.

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CHAPTER 15

TEST CIRCUITS FOR SCR'S

When it is anticipated that SCR's will be used for production purposes, it is essential that some basic equipment be made available for testing the characteristics of SCR's in the factory. The test circuits in this chapter are intended to serve this purpose and several others:

1. Incoming inspection of SCR's.
2. Troubleshooting SCR circuits.
3. Preventive maintenance.
4. Comparison of SCR's of different types and manufacture.
5. Development of better understanding of SCR characteristics.

15.1 TEST CIRCUITS FOR V_{BO}, PRV, AND GATE CHARACTERISTICS

Figure 15.1 illustrates a circuit for testing the forward and reverse blocking characteristics and the gate firing characteristics of all G-E low, medium, and high current SCR's except the very low current SCR's in the TO-5 package. This circuit consists of a variable voltage current-limited power supply that develops a half sine wave voltage across the SCR to minimize junction heating.

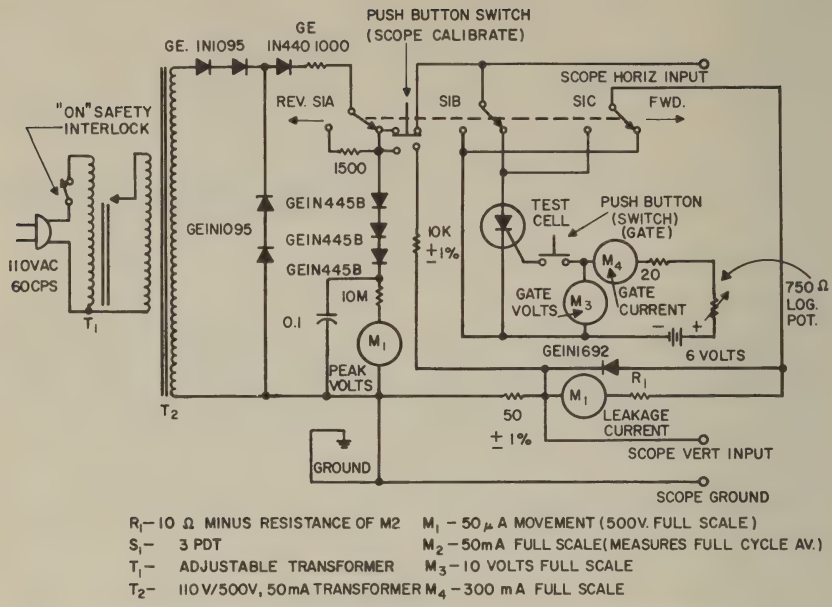
Instrumentation consists of suitable meters to indicate voltage and current values. An oscilloscope with separate horizontal and vertical inputs can be added to provide a visual display of the forward and reverse voltage-current characteristics. Test procedures are as follows:

Scope Calibration

Horizontal deflection on the scope represents the anode voltage on the SCR. Gain should be adjusted to correlate with the reading on meter M_1. Vertical deflection on the scope is developed by the voltage across the 50Ω resistor, and thus represents anode current. With the "Scope Calibrate" button depressed, peak current in milliamperes through the 50Ω resistor is 0.1 times the reading on meter M_1. Vertical gain should be adjusted for 1 or 10 ma per inch.

V_{BO}

Switch S_1 to "Forward" position. Raise voltage by means of adjustable transformer T_1. Read V_{BO} on meter M_1 just prior to breakover as indicated by abrupt rise in reading on M_2 and drop in reading on M_1. Prior to breakover, meter M_2 will read full cycle average leakage current. The scope will trace a plot of the forward voltage current relationship.



R_1 – 10 Ω MINUS RESISTANCE OF M2 — M_1 – 50 μA MOVEMENT (500V. FULL SCALE)
S_1 – 3 PDT — M_2 – 50mA FULL SCALE(MEASURES FULL CYCLE AV.)
T_1 – ADJUSTABLE TRANSFORMER — M_3 – 10 VOLTS FULL SCALE
T_2 – 110V/500V, 50mA TRANSFORMER — M_4 – 300 mA FULL SCALE

Test Set for Measuring V_{BO}, PRV, and Gate Characteristics of SCR's (Except C5 & 1N1595)
Figure 15.1

I_{GF}-V_{GF} Firing Requirements

With switch S_1 in the "Forward" position and M_1 at desired level of anode voltage, depress "Gate" button and gradually raise gate current M_4 by adjusting the 750 ohm potentiometer. Read I_{GF} on meter M_4 and V_{GF} on meter M_3 just prior to breakover. To return the SCR to its forward blocking state, reduce gate current.

PRV and Reserve Leakage Current

Switch S_1 to "Reverse" position. Raise M_1 to the PRV rating of the SCR. Read full cycle average reverse leakage current I_R on M_2 or peak leakage current on the scope display.

Figure 15.2 depicts a V_{BO}/PRV and gate characteristic test set suitable for all TO-5 package controlled rectifiers. Because SCR leakage currents are so small, V_{BO} and PRV measurements must be made at very low frequency, to minimize any errors introduced by stray capacitance charging currents in the test equipment itself. A 2 cps half wave sinusoid (V_{IN}), which can be obtained by amplifying and rectifying the output of a low frequency signal generator to 500 volts peak, is used for this part of the test. Procedure is as follows:

Test Oscilloscope Calibration

With switches S_3 and S_2 both in position (1) adjust R_{19} to give a *peak* voltage reading of 0.5 volts ±5% at terminal V; adjust R_{20} to give 1.0 volt ±5% peak at terminal H. A very high impedance voltmeter must be used to set these figures. The test oscilloscope should now be adjusted for 10 centimeter horizontal and 5 centimeter vertical deflection when connected to H and V.

V_{BO} and Forward E-I Characteristic

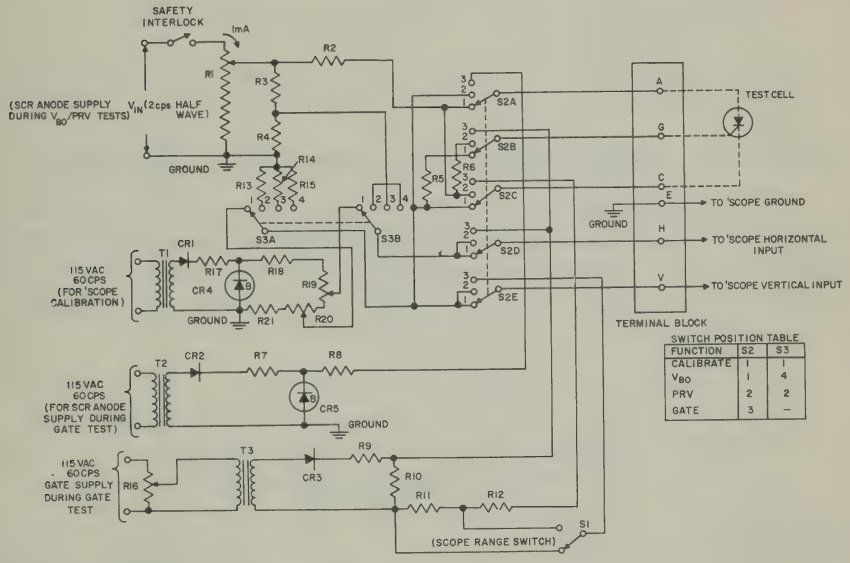
With V_{IN} applied leave S_2 at position (1) and rotate S_3 to (4). Adjust R_1 until cell V_{BO} is indicated by a sudden increase in forward current. Read off V_{BO} and forward leakage current direct from E-I display on oscilloscope.

PRV and Reverse E-I Characteristic

With S_2 at (2) and S_3 at (2) adjust R_1 until oscilloscope trace indicates that rated PRV is being applied to the cell. Read off reverse leakage current at this value of reverse voltage.

Gate Characteristic and Cell Firing Point

V_{IN} is not required for this part of the test. Both anode voltage and gate signal are supplied by self-contained power supplies. Select position (3) on S_2. Increase gate voltage by turning up R_{16} until unit fires. The oscilloscope now displays the SCR gate characteristic; gate voltage and current to fire are indicated by a sudden discontinuity in the E-I trace. Note that once the SCR has fired some fraction of the anode current will flow out of the gate and appear as negative gate current (a discontinuity) on the displayed characteristic.



V_{BO}, PRV Gate Characteristic Test Set for 2N1595, C5
Figure 15.2

Parts List for Figure 15.2

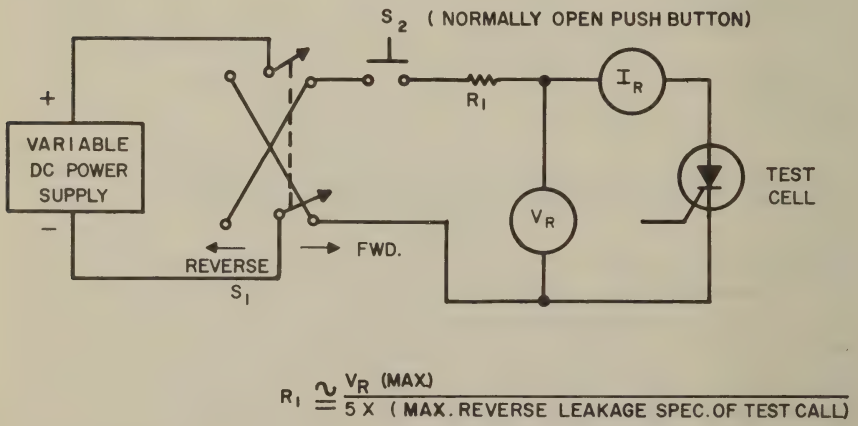
All resistors 10% unless otherwise specified

R_1 — 100K 5 watt carbon potentiometer
R_2 — 47K 1 watt
R_3 — 1M 1% ½ watt
R_4 — 2K 1% ½ watt
R_5 — 1K ½ watt
R_6 — 1K ½ watt
R_7 — 100 ohm 5 watt

R_8 — 600 ohm 1 watt
R_9 — 1K 1 watt
R_{10} — 100 ohm 1% 1 watt
R_{11} — 1800 ohm 1% ½ watt
R_{12} — 200 ohm 1% ½ watt
R_{13} — 10K 1% ½ watt
R_{14} — 2K 1% ½ watt
R_{15} — 1K 1% ½ watt
R_{16} — 5K 2 watt potentiometer
R_{17} — 390 ohm 1% ½ watt
R_{18} — 15K 1% ½ watt
R_{19} — Potentiometer 5K ½ watt
R_{20} — Potentiometer 100 ohm ½ watt
R_{21} — 390 ohm ½ watt
CR_1, CR_2, CR_3 — Rectifier G-E 1N91 (3 required)
CR_4 — Zener Diode 22 volt 1 watt
CR_5 — Zener Diode G-E 4JZ4X6.2B
T_1, T_2, T_3 — Transformer UTC #FT10 (3 required)
S_1 — Switch, SPDT, 110 volt Rotary, Break before make
S_2 — Switch, 5P3T, 1000 volt Rotary, Break before make
S_3 — Switch, DP4T, 110 volt Rotary, Break before make

15.2 DC FORWARD AND REVERSE LEAKAGE

The circuit of Figure 15.3 provides a simple and inexpensive means for checking the instantaneous leakage characteristics of SCR's (or rectifiers). Push button S_2 should not be omitted, as it prevents continuous power from being applied to the cell and reduces the possibility of thermal runaway occurring.



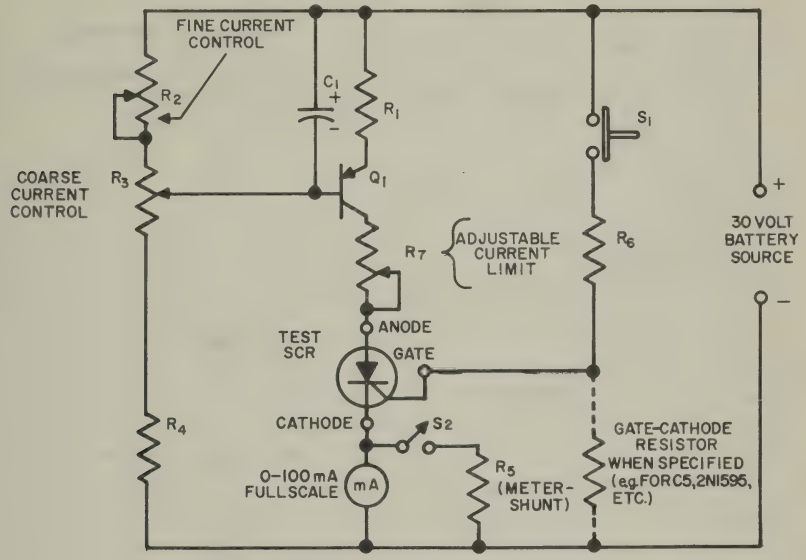
$$R_1 \simeq \frac{V_R \text{ (MAX)}}{5 \times \text{(MAX. REVERSE LEAKAGE SPEC. OF TEST CALL)}}$$

DC Leakage Test Circuit
Figure 15.3

15.3 MEASUREMENT OF HOLDING CURRENT

A simple series circuit consisting of battery, potentiometer, ammeter and test SCR is unsuitable for the measurement of SCR holding current since *smooth* reduction in cell current is not possible with such an arrangement. It has been found that noise and transients generated by a potentiometer as its resistance is increased are sufficient to turn the SCR off at an indicated DC current much higher than its true holding current. The circuit of Figure 15.4 utilizes a transistor as a constant current source to overcome this limitation.

R_3 should be set initially so that fairly high current will flow through the test SCR when S_1 is closed. Current is then progressively reduced, at first using R_3, and finally with R_2 as cell current drops towards its specified holding value. S_2 switches a shunt across the meter to give 1000 ma full scale deflection if required.



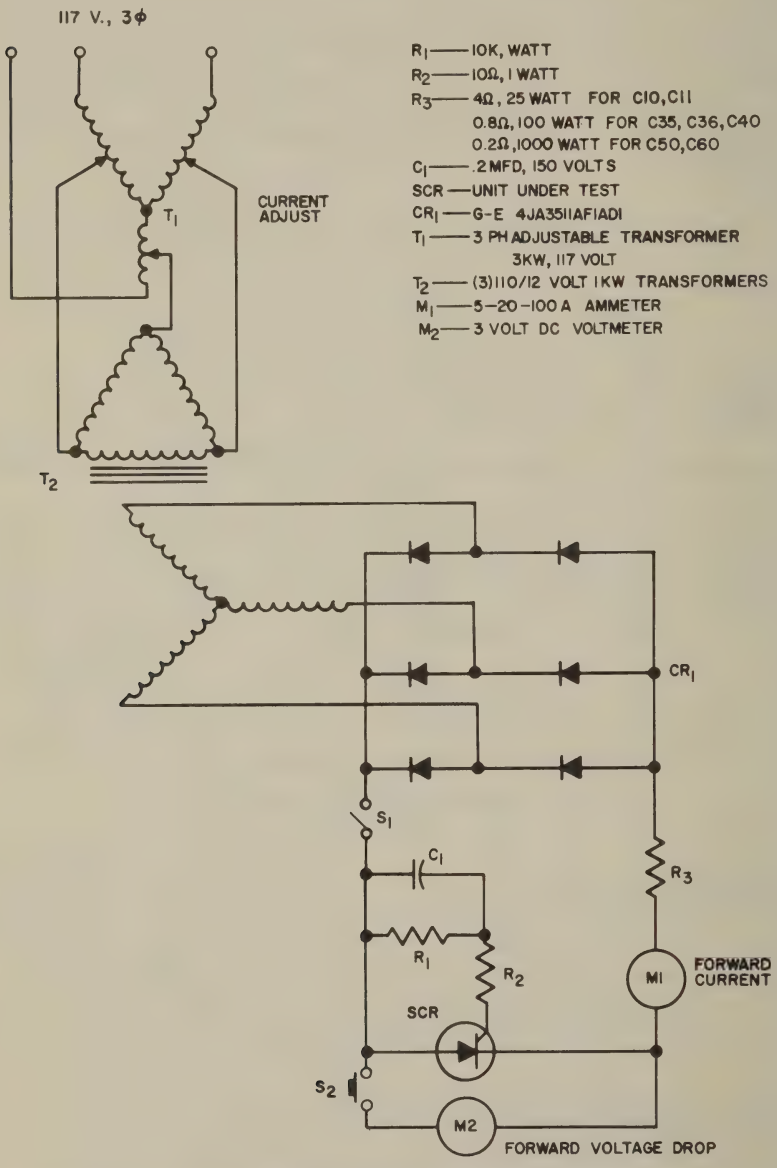
Holding Current Test Set
Figure 15.4

Parts List for Figure 15.4

R_1 — 10 ohm 10 watt
R_2 — 10 ohm 25 watt potentiometer
R_3 — 50 ohm 10 watt
R_4 — 100 ohm 10 watt
R_5 — Shunt for 1000 ma full scale (select to suit meter)
R_6 — 1K 1 watt
R_7 — 50 ohm 25 watt
Q_1 — 2N174 or equivalent
C_1 — 100 μf 25 VDC
S_1 — Normally open push button
S_2 — SPST

15.4 FORWARD VOLTAGE DROP TEST CIRCUIT

The circuit of Figure 15.5 can be used to test the forward voltage drop of the SCR in the conducting state. In this test, the SCR is subjected to a DC current as read by meter M_1, and the voltage drop across the SCR is measured



Forward Voltage Drop Test Circuits for SCR's
Figure 15.5

by meter M_2. To make the measurement, close S_1 with T_1 in a position approximately midway between the end positions. Adjust T_1 to the level of current desired on M_1. Read M_2 by depressing S_2. These readings should be less than the maximum values specified on the forward characteristic curves in the specification bulletin for the particular device. A current level somewhere near the continuous duty current rating of the SCR is recommended. If the SCR is not attached to a heatsink for this measurement, the readings should be completed within two or three seconds to prevent overheating of the cell. The foregoing tests can be conducted at any ambient temperature within the operating range provided that the ratings at the stud temperature are not exceeded.

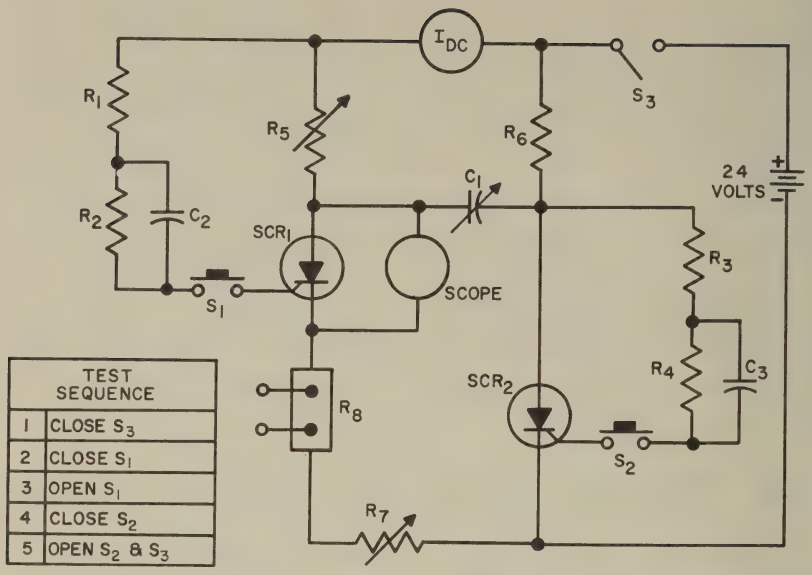
Special oscilloscopes such as the Tektronix Type 575 which are designed to trace transistor characteristic curves may be used for checking the firing characteristics and holding current requirements of SCR's. The power supply in the Tektronix 575 limits maximum anode voltage to 400 volts positive or negative.

15.5 TURN-OFF TIME TEST CIRCUIT

As discussed in Chapter 5, the turn-off time depends on a number of circuit parameters. Thus, a turn-off time specification inherently must include the precise value of these circuit parameters to be meaningful. Accordingly, specifications for General Electric SCR's with guaranteed turn-off limits list the applicable circuit parameters and show the test circuit which will apply these parameters to the SCR. For this information, the reader is referred to the specification bulletin for the SCR under consideration (e.g., C40).

For general turn-off time test work, the type of circuit shown in Figure 15.6 can be used for low, medium, and high current SCR's by proper manipulation of the circuit constants. Forward load current is adjustable by R_5 from approximately ½ ampere to 70 amperes and the length of time SCR_1 is reverse biased during the turn-off cycle can be adjusted by manipulating R_5 and C_1. The peak reverse current during the recovery period can be adjusted by R_7 and this current can be viewed on a scope by monitoring the voltage across a noninductive shunt R_8. If one is interested in only one particular load current range, there is of course no necessity in providing the complete range of resistors and capacitors specified in Figure 15.6.

This test circuit subjects the SCR to current and voltage waveforms similar to those found in a parallel inverter circuit. Closing S_1 and S_3 fires SCR_1, the unit under test, so that load current flows through R_5 and the ammeter. In less than a second C_1 charges through R_6 to the voltage being developed across R_5 by load current flow. If S_2 is now closed, SCR_2 turns on. This applies C_1 across SCR_1 so that the current through SCR_1 is reversed. C_1 furnishes a short pulse of reverse recovery current through SCR_1 until this SCR recovers its reverse blocking ability. After this initial pulse of current, C_1 continues its discharge through SCR_2, the battery, and R_5 at a rate dependent on the time constant of R_5C_1. After a time interval, t_1, in Figure 15.7, somewhat less than the R_5C_1 time constant, the anode to cathode voltage of SCR_1 passes through zero and starts building up in the forward direction. If the turn-off time, t_o, of the SCR



TEST SEQUENCE	
1	CLOSE S_3
2	CLOSE S_1
3	OPEN S_1
4	CLOSE S_2
5	OPEN S_2 & S_3

R_1, R_3 — 100 OHMS, 1 WATT
R_2, R_4 — 1 MEG, 1 WATT
R_5 — VARIABLE RESISTOR, 0.25Ω, 2.5KW TO 50Ω, 15 WATT
R_6 — 1000Ω, 2 WATT
R_7 — 0.1Ω, 500W TO 1Ω, 10 WATT
R_8 — NON-INDUCTIVE SHUNT (IF USED)
C_1 — 0.1–100μfd PAPER CAPACITORS, 150 VOLTS
C_2, C_3, — 0.5μfd – 200 VOLT PAPER CAPACITORS
SCR_1 — TEST CONTROLLED RECTIFIER
SCR_2 — SAME AS SCR_1

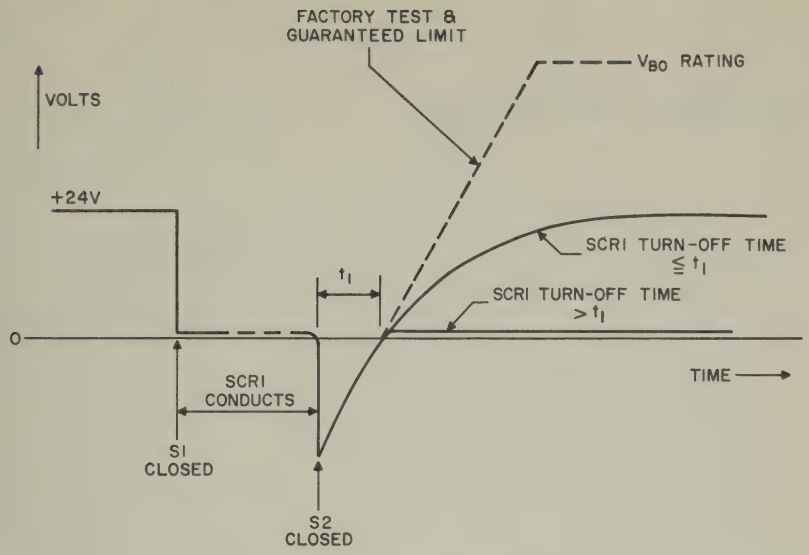
Turn-Off Time Test Circuit
Figure 15.6

Parts List for Turn-off Time Test Circuit

R_1, R_3 — 100Ω, 1 watt
R_2, R_4 — 1 Meg, 1 watt
R_5 — Variable Resistor, .25Ω, 2.5KW to 50Ω, 15 watts
R_6 — 1000Ω, 2 watts
R_7 — 0.1Ω, 500 W to 1Ω, 10 watt
R_8 — Non-inductive shunt (if used)
C_1 — 0.1-100 μfd paper capacitors, 150 volts
SCR_1 — Test rectifier
SCR_2 — Same as SCR_1

is less than t_1, it will remain turned off and the ammeter reading will return to zero. If not, the SCR will turn back on and current will continue to flow until S_3 is opened.

The turn-off interval t_1 can be measured by observing the anode to cathode voltage across SCR_1 on an oscilloscope such as the Tektronix 545 or equivalent. A waveshape similar to that in Figure 15.7 will be observed.



Voltage Across SCR_1
During Turn-Off Time Test
Figure 15.7

Satisfactory operation of this circuit requires careful attention to detail. The DC source must have good regulation if C_1 is to develop ample commutation voltage for turning off SCR_1. In order to minimize circuit inductance, power leads should be heavy copper braid when testing medium and high current SCR's, and lead lengths should be held to an absolute minimum.

Turn-off time testing in the General Electric factory is performed with a fixed rate of rise of reapplied forward voltage as indicated by the dashed line in Figure 15.7. This is a more severe test on the SCR than the exponential curve and it requires considerably more elaborate test equipment than in Figure 15.6. For those who wish to test under these conditions, information on the factory test circuit will be provided upon request. (Ref. 1)

REFERENCE

1. "Turn-Off Time Characterization and Measurement of Silicon Controlled Rectifiers," R. F. Dyer and G. K. Houghton, AIEE CP61-301.

CHAPTER 16

SELECTING THE PROPER SCR

A glance at the SCR specifications in Chapter 17 shows that the designer has available to him a variety of SCR's of different current and voltage ratings (from a few hundred milliamperes to over 100 amperes and up to 500 volts). Also, he has special SCR's with guaranteed turn-off times for certain applications such as inverters.

To apply the SCR correctly, none of its ratings should be exceeded. By the same token it would be uneconomical to apply the device too conservatively. Since SCR ratings and characteristics, as is customary for semiconductors, are specified as maximum or minimum values (worst case), the designer must determine which of the parameters specified are limiting to his particular application. In this manner he is not penalized by application practices that may have been established in other industries. Each parameter is given at its limit, allowing the designer to determine for himself which one is limiting.

The limiting parameter in most applications is usually one like average or RMS current, non-recurrent surge current, operating temperature, turn-off time or voltage, not to mention environmental or mechanical requirements. The chart introducing Chapter 17 can conveniently be used to check some of the important parameters against available SCR's.

The following is a check list of the steps that should be taken or considered in selecting the proper SCR.

1. *Determine Circuit Requirements on SCR*

   Voltage across and current through the SCR must be determined in terms of circuit input and output requirements. Figure 16.1 shows these for some common SCR circuits.

   Note: Check *voltage transients* (Chapter 12).

   Check current carrying capability required if *current waveform is irregular* (Chapter 3).

2. *Select Proper SCR*

   Refer to introductory chart and detailed specifications in Chapter 17. Use voltage and current requirements as determined in step (1).

3. *Determine Proper Heatsink*

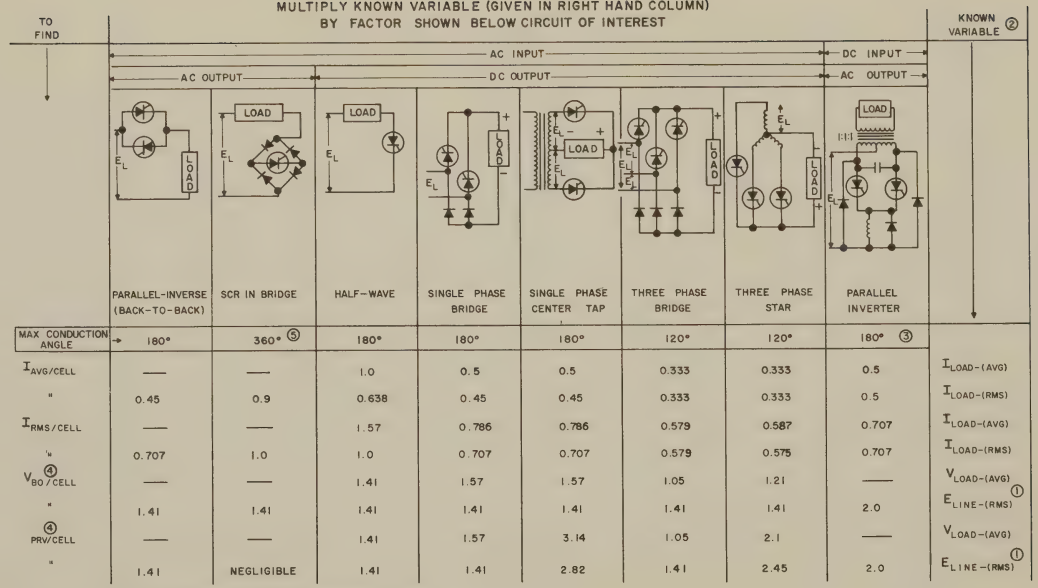
   a. *Check* maximum allowable ambient temperature if a *lead mounted* or *TO-5* package SCR was selected.

   b. *Select* proper size *heatsink* from *fin curves* given on specification bulletin for *stud-mounted* SCR's.

   c. *Determine* proper size *heatsink* from *Chapter 13* if *fin curves* are *not given* for a *stud-mounted* SCR.

4. *Design Firing Circuit*

   See *Chapter 4* for SCR firing requirements and design criteria. Commercially available packaged firing circuits are also listed in Chapter 4.


MULTIPLY KNOWN VARIABLE (GIVEN IN RIGHT HAND COLUMN)
BY FACTOR SHOWN BELOW CIRCUIT OF INTEREST
TO FIND
KNOWN VARIABLE ②
AC INPUT
DC INPUT
AC OUTPUT
DC OUTPUT
AC OUTPUT
LOAD
PARALLEL-INVERSE (BACK-TO-BACK)
SCR IN BRIDGE
HALF-WAVE
SINGLE PHASE BRIDGE
SINGLE PHASE CENTER TAP
THREE PHASE BRIDGE
THREE PHASE STAR
PARALLEL INVERTER
MAX CONDUCTION ANGLE → 180° 360° ⑤ 180° 180° 180° 120° 120° 180° ③
$I_{AVG/CELL}$ — — 1.0 0.5 0.5 0.333 0.333 0.5 $I_{LOAD-(AVG)}$
" 0.45 0.9 0.638 0.45 0.45 0.333 0.333 0.5 $I_{LOAD-(RMS)}$
$I_{RMS/CELL}$ — — 1.57 0.786 0.786 0.579 0.587 0.707 $I_{LOAD-(AVG)}$
" 0.707 1.0 1.0 0.707 0.707 0.579 0.575 0.707 $I_{LOAD-(RMS)}$
④ V_{BO}/CELL — — 1.41 1.57 1.57 1.05 1.21 — $V_{LOAD-(AVG)}$
" 1.41 1.41 1.41 1.41 1.41 1.41 1.41 2.0 $E_{LINE-(RMS)}$ ①
④ PRV/CELL — — 1.41 1.57 3.14 1.05 2.1 — $V_{LOAD-(AVG)}$
" 1.41 NEGLIGIBLE 1.41 1.41 2.82 1.41 2.45 2.0 $E_{LINE-(RMS)}$ ①

① PER TRANSFORMER LEG WHERE TRANSFORMER IS SHOWN.
② WITH NO FIRING ANGLE DELAY
③ ASSUMED PERFECT SQUARE-WAVE OUTPUT.
④ MINIMUM REQUIRED CELL CAPABILITY. ACTUAL VALUE SELECTED MUST BE DETERMINED BY CIRCUIT DESIGNER ON BASIS OF KNOWN AND POTENTIAL VOLTAGE TRANSIENTS.
⑤ WHERE THIS 360° "FULL WAVE" CONDUCTION ANGLE IS NOT GIVEN ON SPECIFICATION BULLETIN USE 180° CONDUCTION ANGLE STUD TEMPERATURE CURVE AND INCREASE CURRENT AS FOLLOWS:

SCR TYPE	
2N1777	50%
2N1777A	50%
2N1842	20%
2N681	20%

⑥ VALUES PERTAIN TO RESISTIVE LOADING.

Circuit Constants for Common SCR Circuits
Figure 16.1

5. *Design Fault Protection*

   Protect SCR's and associated semiconductor components against short-circuit and other fault conditions if required; see Chapter 11. In some applications economic factors and industry practice may preclude or not require protective circuitry coordination.

Beyond these elementary steps there are often other considerations meriting special attention:

1. Series and parallel operation—Chapter 6
2. Radio interference and interaction—Chapter 13
3. Frequency response—Chapters 3 and 5.

CHAPTER 17

GENERAL ELECTRIC SEMICONDUCTOR SPECIFICATIONS

The following pages list condensed specifications of the General Electric line of Silicon Controlled Rectifiers (SCR's), rectifiers, and zener diodes at the time of publication of this Manual. Also shown are abbreviated specifications for the 2N1671 series of Unijunction Transistors. For the latest detailed specification information, please request the specification bulletin for the particular type of interest.

For a definition of the terms used in the specifications that follow please refer to Chapter 2.

The following chart is offered as an index to the G-E line of SCR's:

SCR SPECIFICATION INDEX

JEDEC Type No.	G.E. Type No.	Devel. Type No.	Max. Avg. Single Phase Current	Max. RMS Current	Operating Temp. Max.	Operating Temp. Min.	Max. I_{GF} Required To Fire +25°C	Guaranteed Turn-off Time**	PRV and V_{BO} Up To	Housing Design	Outline No.	Specs. on Page
—	C5	ZJ203	1.0	1.6	125°C	−65°C	200 μa	—	400	Single End Lead Mount	1	250
2N1595-1599	—	—	1.0	1.6	150°C†	−65°C	10 ma	—	400	Single End Lead Mount	1	256
2N1929-1935	C8	ZJ209	2.0	2.7	125°C	−65°C	15 ma	—	300	Double End Lead Mounted	2	261
—	C9	(Inverter)	2.0	2.7	125°C	−65°C	15 ma	12 μsec	300	Double End Lead Mounted	2	308
2N1770-1777	C11	ZJ54L	4.7	7.0	125°C	−65°C	15 ma	—	400	7/16" Hex Stud	3	267
—	C12	(Inverter)	4.7	7.0	125°C	−65°C	15 ma	12 μsec	300	7/16" Hex Stud	3	309
2N1770A-1777A	C10	ZJ54A	4.7	7.0	150°C	−65°C	15 ma	—	400	7/16" Hex Stud	3	274
2N1842-1850	C36	ZJ39L	10	16	100°C	−40°C	80 ma	—	500	9/16" Hex Stud	4	280
2N681-689*	C35	ZJ39A	16	25	125°C	−65°C	40 ma	—	500	9/16" Hex Stud	4	287
—	C40	(Inverter)	16	25	125°C	−65°C	40 ma	12 μsec	300	9/16" Hex Stud	4	310
2N1909-1916	C50	ZJ50L	70	110	125°C	−40°C	70 ma	—	500	1 1/16" Hex Stud	5	294
—	C55	(Inverter)	70	110	125°C	−40°C	70 ma	20 μsec	300	1 1/16" Hex Stud	5	311
2N2023-2030	C60	ZJ50B	70	110	150°C	−65°C	70 ma	—	400	1 1/16" Hex Stud	5	301

*USN Specification 2N681-2N688 MIL-S-19500-108 Available

†No V_{BO} specified above 125°C

**Under Specified Test Conditions

TYPE C5U-C5D
(Former ZJ203 Series)
Outline Drawing No. 1

High Sensitivity Low Current
Silicon Controlled Rectifier
1.6 Amperes

The C5 Silicon Controlled Rectifier is an all diffused three junction semiconductor device for use in very low power switching and control applications.

Type	Minimum Forward Breakover Voltage (V_{BO})* $T_J = -65°C$ to $+125°C$	Repetitive Peak Reverse Voltage (PRV) $T_J = -65°C$ to $+125°C$	Transient Peak Reverse Voltage (Non-recurrent, <5 Millisec.) $T_J = -65°C$ to $+125°C$
C5U	25 volts	25 volts	40 volts
C5F	50 volts	50 volts	75 volts
C5A	100 volts	100 volts	150 volts
C5G	150 volts	150 volts	225 volts
C5B	200 volts	200 volts	300 volts
C5H	250 volts	250 volts	350 volts
C5C	300 volts	300 volts	400 volts
C5D	400 volts	400 volts	500 volts

*With 1000 ohms or less connected from gate to cathode. See Chart 2.

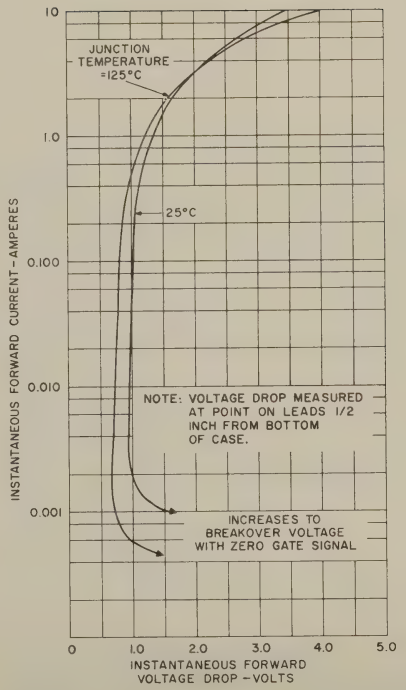
Maximum Allowable Ratings

Repetitive Peak Forward Blocking Voltage (PFV)	500 volts
RMS Forward Current	1.6 amperes
Average Forward Current (I_F)	Depends on conduction angle (See Charts 4 and 5)
Peak One Cycle Surge Current (i_{surge})	18 amperes
Peak Gate Power (p_G)	0.1 watt
Average Gate Power (P_G)	0.01 watt
Peak Gate Current (i_G)	0.1 ampere
Peak Gate Voltage (v_G), Forward and Reverse	6 volts
Storage Temperature	−65°C to +150°C
Operating Junction Temperature	−65°C to +125°C

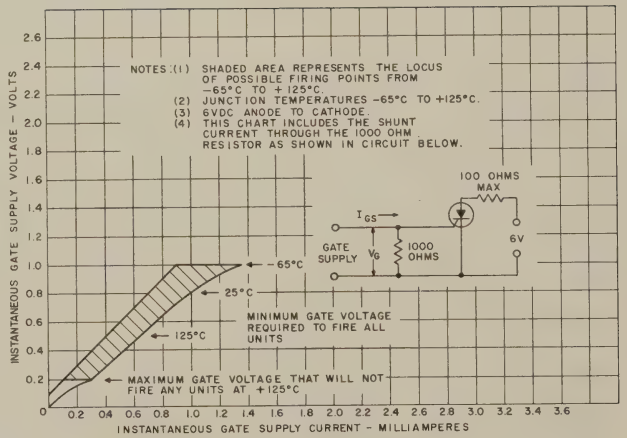
Characteristics

Maximum Reverse (i_r) or Forward (i_s) leakage current—See Chart 7
Gate Firing Characteristics—See Charts 2 and 3
Forward Voltage Drop—See Chart 1
Maximum Holding Current *(I_H) 2.0 ma ($T_J = 25°C$)

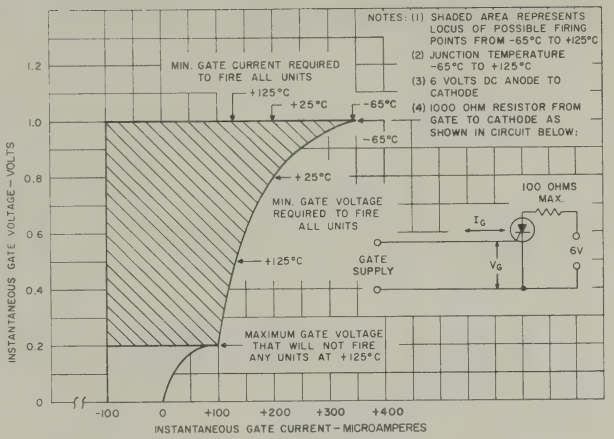
*With 1000 ohms or less connected from gate to cathode. See Chart 2.



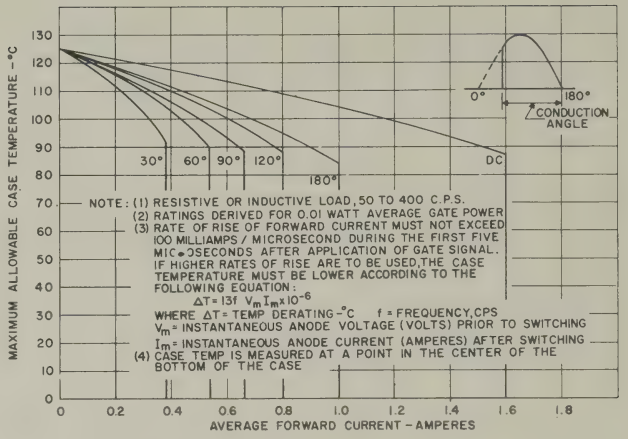
1. Maximum Forward Characteristics Conducting State


NOTES: (1) SHADED AREA REPRESENTS THE LOCUS OF POSSIBLE FIRING POINTS FROM −65°C TO +125°C.
(2) JUNCTION TEMPERATURES −65°C TO +125°C.
(3) 6VDC ANODE TO CATHODE.
(4) THIS CHART INCLUDES THE SHUNT CURRENT THROUGH THE 1000 OHM RESISTOR AS SHOWN IN CIRCUIT BELOW.
100 OHMS MAX
I_{GS}
GATE SUPPLY V_G
1000 OHMS
6V
−65°C
25°C
125°C
MINIMUM GATE VOLTAGE REQUIRED TO FIRE ALL UNITS
MAXIMUM GATE VOLTAGE THAT WILL NOT FIRE ANY UNITS AT +125°C
INSTANTANEOUS GATE SUPPLY VOLTAGE - VOLTS
INSTANTANEOUS GATE SUPPLY CURRENT - MILLIAMPERES

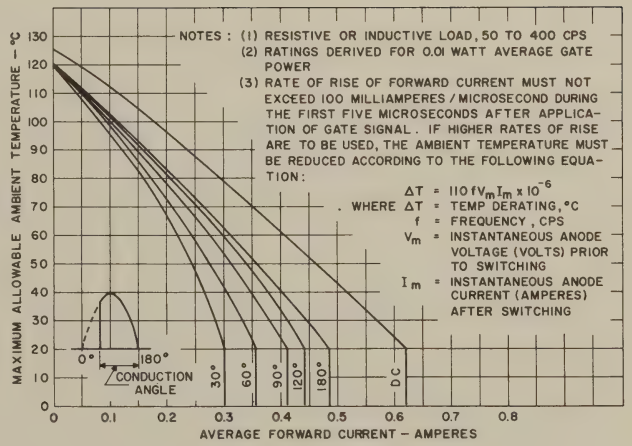
2. Firing Characteristics with External Gate Resistance



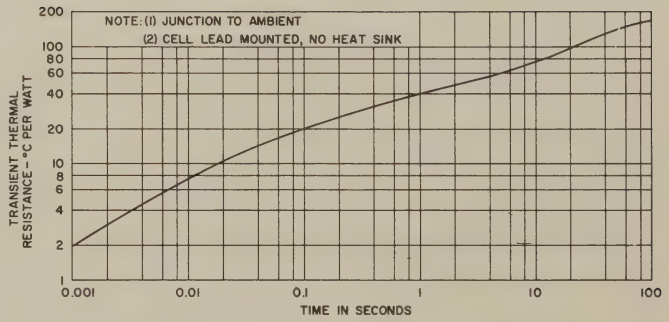
3. Firing Characteristics



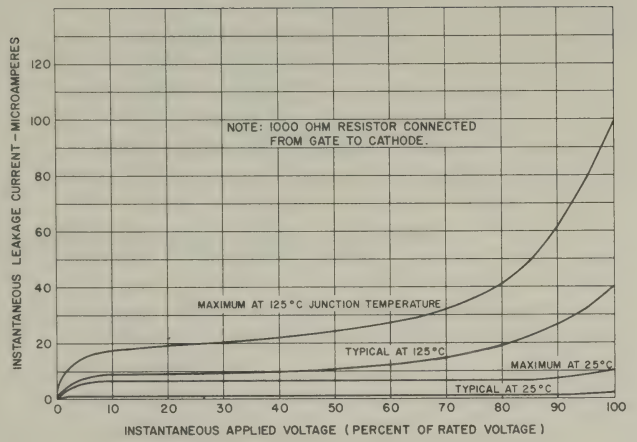
4. Maximum Allowable Case Temperature


NOTES : (1) RESISTIVE OR INDUCTIVE LOAD, 50 TO 400 CPS
(2) RATINGS DERIVED FOR 0.01 WATT AVERAGE GATE POWER
(3) RATE OF RISE OF FORWARD CURRENT MUST NOT EXCEED 100 MILLIAMPERES / MICROSECOND DURING THE FIRST FIVE MICROSECONDS AFTER APPLICATION OF GATE SIGNAL. IF HIGHER RATES OF RISE ARE TO BE USED, THE AMBIENT TEMPERATURE MUST BE REDUCED ACCORDING TO THE FOLLOWING EQUATION:
$\Delta T = 110 f V_m I_m \times 10^{-6}$
. WHERE ΔT = TEMP DERATING, °C
f = FREQUENCY, CPS
V_m = INSTANTANEOUS ANODE VOLTAGE (VOLTS) PRIOR TO SWITCHING
I_m = INSTANTANEOUS ANODE CURRENT (AMPERES) AFTER SWITCHING
MAXIMUM ALLOWABLE AMBIENT TEMPERATURE – °C
AVERAGE FORWARD CURRENT – AMPERES
0°
180°
CONDUCTION ANGLE
30°
60°
90°
120°
180°
DC

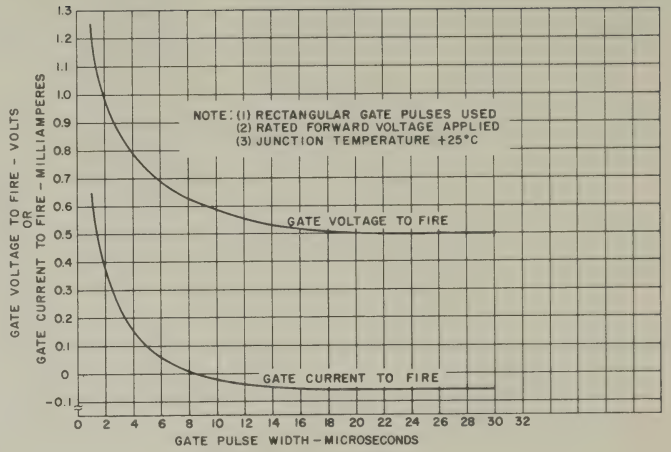
5. Maximum Allowable Ambient Temperature



6. Maximum Transient Thermal Resistance



7. Typical and Maximum Forward and Reverse Blocking Characteristics



8. Typical Gate Voltage and Current Variation with Gate Pulse Width

TYPE 2N1595-2N1599

Low Current
Silicon Controlled Rectifier
1.6 Amperes

Outline Drawing No. 1

Type	Minimum Forward Breakover Voltage (V_{BO})* $T_J = -65°C$ to $+125°C$	Repetitive Peak Reverse Voltage (PRV) $T_J = -65°C$ to $+150°C$
2N1595	50 volts	50 volts
2N1596	100 volts	100 volts
2N1597	200 volts	200 volts
2N1598	300 volts	300 volts
2N1599	400 volts	400 volts

*With 1000 ohms or less connected from gate to cathode.

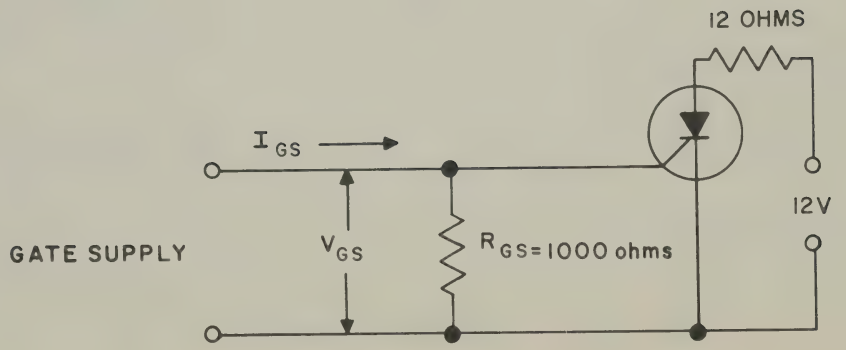
Maximum Allowable Ratings

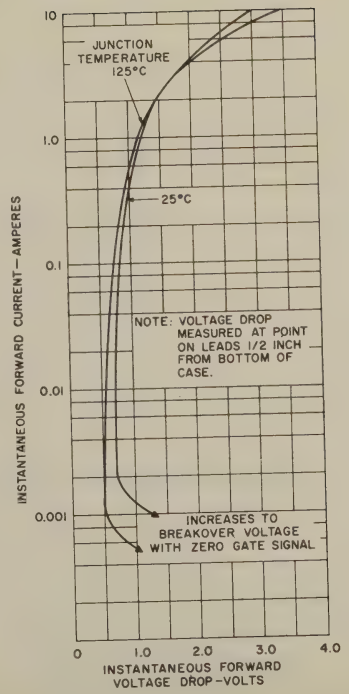
Repetitive Peak Forward Blocking Voltage (PFV)	500 volts
RMS Forward Current	1.6 amperes
Average Forward Current (I_F)	Depends on conduction angle (See Charts 3, 4, 5, and 6)
Peak One Cycle Surge Current (i_{surge})	15 amperes
Peak Gate Power (p_G)	0.1 watt
Average Gate Power (P_G)	0.01 watt
Peak Gate Current (i_G)	0.1 ampere
Peak Gate Voltage (v_G), Forward and Reverse	6 volts
Storage Temperature	$-65°C$ to $+150°C$
Operating Junction Temperature	$-65°C$ to $+150°C$ (See Charts 3, 4, 5, and 6)

Characteristics

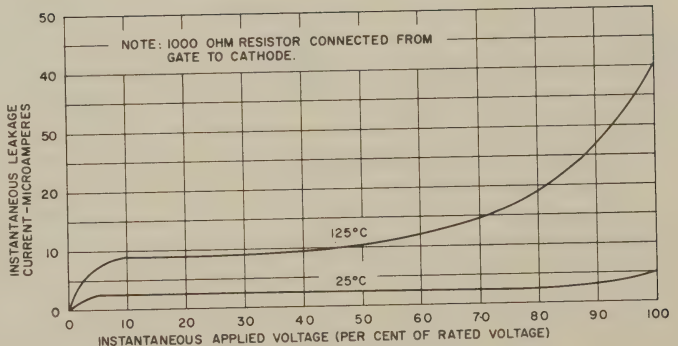
Typical Reverse (i_r) and Forward (i_s) Leakage Current	See Chart 2
Maximum Gate Current to Fire (I_{GS}) at $T_j = 25°C$*	10 mA_{dc}
Maximum Gate Voltage to Fire (V_{GF}) at $T_j = 25°C$	3 V_{dc}
Forward Voltage Drop	See Chart 1
Typical Holding Current (I_H) at $T_j = 25°C$	0.5 mA
Typical Turn-Off Time (t_o) at $T_j = 125°C$	20 μsec

*I_{GS} is defined as follows:

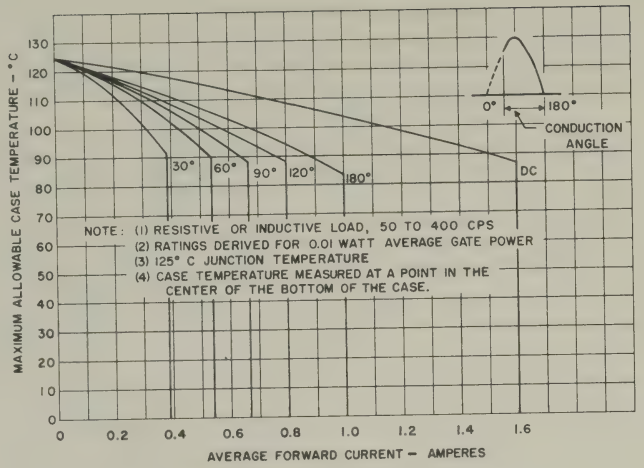




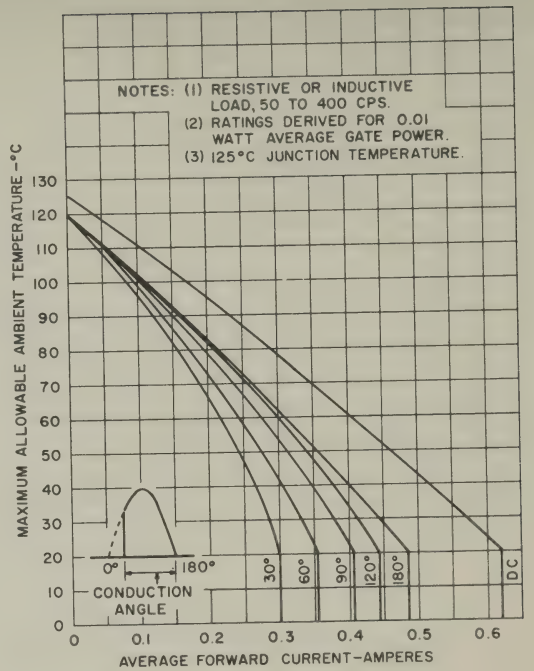
1. Typical Forward Characteristics Conducting State



2. Typical Forward and Reverse Blocking Characteristics



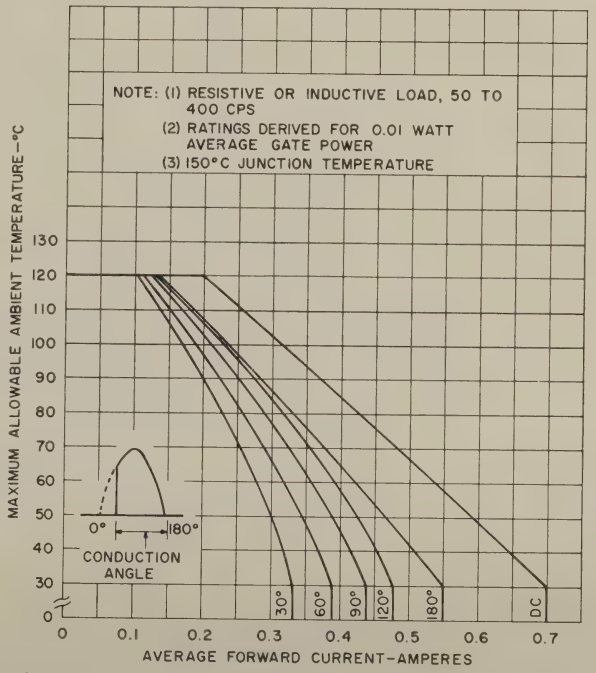
3. Maximum Allowable Case Temperature (125°C Junction Temp.)



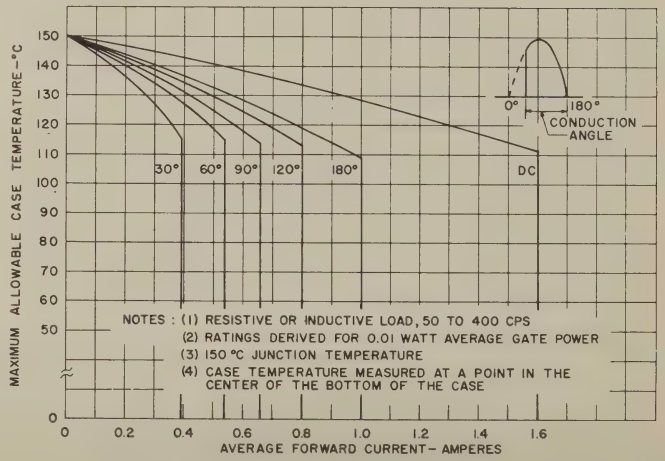
4. Maximum Allowable Ambient Temperature (125°C Junction Temp.)

2N1595 (Continued)

Charts 5 and 6 apply to latching applications where SCR need not block forward voltage after being turned on, since the V_{BO} specification does not apply above 125°C junction temperature. SCR will again block rated forward voltage after junction temperature drops below 125°C.



5. Maximum Allowable Ambient Temperature (150°C Junction Temp.)



6. Maximum Allowable Case Temperature (150°C Junction Temp.)

TYPE 2N1929-2N1935
(C8 Series)
Outline Drawing No. 2

Low Current
Silicon Controlled Rectifier
2.7 Amperes

The unique double-ended mechanical design of the 2N1929-1935 permits point-to-point wiring flexibility in circuit layout design. A prime feature of these devices is that high current loads are carried without the use of any external heat sink.

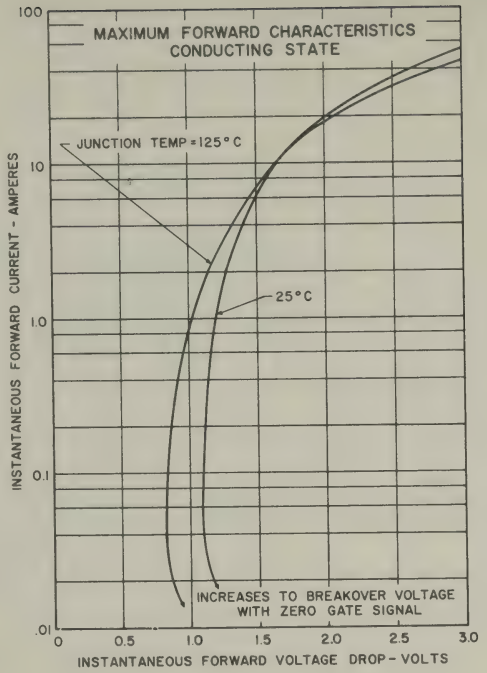
Maximum Allowable Ratings (Resistive or Inductive Load, 50-400 cps)

	2N1929 (C8U)	2N1930 (C8F)	2N1931 (C8A)	2N1932 (C8G)	2N1933 (C8B)	2N1934 (C8H)	2N1935 (C8C)
Transient Peak Reverse Voltage (Non-recurrent <5 millisec.)*	35	75	150	225	300	350	400 volts
Repetitive Peak Reverse Voltage (PRV)*	25	50	100	150	200	250	300 volts
Repetitive Peak Forward Blocking Voltage (PRV)	480 volts						
Average Forward Current (I_F)	Depends on Conduction Angle (See Chart 3)						
Peak One Cycle Non-recurrent Surge Current (I_{surge})	30 amperes (See Chart 8)						
Peak Gate Power (p_G)	5 watts						
Average Gate Power (P_G)	0.1 watt						
Peak Gate Current (i_G)	2.0 amperes						
Peak Gate Voltage (v_G) (Forward and Reverse)	10 volts						
Operating Junction Temperature	−65°C to +125°C						
Storage Temperature	−65°C to +150°C						

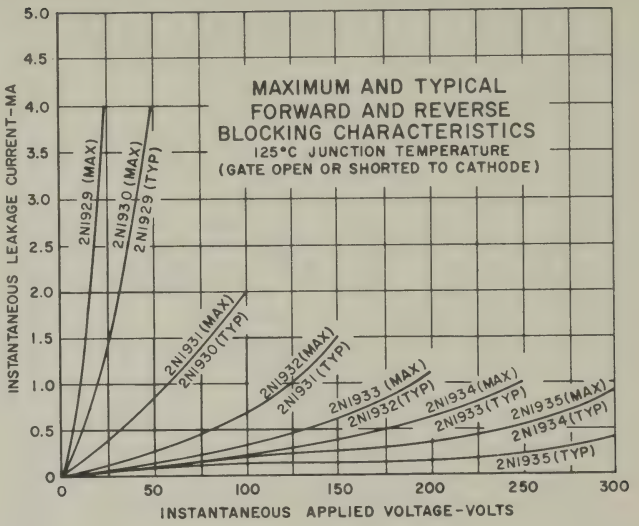
Characteristics at Maximum Ratings (125°C Junction Temperature)

	2N1929	2N1930	2N1931	2N1932	2N1933	2N1934	2N1935
Minimum Forward Break-over Voltage (VBO)	25	50	100	150	200	250	300 volts
Maximum Reverse (I_R) or Forward (I_S) Leakage Current (DC)	4.0	4.0	2.0	1.5	1.1	1.0	0.9 ma
Maximum Forward Voltage Drop (V_F)	1.1 volts (at 1.1 amps DC)						
Gate Firing Characteristic (See Chart 5)							
Maximum Thermal Resistance (R_T)	90°C/watt (Junction to Ambient)						
Maximum Holding Current (I_H)	20 ma at 25°C Junction Temp.						
Typical Holding Current (I_H)	8 ma at 25°C Junction Temp.						

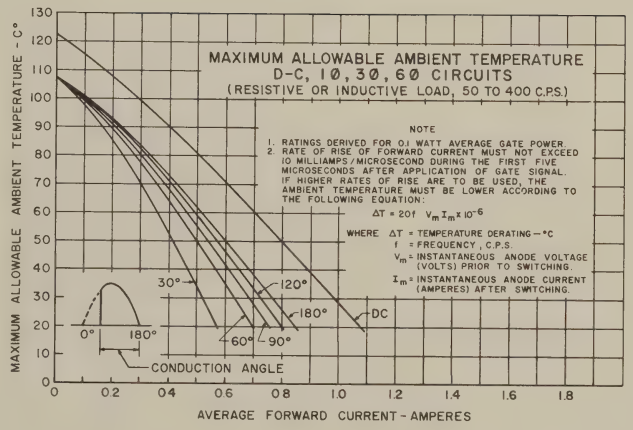
*PRV ratings apply for zero or negative gate voltage only.



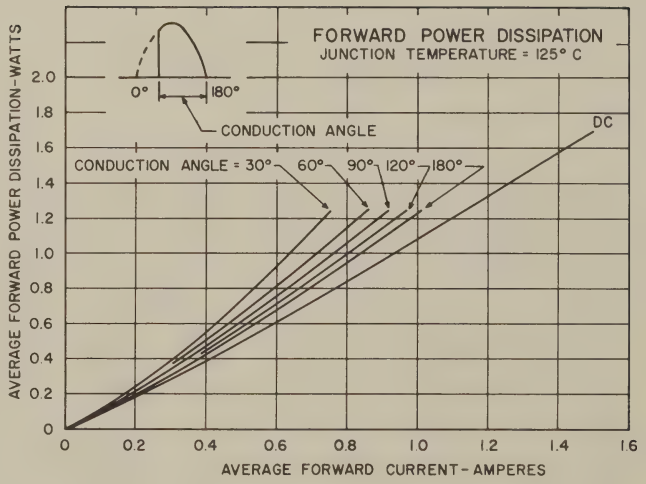
1. Maximum Forward Characteristics



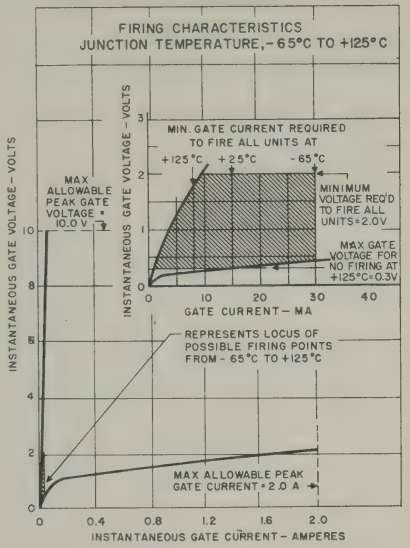
2. Maximum and Typical Reverse and Forward Blocking Characteristics


MAXIMUM ALLOWABLE AMBIENT TEMPERATURE
D-C, 10, 30, 60 CIRCUITS
(RESISTIVE OR INDUCTIVE LOAD, 50 TO 400 C.P.S.)
NOTE
1. RATINGS DERIVED FOR 0.1 WATT AVERAGE GATE POWER.
2. RATE OF RISE OF FORWARD CURRENT MUST NOT EXCEED 10 MILLIAMPS/MICROSECOND DURING THE FIRST FIVE MICROSECONDS AFTER APPLICATION OF GATE SIGNAL. IF HIGHER RATES OF RISE ARE TO BE USED, THE AMBIENT TEMPERATURE MUST BE LOWER ACCORDING TO THE FOLLOWING EQUATION:
$\Delta T = 20f\ V_m I_m \times 10^{-6}$
WHERE ΔT = TEMPERATURE DERATING — °C
f = FREQUENCY, C.P.S.
V_m = INSTANTANEOUS ANODE VOLTAGE (VOLTS) PRIOR TO SWITCHING.
I_m = INSTANTANEOUS ANODE CURRENT (AMPERES) AFTER SWITCHING.
30°
120°
180°
DC
60°
90°
0°
180°
CONDUCTION ANGLE
MAXIMUM ALLOWABLE AMBIENT TEMPERATURE - C°
AVERAGE FORWARD CURRENT - AMPERES

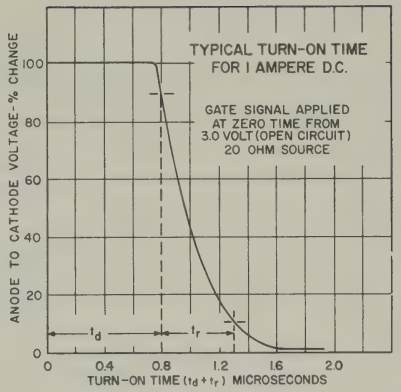
3. Maximum Forward Current vs. Ambient Temperature



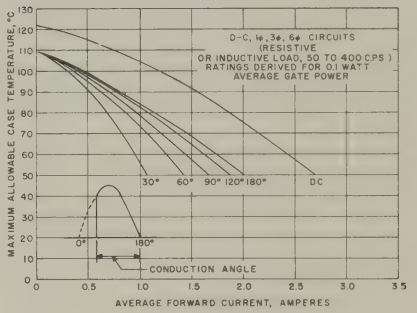
4. Forward Power Dissipation


FIRING CHARACTERISTICS
JUNCTION TEMPERATURE, -65°C TO +125°C
INSTANTANEOUS GATE VOLTAGE - VOLTS
INSTANTANEOUS GATE VOLTAGE - VOLTS
MIN. GATE CURRENT REQUIRED TO FIRE ALL UNITS AT
+125°C
+25°C
-65°C
MAX ALLOWABLE PEAK GATE VOLTAGE = 10.0 V
MINIMUM VOLTAGE REQ'D TO FIRE ALL UNITS=2.0V
MAX GATE VOLTAGE FOR NO FIRING AT +125°C=0.3V
GATE CURRENT - MA
REPRESENTS LOCUS OF POSSIBLE FIRING POINTS FROM - 65°C TO +125°C
MAX ALLOWABLE PEAK GATE CURRENT = 2.0 A
INSTANTANEOUS GATE CURRENT - AMPERES

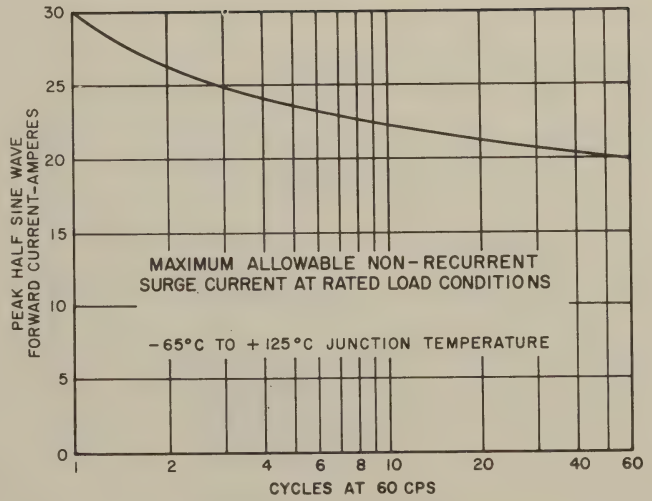
5. Firing Characteristics


TYPICAL TURN-ON TIME FOR 1 AMPERE D.C.
GATE SIGNAL APPLIED AT ZERO TIME FROM 3.0 VOLT (OPEN CIRCUIT) 20 OHM SOURCE
ANODE TO CATHODE VOLTAGE - % CHANGE
t_d
t_r
TURN-ON TIME ($t_d + t_r$) MICROSECONDS

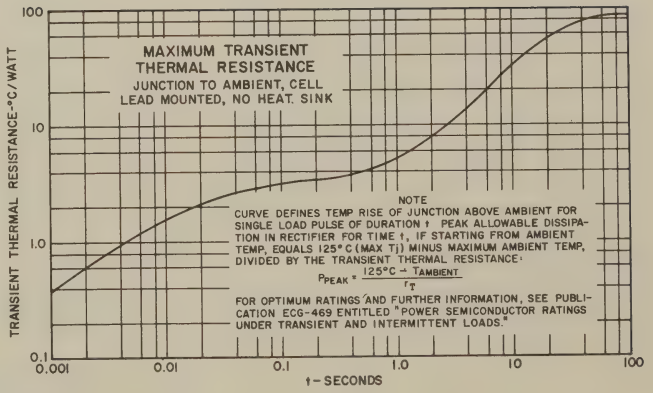
6. Typical Turn-On Time



7. Maximum Allowable Case Temperature



8. Maximum Allowable Non-Recurrent Surge Current at Rated Load Conditions


TRANSIENT THERMAL RESISTANCE-°C/WATT
100
10
1.0
0.1
MAXIMUM TRANSIENT
THERMAL RESISTANCE
JUNCTION TO AMBIENT, CELL
LEAD MOUNTED, NO HEAT SINK
NOTE
CURVE DEFINES TEMP RISE OF JUNCTION ABOVE AMBIENT FOR SINGLE LOAD PULSE OF DURATION t PEAK ALLOWABLE DISSIPATION IN RECTIFIER FOR TIME t, IF STARTING FROM AMBIENT TEMP, EQUALS 125°C (MAX Tj) MINUS MAXIMUM AMBIENT TEMP, DIVIDED BY THE TRANSIENT THERMAL RESISTANCE.
$P_{PEAK} = \frac{125°C - T_{AMBIENT}}{r_T}$
FOR OPTIMUM RATINGS AND FURTHER INFORMATION, SEE PUBLICATION ECG-469 ENTITLED "POWER SEMICONDUCTOR RATINGS UNDER TRANSIENT AND INTERMITTENT LOADS."
0.001
0.01
0.1
1.0
10
100
t-SECONDS

9. Maximum Transient Thermal Resistance

TYPE 2N1770-2N1777
(C11 Series)

Outline Drawing No. 3

Low Current
Silicon Controlled Rectifier
7 Amperes

The high current capability of the 2N1770-2N1777 results from the copper anode stud construction, allowing direct mounting to a heat sink.

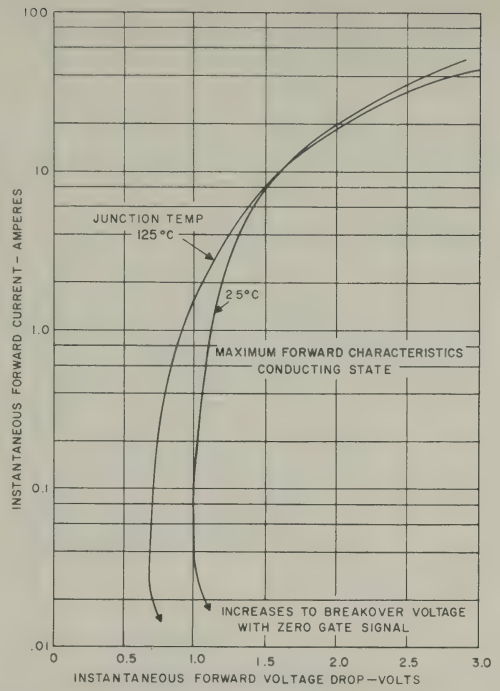
Maximum Allowable Ratings (Resistive or Inductive Load, 50-400 cps)

	2N1770 (C11U)	2N1771 (C11F)	2N1772 (C11A)	2N1773 (C11G)	2N1774 (C11B)	2N1775 (C11H)	2N1776 (C11C)	2N1777 (C11D)
Transient Peak Reverse Voltage (Non-recurrent, <5 millisecond)*	35	75	150	225	300	350	400	500 volts
Repetitive Peak Reverse Voltage (PRV) *	25	50	100	150	200	250	300	400 volts
Repetitive Peak Forward Blocking Voltage (PFV)	480 volts							
Average Forward Current (I_F)	Up to 4.7 amperes (See Chart 3)							
Peak One Cycle Non-Recurrent Surge Current (I_{surge})	60 amperes (See Chart 10)							
Peak Current During Turn-On Time Interval	125 amperes							
I^2t (for fusing)	Calculate from Chart 9							
Peak Gate Current (i_G)	2.0 amperes							
Peak Gate Voltage (v_G), Forward and Reverse	10 volts							
Peak Gate Power (p_G)	5 watts							
Average Gate Power (P_G)	0.5 watts							
Storage Temperature	−65°C to +150°C							
Operating Junction Temperature	−65°C to +125°C (See Charts 3 and 5)							
Stud Torque	15 inch-pounds							

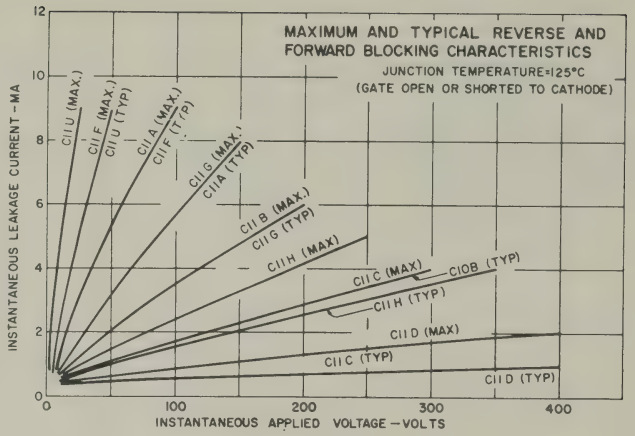
Characteristics at Maximum Ratings (125°C Junction Temperature)

	2N1770 (C11U)	2N1771 (C11F)	2N1772 (C11A)	2N1773 (C11G)	2N1774 (C11B)	2N1775 (C11H)	2N1776 (C11C)	2N1777 (C11D)
Minimum Forward Break-over Voltage (V_{BO})	25	50	100	150	200	250	300	400 volts
Maximum Reverse (I_R) or Forward (I_S) Leakage Current (Full Cycle Average)*	4.5	4.5	4.5	4.0	3.0	2.5	2.0	1.0 ma
Maximum Forward Voltage ($V_{F\ AVG.}$)	0.80 volt (4.7 amp avg., 180° conduction angle)							
Gate Firing Characteristics (See Chart 6)								
Maximum Thermal Resistance (R_T)	3.1°C/watt (Junction to stud)							
Typical Holding Current (I_H)	4.0 ma							

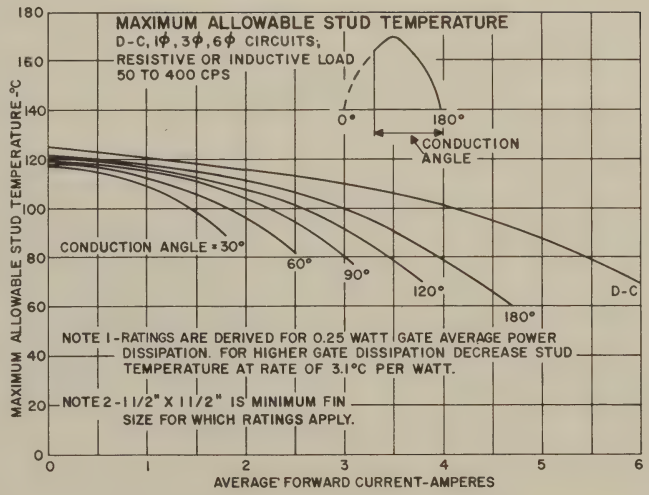
*PRV ratings apply for zero or negative gate voltage only. Maximum stud to ambient thermal resistance for which maximum PRV ratings apply equals 18°C/watt.



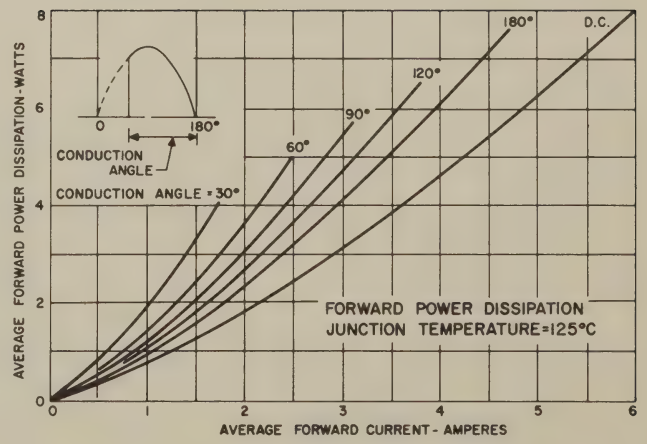
1. Maximum Forward Characteristics Conducting State



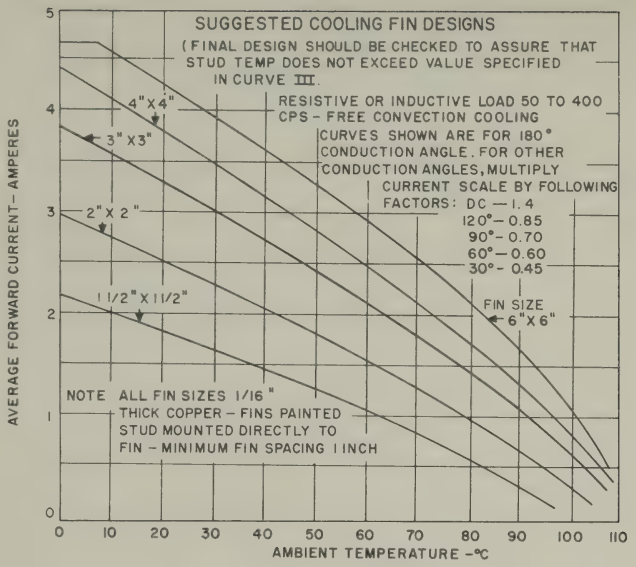
2. Maximum and Typical Reverse and Forward Blocking Characteristics


MAXIMUM ALLOWABLE STUD TEMPERATURE
D-C, 1Φ, 3Φ, 6Φ CIRCUITS;
RESISTIVE OR INDUCTIVE LOAD
50 TO 400 CPS
0°
180°
CONDUCTION ANGLE
CONDUCTION ANGLE = 30°
60°
90°
120°
180°
D-C
NOTE 1 - RATINGS ARE DERIVED FOR 0.25 WATT GATE AVERAGE POWER DISSIPATION. FOR HIGHER GATE DISSIPATION DECREASE STUD TEMPERATURE AT RATE OF 3.1°C PER WATT.
NOTE 2 - 1 1/2" X 1 1/2" IS MINIMUM FIN SIZE FOR WHICH RATINGS APPLY.
MAXIMUM ALLOWABLE STUD TEMPERATURE - °C
AVERAGE FORWARD CURRENT - AMPERES

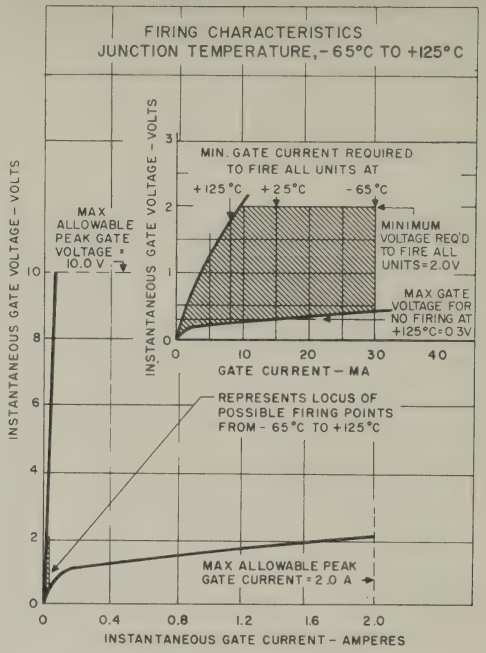
3. Maximum Allowable Stud Temperature



4. Forward Power Dissipation

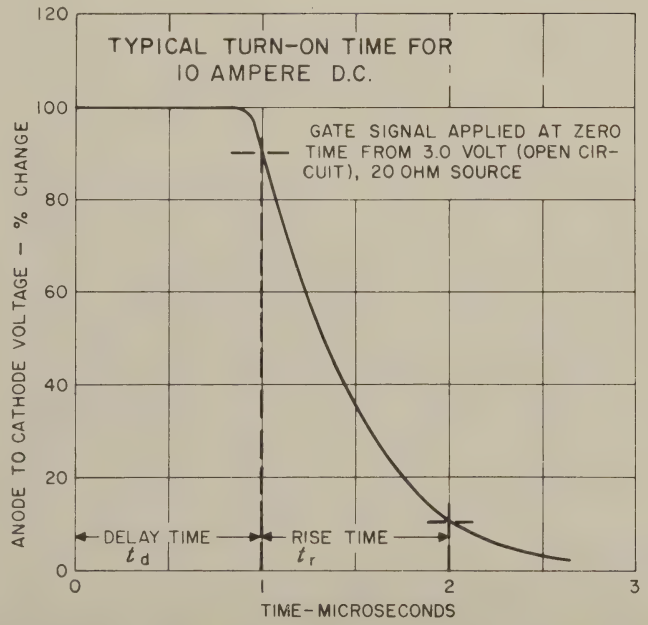


5. Suggested Cooling Fin Designs

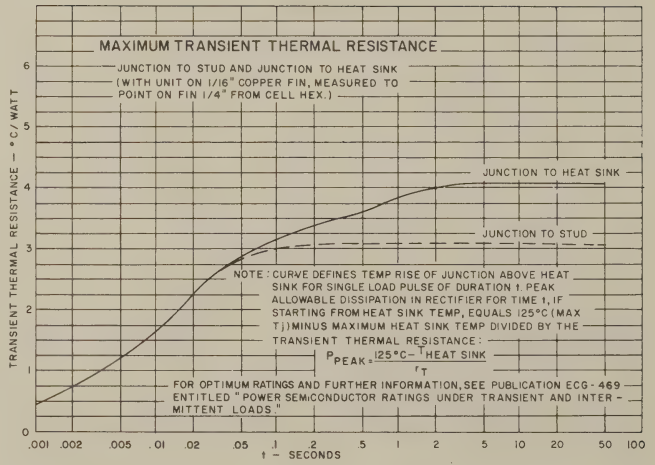


6. Firing Characteristics

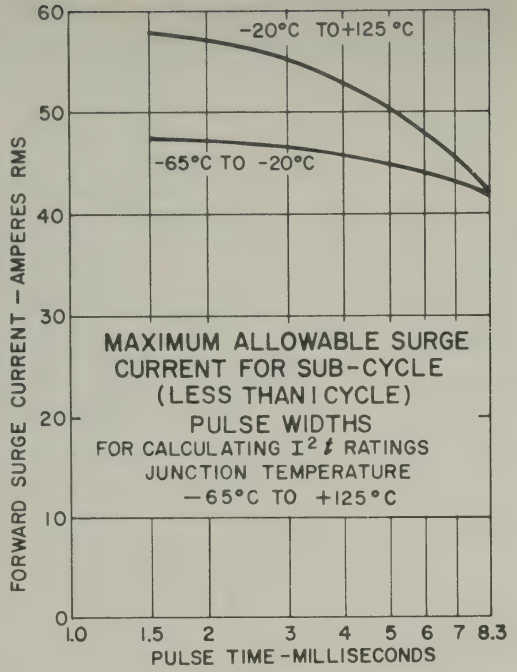
2N1770 (Continued)



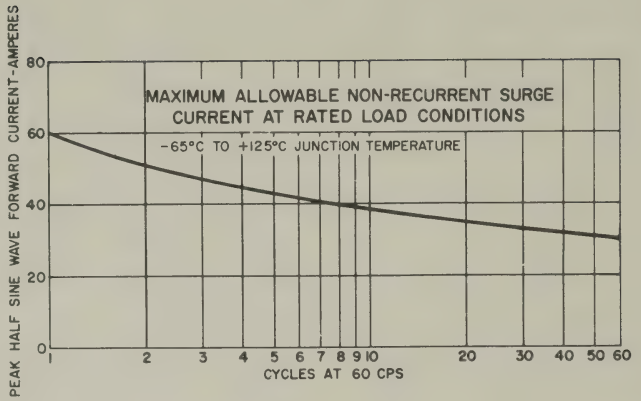
7. Typical Turn-On Time


MAXIMUM TRANSIENT THERMAL RESISTANCE
JUNCTION TO STUD AND JUNCTION TO HEAT SINK (WITH UNIT ON 1/16" COPPER FIN, MEASURED TO POINT ON FIN 1/4" FROM CELL HEX.)
TRANSIENT THERMAL RESISTANCE – °C/WATT
JUNCTION TO HEAT SINK
JUNCTION TO STUD
NOTE: CURVE DEFINES TEMP RISE OF JUNCTION ABOVE HEAT SINK FOR SINGLE LOAD PULSE OF DURATION t. PEAK ALLOWABLE DISSIPATION IN RECTIFIER FOR TIME t, IF STARTING FROM HEAT SINK TEMP, EQUALS 125°C (MAX TJ) MINUS MAXIMUM HEAT SINK TEMP DIVIDED BY THE TRANSIENT THERMAL RESISTANCE:
$P_{PEAK} = \frac{125°C - T_{HEAT\ SINK}}{r_T}$
FOR OPTIMUM RATINGS AND FURTHER INFORMATION, SEE PUBLICATION ECG-469 ENTITLED "POWER SEMICONDUCTOR RATINGS UNDER TRANSIENT AND INTERMITTENT LOADS."
0
1
2
3
4
5
6
.001
.002
.005
.01
.02
.05
.1
.2
.5
1
2
5
10
20
50
100
t – SECONDS

8. Transient Thermal Resistance



9. Sub-Cycle Surge Rating



10. Surge Rating, 1 to 60 CPS

TYPE 2N1770A-2N1777A (C10 Series)

Outline Drawing No. 3

Low Current Silicon Controlled Rectifier 7 Amperes (High Temperature Type)

Maximum Allowable Ratings (Resistive or Inductive Load, 50-400 cps)

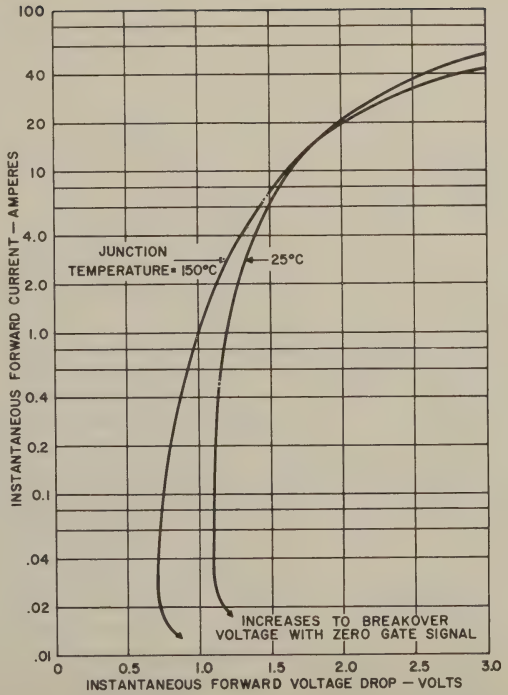
	2N1770A (C10U)	2N1771A (C10F)	2N1772A (C10A)	2N1773A (C10G)	2N1774A (C10B)	2N1775A (C10H)	2N1776A (C10C)	2N1777A (C10D)
Transient Peak Reverse Voltage (Non-recurrent, <5 millisec.)*	35	75	150	225	300	350	400	500 volts
Repetitive Peak Reverse Voltage (PRV)*	25	50	100	150	200	250	300	400 volts
RMS Voltage (V_{RMS}), Sinusoidal	17.5	35	70	105	140	175	210	280 volts
Repetitive Peak Forward Blocking Voltage (PFV)	480 volts							
Average Forward Current (I_F)	(See Chart 3)							
Peak One Cycle Non-Recurrent Surge Current (I_{surge})	60 amperes (See Chart 8)							
Peak Current During Turn-On Time Interval	125 amperes							
I^2t (for fusing)	Calculate from Chart 9							
Peak Gate Current (i_G)	2.0 amperes							
Peak Gate Voltage (v_G), Forward and Reverse	10 volts							
Peak Gate Power (p_G)	5 watts							
Average Gate Power (P_G)	0.5 watts							
Storage Temperature	−65°C to +150°C							
Operating Junction Temperature	−65°C to +150°C (See Charts 3 and 5)							
Stud Torque	15 inch-pounds							

Characteristics at Maximum Ratings (150°C Junction Temperature)

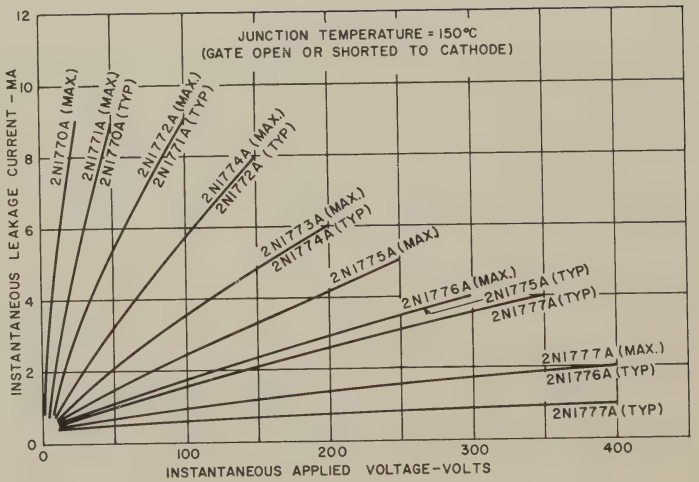
	2N1770A (C10U)	2N1771A (C10F)	2N1772A (C10A)	2N1773A (C10G)	2N1774A (C10B)	2N1775A (C10H)	2N1776A (C10C)	2N1777A (C10D)
Minimum Forward Break-over Voltage (V_{BO})	25	50	100	150	200	250	300	400 volts
Maximum Reverse (I_R) or Forward (I_S) Leakage Current (Full Cycle Average)*	4.5	4.5	4.5	4.0	3.0	2.5	2.0	1.0 ma
Maximum Forward Voltage ($V_{F\ AVG.}$)	0.75 volts (4.7 amp avg., 180° conduction angle)							
Gate Firing Characteristic	(See Chart 6)							
Maximum Thermal Resistance (R_T)	3.1°C/watt (Junction to stud)							
Typical Holding Current (I_H)	8.0 ma @ 25°C Junction Temperature							

*PRV ratings apply for zero or negative gate voltage only.

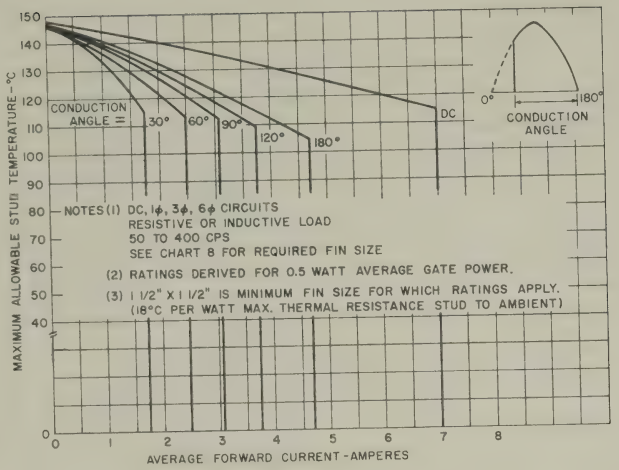
2N1770A (Continued)



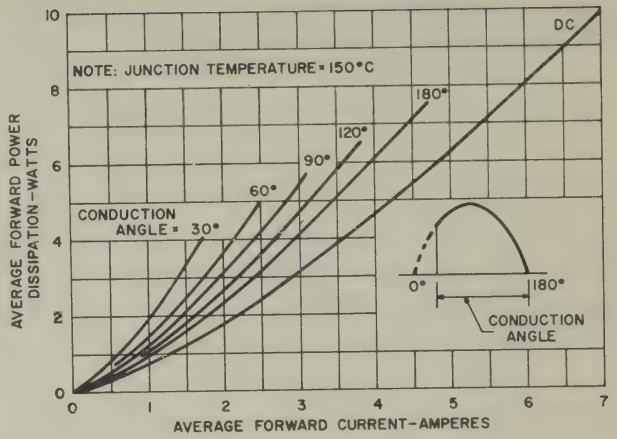
1. Maximum Forward Characteristics Conducting State



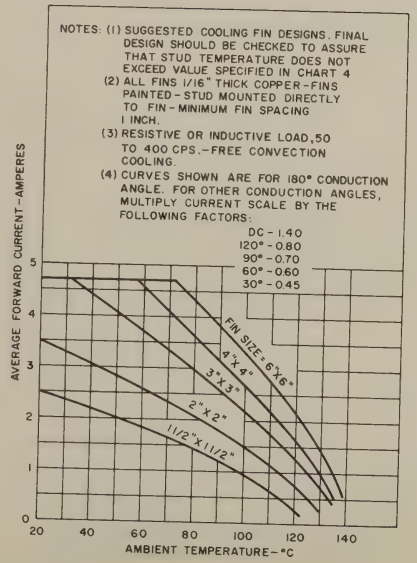
2. Maximum and Typical Reverse and Forward Blocking Characteristics


MAXIMUM ALLOWABLE STUD TEMPERATURE - °C
AVERAGE FORWARD CURRENT - AMPERES
CONDUCTION ANGLE =
30°
60°
90°
120°
180°
DC
0°
180°
CONDUCTION ANGLE
NOTES (1) DC, 1ϕ, 3ϕ, 6ϕ CIRCUITS
RESISTIVE OR INDUCTIVE LOAD
50 TO 400 CPS
SEE CHART 8 FOR REQUIRED FIN SIZE
(2) RATINGS DERIVED FOR 0.5 WATT AVERAGE GATE POWER.
(3) 1 1/2" X 1 1/2" IS MINIMUM FIN SIZE FOR WHICH RATINGS APPLY.
(18°C PER WATT MAX. THERMAL RESISTANCE STUD TO AMBIENT)

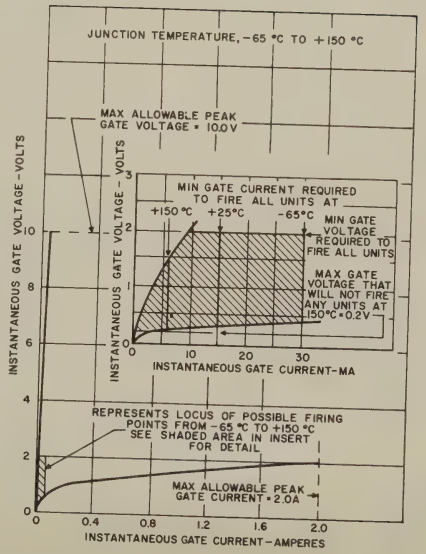
3. Maximum Allowable Stud Temperature for Sinusoidal Current Waveform



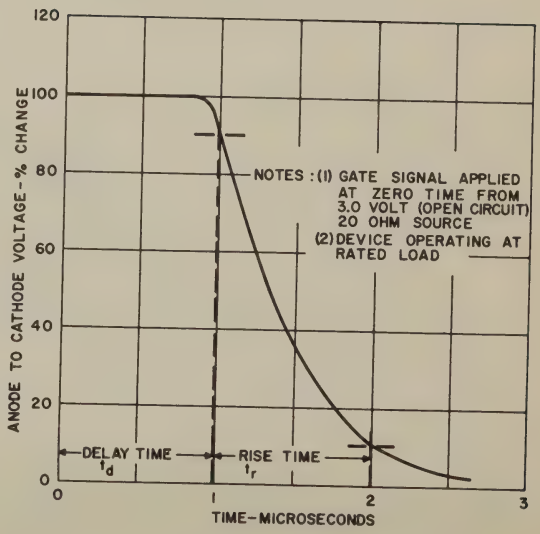
4. Forward Power Dissipation for Sinusoidal Current Waveform


NOTES: (1) SUGGESTED COOLING FIN DESIGNS. FINAL DESIGN SHOULD BE CHECKED TO ASSURE THAT STUD TEMPERATURE DOES NOT EXCEED VALUE SPECIFIED IN CHART 4
(2) ALL FINS 1/16" THICK COPPER-FINS PAINTED-STUD MOUNTED DIRECTLY TO FIN-MINIMUM FIN SPACING 1 INCH.
(3) RESISTIVE OR INDUCTIVE LOAD, 50 TO 400 CPS.-FREE CONVECTION COOLING.
(4) CURVES SHOWN ARE FOR 180° CONDUCTION ANGLE. FOR OTHER CONDUCTION ANGLES, MULTIPLY CURRENT SCALE BY THE FOLLOWING FACTORS:
DC - 1.40
120° - 0.80
90° - 0.70
60° - 0.60
30° - 0.45
AVERAGE FORWARD CURRENT - AMPERES
FIN SIZE - 6"X6"
4"X4"
3"X3"
2"X2"
1 1/2"X1 1/2"
AMBIENT TEMPERATURE - °C

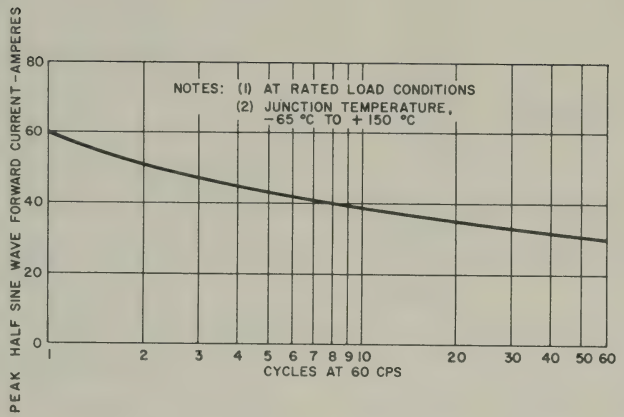
5. Maximum Forward Current vs. Ambient Temperature for Various Fin Sizes


JUNCTION TEMPERATURE, -65 °C TO +150 °C
MAX ALLOWABLE PEAK GATE VOLTAGE = 10.0V
MIN GATE CURRENT REQUIRED TO FIRE ALL UNITS AT
+150 °C +25°C -65°C
MIN GATE VOLTAGE REQUIRED TO FIRE ALL UNITS
MAX GATE VOLTAGE THAT WILL NOT FIRE ANY UNITS AT 150°C = 0.2V
INSTANTANEOUS GATE VOLTAGE - VOLTS
INSTANTANEOUS GATE CURRENT - MA
REPRESENTS LOCUS OF POSSIBLE FIRING POINTS FROM -65 °C TO +150 °C SEE SHADED AREA IN INSERT FOR DETAIL
MAX ALLOWABLE PEAK GATE CURRENT = 2.0A
INSTANTANEOUS GATE CURRENT - AMPERES

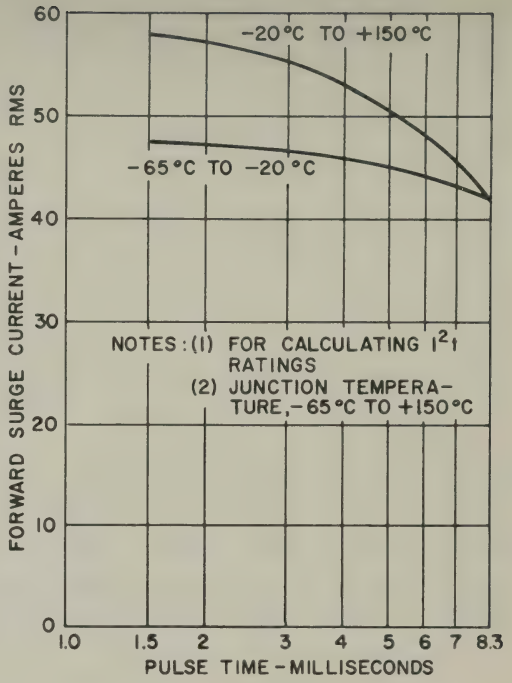
6. Firing Characteristics


NOTES: (1) GATE SIGNAL APPLIED AT ZERO TIME FROM 3.0 VOLT (OPEN CIRCUIT) 20 OHM SOURCE
(2) DEVICE OPERATING AT RATED LOAD
ANODE TO CATHODE VOLTAGE - % CHANGE
DELAY TIME
RISE TIME
TIME - MICROSECONDS

7. Typical Turn-On Time



8. Maximum Allowable Non-Recurrent Surge Current Rating



9. Maximum Allowable Non-Recurrent Sub-Cycle Surge Current Rating

TYPE 2N1842-2N1850
(C36 Series)
Outline Drawing No. 4

Medium Current
Silicon Controlled Rectifier
16 Amperes

Maximum Allowable Ratings (Resistive or Inductive Load, 50 to 400 CPS)

	2N1842 (C36U)	2N1843 (C36F)	2N1844 (C36A)	2N1845 (C36G)	2N1846 (C36B)	2N1847 (C36H)	2N1848 (C36C)	2N1849 (C36D)	2N1850 (C36E)
Transient Peak Reverse Voltage (Non-recurrent <5 millisec.)*	35	75	150	225	300	350	400	500	600 volts
Repetitive Peak Reverse Voltage (PRV)*	25	50	100	150	200	250	300	400	500 volts

Repetitive Peak Forward Blocking Voltage (PFV)	600 volts
RMS Forward Current	16 amperes (For all conduction angles)
Average Forward Current (I_F)	Depends on conduction angle (See Charts 3 and 5)
Peak One Cycle Surge Current (I_{surge})	125 amperes (See Chart 8)
Peak Current During Turn-on Time Interval	(See Note)
I^2t (for fusing)	40 ampere^2 seconds (time $\leqq$ .008 seconds)
Peak Gate Power (P_G)	5 watts
Average Gate Power (P_G)	0.5 watt
Peak Gate Current (I_G)	2 amperes
Peak Gate Voltage (V_G) (forward)	10 volts
Peak Gate Voltage (V_G) (reverse)	5 volts
Storage Temperature	−40°C to +125°C
Operating Junction Temperature	−40°C to +100°C (See Charts 3 and 5)
Stud Torque	30 inch-pounds

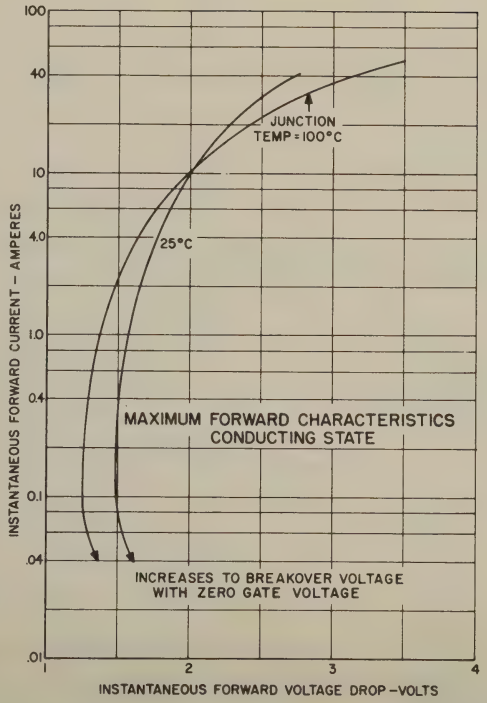
Characteristics at Maximum Ratings (100° Junction Temperature)

	2N1842 (C36U)	2N1843 (C36F)	2N1844 (C36A)	2N1845 (C36G)	2N1846 (C36B)	2N1847 (C36H)	2N1848 (C36C)	2N1849 (C36D)	2N1850 (C36E)
Minimum Forward Breakover Voltage (V_{BO})	25	50	100	150	200	250	300	400	500 volts
Minimum Time Constant for Application of Forward Blocking Voltage (Also See Chart 10)	2.6	3.0	3.9	4.8	5.7	6.6	7.5	9.2	11.0 microsec.
Maximum Reverse (I_R) or Forward (I_S) Leakage Current (Full Cycle Average)*	22.5	19.0	12.5	6.5	6.0	5.5	5.0	4.0	3.0 ma
Maximum Forward Voltage Drop ($V_{F\ AVG.}$)	1.25 volts (Full Cycle Average)								
Gate Firing Characteristic	(See Chart 6)								
Maximum Thermal Resistance (R_T)	2.5°C/watt (Junction to Stud)								
Typical Holding Current (I_H)	20 ma								

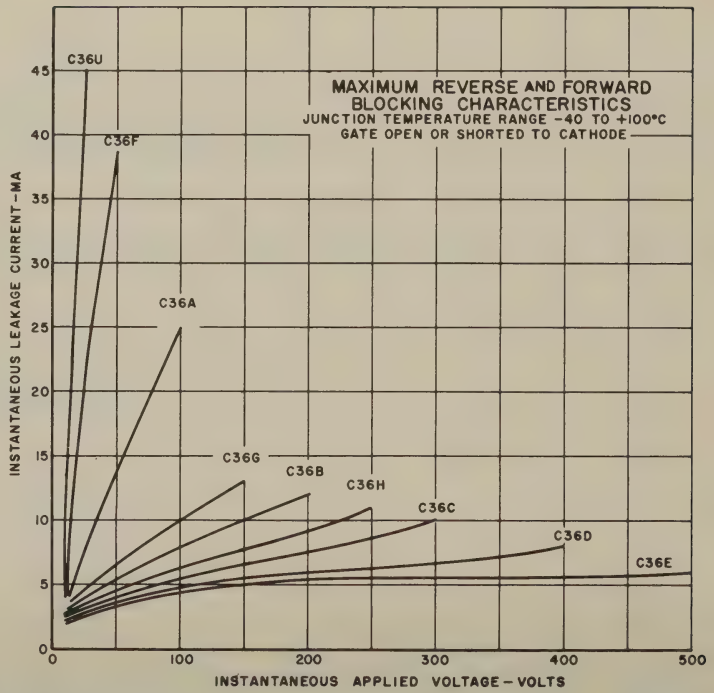
*PRV ratings apply for zero or negative gate voltage. For positive gate voltage applied simultaneously with PRV, see Application Notes. Maximum heat sink thermal resistance for which maximum PRV ratings apply equals 11.0°C per watt.

NOTE: Peak recurrent current during turn-on interual must be limited to values below.

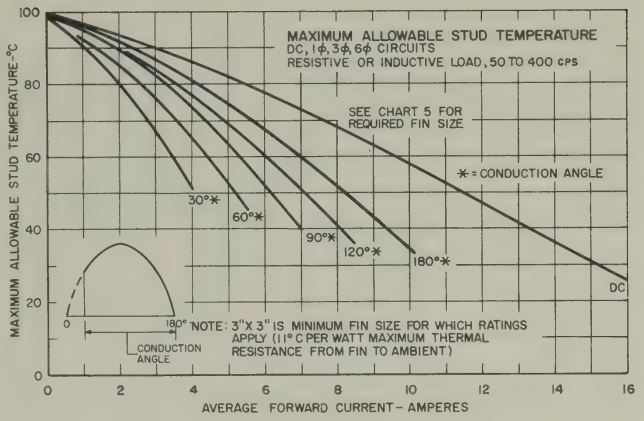
Max Voltages to be Switched	Allow Recurrent Peak Current (Rise Time 5.0 Microseconds)
100V	300A
200V	140A
300V	75A
400V	65A
500V	60A



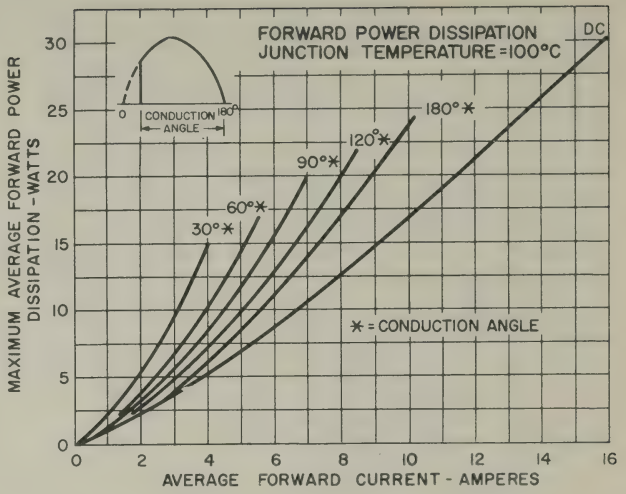
1. Maximum Forward Characteristics Conducting State



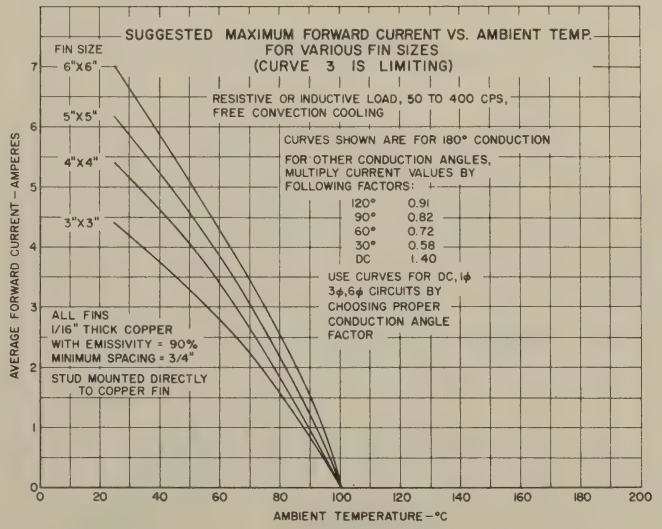
2. Maximum Reverse and Forward Blocking Characteristics



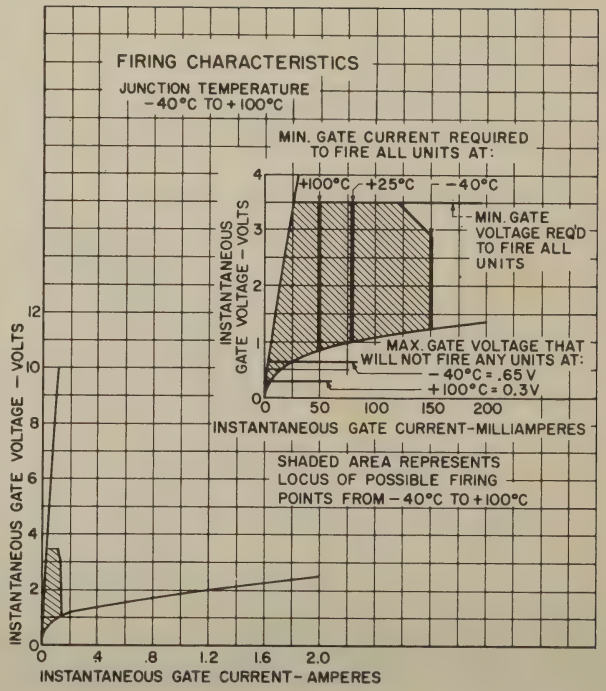
3. Maximum Allowable Stud Temperature



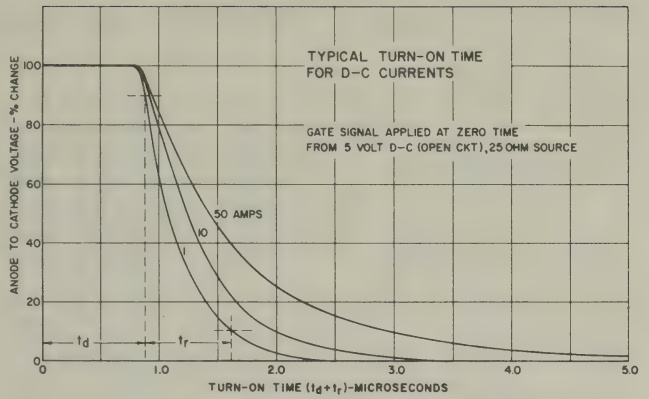
4. Forward Power Dissipation



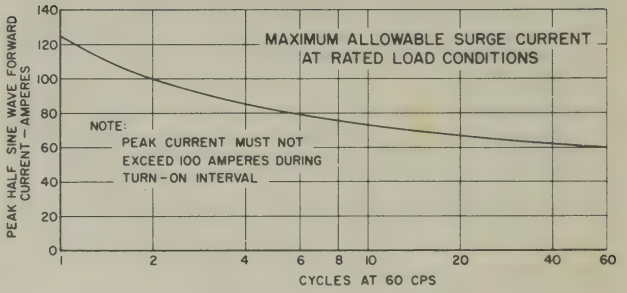
5. Maximum Forward Current vs. Ambient Temperature for Various Fin Sizes



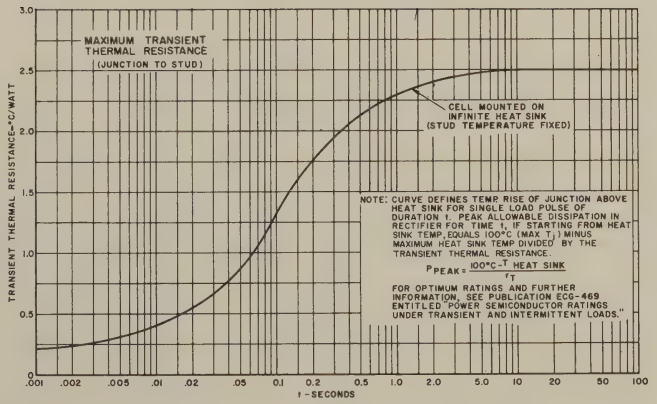
6. Firing Characteristics



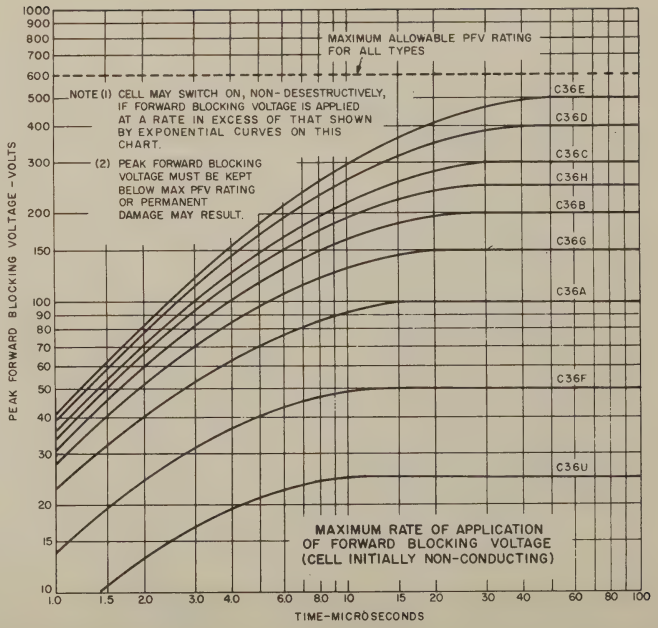
7. Typical Turn-On Time



8. Maximum Allowable Surge Current at Rated Load Conditions



9. Maximum Transient Thermal Resistance



10. Maximum Rate of Application of Forward Blocking Voltage

TYPE 2N681-2N689
(USN Specification 2N681-2N688 MIL-S-19500-108 Available) (C35 Series)
Outline Drawing No. 4

Medium Current
Silicon Controlled Rectifier
25 Amperes

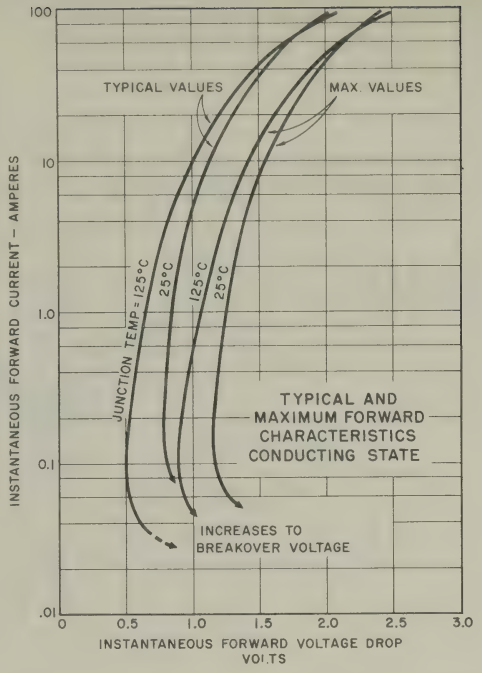
Maximum Allowable Ratings (Resistive or Inductive Load, 50 to 400 CPS)

	2N681 (C35U)	2N682 (C35F)	2N683 (C35A)	2N684 (C35G)	2N685 (C35B)	2N686 (C35H)	2N687 (C35C)	2N688 (C35D)	2N689 (C35E)	
Transient Peak Reverse Voltage (Non-Recurrent <5 millisec.)*	35	75	150	225	300	350	400	500	600	volts
Repetitive Peak Reverse Voltage (PRV)*	25	50	100	150	200	250	300	400	500	volts
Repetitive Peak Forward Blocking Voltage (PFV)	600 volts									
RMS Forward Current	25 amperes (For all conduction angles)									
Average Forward Current (I_F)	Depends on conduction angle (See Charts 4 and 6)									
Peak One Cycle Surge Current (I_{surge})	150 amperes (See Chart 9)									
Peak Current During Turn-on Time Interval	(See Chart 9)									
I^2t (for fusing)	75 ampere^2 seconds (time $\leqq$ .008 seconds)									
Peak Gate Power (p_G)	5 watts									
Average Gate Power (P_G)	0.5 watt									
Peak Gate Current (i_G)	2 amperes									
Peak Gate Voltage (v_G) (forward)	10 volts									
Peak Gate Voltage (v_G) (inverse)	5 volts									
Storage Temperature	−65°C to +150°C									
Operating Junction Temperature	−65°C to +125°C (See Charts 4 and 6)									
Stud Torque	30 inch-pounds									

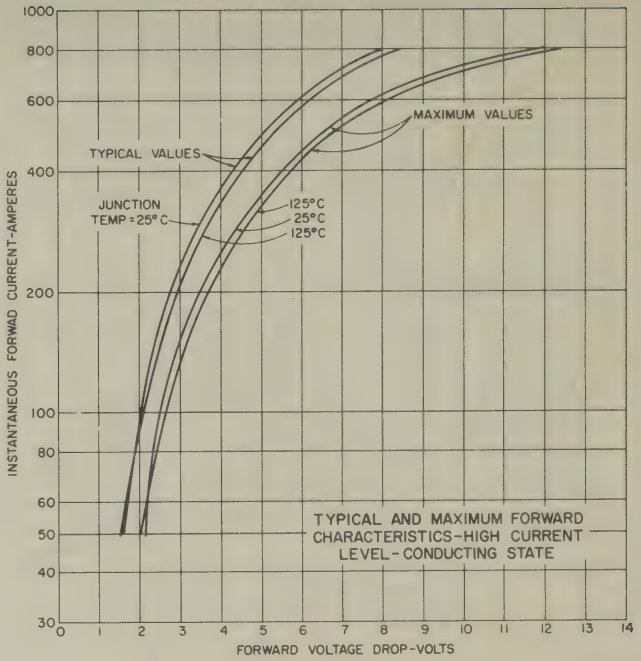
Characteristics at Maximum Ratings (+125°C Junction Temperature)

	2N681 (C35U)	2N682 (C35F)	2N683 (C35A)	2N684 (C35G)	2N685 (C35B)	2N686 (C35H)	2N687 (C35C)	2N688 (C35D)	2N689 (C35E)	
Minimum Forward Breakover Voltage (V_{BO})	25	50	100	150	200	250	300	400	500	volts
Minimum Time Constant for Application of Forward Blocking Voltage (Also see Chart 11)	2.6	3.0	3.9	4.8	5.7	6.6	7.5	9.2	11.0	microsec.
Maximum Reverse (I_R) or Forward (I_S) Leakage Current (Full Cycle Average)*	6.5	6.5	6.5	6.5	6.0	5.5	5.0	4.0	3.0	ma
Maximum Forward Voltage ($V_{F\ AVG.}$)	0.86 volts (16 amperes avg., 180° conduction angle)									
Gate Firing Characteristic	(See Chart 7)									
Maximum Thermal Resistance (R_T)	2°C/watt (Junction to Stud)									
Typical Holding Current (I_H)	10 ma									

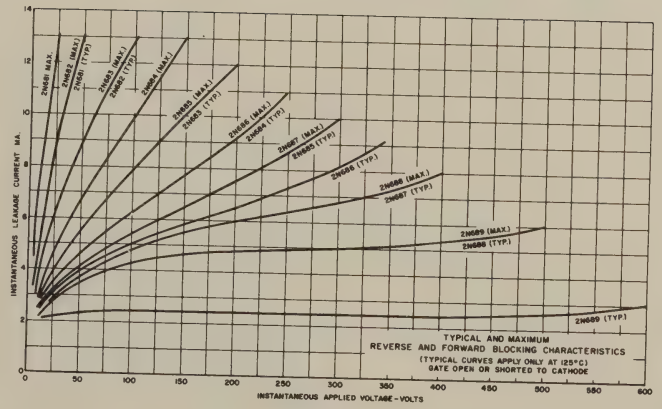
*PRV ratings apply for zero or negative gate voltage. For positive gate voltage applied simultaneously with PRV, see Application Notes. Maximum heat sink thermal resistance for which maximum PRV ratings apply equals 11.0°C per watt.



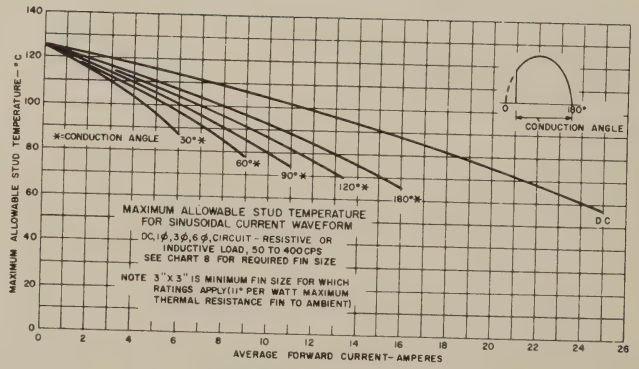
1. Typical and Maximum Forward Characteristics-Conducting State



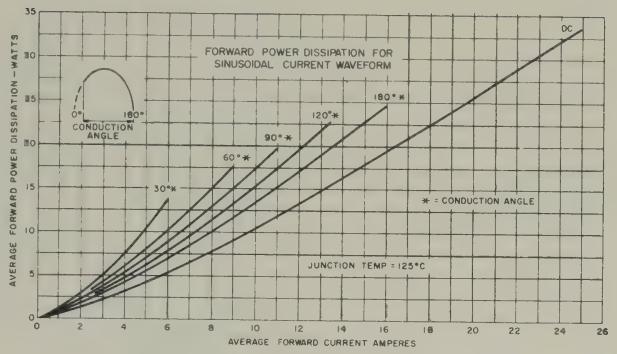
2. Typical and Maximum Forward Characteristics—High Current Level-Conducting State



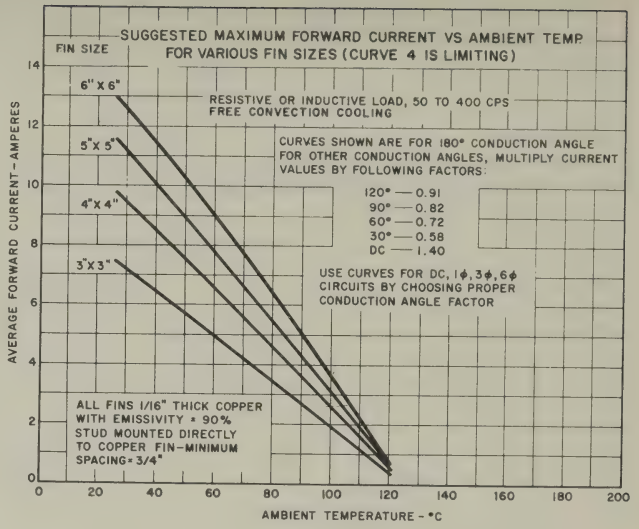
3. Typical and Maximum Reverse and Forward Blocking Characteristics



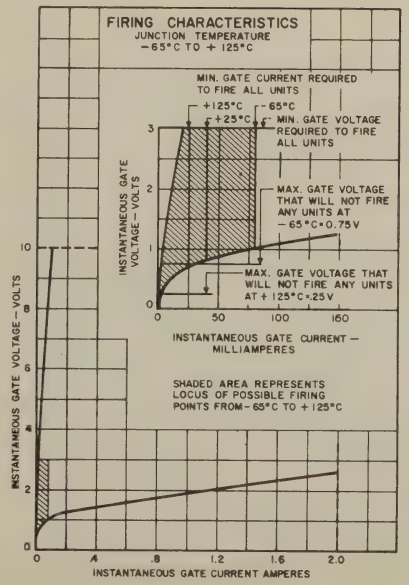
4. Maximum Allowable Stud Temperature for Sinusoidal Current Waveform



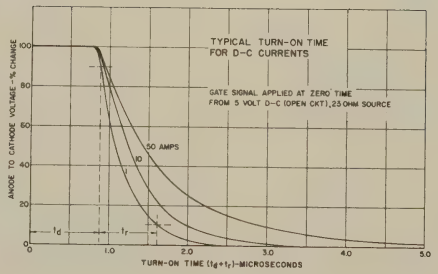
5. Forward Power Dissipation for Sinusoidal Current Waveform


SUGGESTED MAXIMUM FORWARD CURRENT VS AMBIENT TEMP FOR VARIOUS FIN SIZES (CURVE 4 IS LIMITING)
FIN SIZE
6" X 6"
5" X 5"
4" X 4"
3" X 3"
RESISTIVE OR INDUCTIVE LOAD, 50 TO 400 CPS FREE CONVECTION COOLING
CURVES SHOWN ARE FOR 180° CONDUCTION ANGLE FOR OTHER CONDUCTION ANGLES, MULTIPLY CURRENT VALUES BY FOLLOWING FACTORS:
120° — 0.91
90° — 0.82
60° — 0.72
30° — 0.58
DC — 1.40
USE CURVES FOR DC, 1φ, 3φ, 6φ CIRCUITS BY CHOOSING PROPER CONDUCTION ANGLE FACTOR
ALL FINS 1/16" THICK COPPER WITH EMISSIVITY = 90% STUD MOUNTED DIRECTLY TO COPPER FIN—MINIMUM SPACING = 3/4"
AVERAGE FORWARD CURRENT - AMPERES
AMBIENT TEMPERATURE - °C

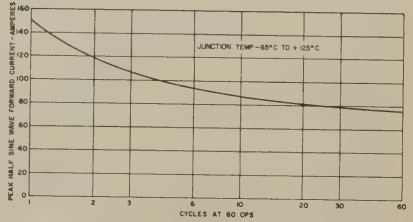
6. Maximum Forward Current vs. Ambient Temperature for Various Fin Sizes


FIRING CHARACTERISTICS
JUNCTION TEMPERATURE
−65°C TO + 125°C
MIN. GATE CURRENT REQUIRED TO FIRE ALL UNITS
+125°C
+25°C
−65°C
MIN. GATE VOLTAGE REQUIRED TO FIRE ALL UNITS
MAX. GATE VOLTAGE THAT WILL NOT FIRE ANY UNITS AT −65°C+0.75V
MAX. GATE VOLTAGE THAT WILL NOT FIRE ANY UNITS AT + 125°C+.25V
INSTANTANEOUS GATE VOLTAGE – VOLTS
INSTANTANEOUS GATE CURRENT – MILLIAMPERES
SHADED AREA REPRESENTS LOCUS OF POSSIBLE FIRING POINTS FROM −65°C TO + 125°C
INSTANTANEOUS GATE VOLTAGE – VOLTS
INSTANTANEOUS GATE CURRENT AMPERES

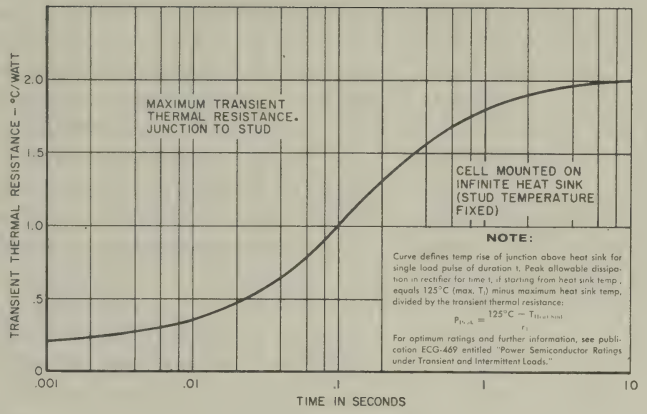
7. Firing Characteristics


TYPICAL TURN-ON TIME FOR D-C CURRENTS
GATE SIGNAL APPLIED AT ZERO TIME FROM 5 VOLT D-C (OPEN CKT), 2.5 OHM SOURCE
50 AMPS
10
ANODE TO CATHODE VOLTAGE – % CHANGE
TURN-ON TIME (td+tr)–MICROSECONDS

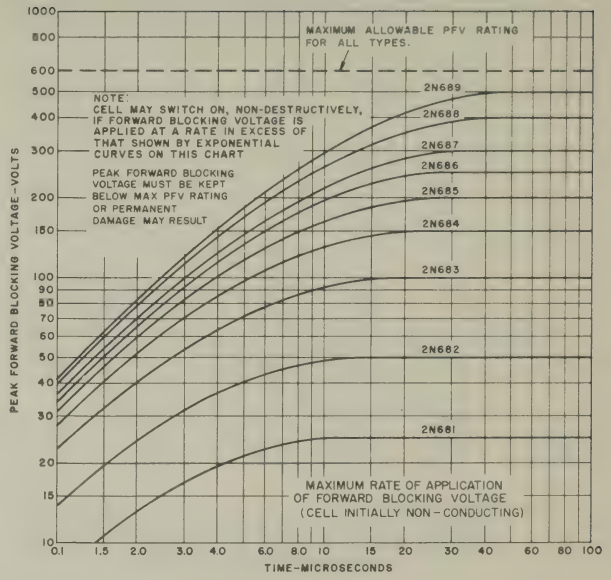
8. Typical Turn-On Time for D-C Currents



9. Maximum Allowable Non-Recurrent Surge Current at Rated Load Conditions


TRANSIENT THERMAL RESISTANCE – °C/WATT
2.0
1.5
1.0
.5
0
.001
.01
.1
1
10
TIME IN SECONDS
MAXIMUM TRANSIENT THERMAL RESISTANCE. JUNCTION TO STUD
CELL MOUNTED ON INFINITE HEAT SINK (STUD TEMPERATURE FIXED)
NOTE:
Curve defines temp rise of junction above heat sink for single load pulse of duration t. Peak allowable dissipation in rectifier for time t, if starting from heat sink temp., equals 125°C (max. T_j) minus maximum heat sink temp, divided by the transient thermal resistance:
$P_{(t)A} = \frac{125°C - T_{(t)at\ sink}}{r_t}$
For optimum ratings and further information, see publication ECG-469 entitled "Power Semiconductor Ratings under Transient and Intermittent Loads."

10. Maximum Transient Thermal Resistance



11. Maximum Rate of Application of Forward Blocking Voltage

TYPE 2N1909-2N1916
(C50 Series)
Outline Drawing No. 5

High Current
Silicon Controlled Rectifier
110 Amperes

Maximum Allowable Ratings (Resistive or Inductive Load, 50 to 400 cps)

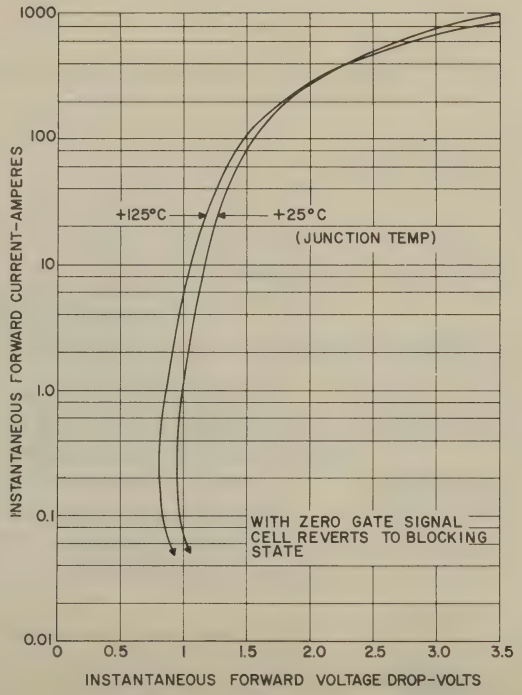
	2N1909 (C50U)	2N1910 (C50F)	2N1911 (C50A)	2N1912 (C50G)	2N1913 (C50B)	2N1914 (C50H)	2N1915 (C50C)	2N1916 (C50D)	..... (C50E)
Transient Peak Reverse Voltage (Non-recurrent <5 millisecond)*	35	75	150	225	300	350	400	500	600 Volts
Repetitive Peak Reverse Voltage (PRV)*	25	50	100	150	200	250	300	400	500 Volts
Repetitive Peak Forward Blocking Voltage (PFV)	500	500	500	500	500	500	500	500	600 Volts
RMS Forward Current	110 amperes (For all conduction angles)								
Average Forward Current (I_F)	Depends on conduction angle (See Chart 4)								
Peak One Cycle Surge Current (I_{surge})	1000 amperes (See Chart 9)								
Peak Current During Turn-on Time Interval	(See Chart 9)								
I^2t (for fusing)	Up to 4000 ampere^2 seconds (See Chart 5)								
Peak Gate Power (p_G)	5 watts								
Average Gate Power (P_G)	0.5 watts								
Peak Gate Current (i_G)	2 amperes								
Peak Gate Voltage (v_G) (Forward)	10 volts								
Peak Gate Voltage (v_G) (Reverse)	5 volts								
Storage and Operating Junction Temperature	−40°C to +125°C (See Chart 4)								
Stud Torque	150 inch-pounds								

Characteristics at Maximum Ratings (125°C Junction Temperature)

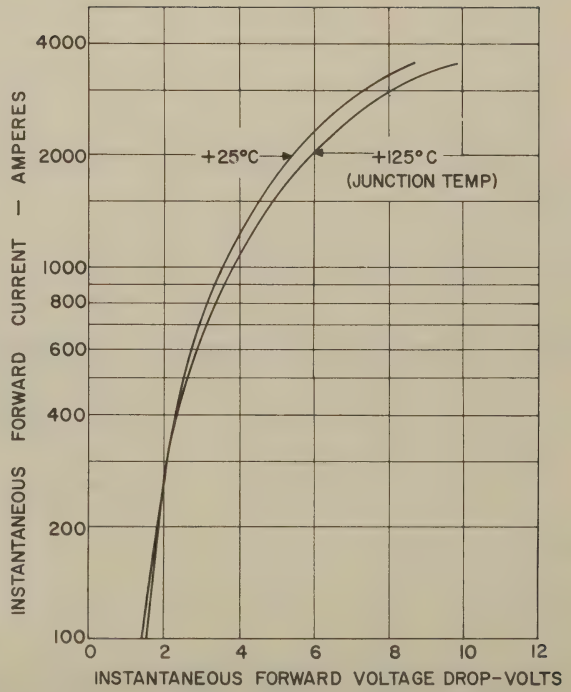
	2N1909 (C50U)	2N1910 (C50F)	2N1911 (C50A)	2N1912 (C50G)	2N1913 (C50B)	2N1914 (C50H)	2N1915 (C50C)	2N1916 (C50D)	..... (C50E)
Minimum Forward Breakover Voltage (V_{BO})	25	50	100	150	200	250	300	400	500 Volts
Maximum Reverse (I_R) or Forward (I_S) Leakage Current (Full Cycle Average)*	6.5	6.5	6.5	6.5	6.0	5.5	5.0	4.0	3.5 ma
Maximum Forward Voltage Drop (Full Cycle Average) ($V_{F\ AVG.}$)	0.80 volts (70 amp avg., 180° conduction angle)								
Gate Firing Characteristics (See Chart 8)									
Maximum Thermal Resistance (R_T)	0.4°C/watt (Junction to Stud) (See Chart 10)								
Typical Holding Current (I_H)	20 ma								

*PRV ratings apply for zero or negative gate voltage. Maximum heatsink thermal resistance for which maximum PRV ratings apply equals 3.5°C/watt.

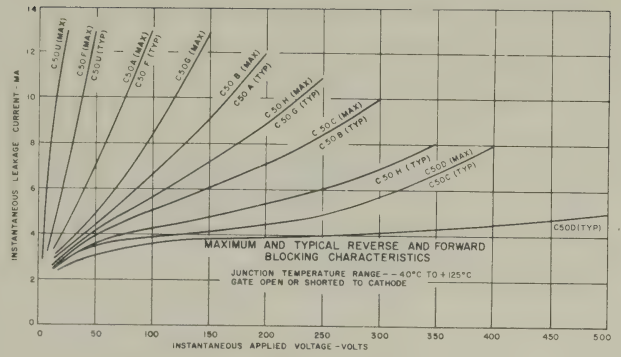
2N1909 (Continued)



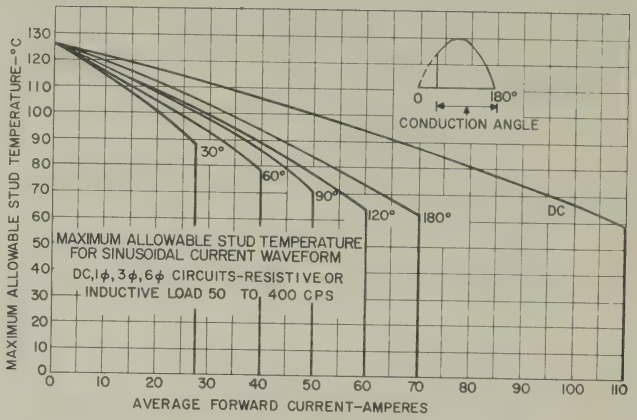
1. Maximum Forward Characteristics Conducting State Low Current Level



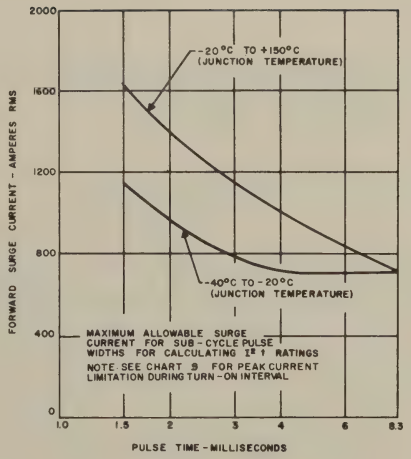
2. Maximum Forward Characteristics Conducting State High Current Level



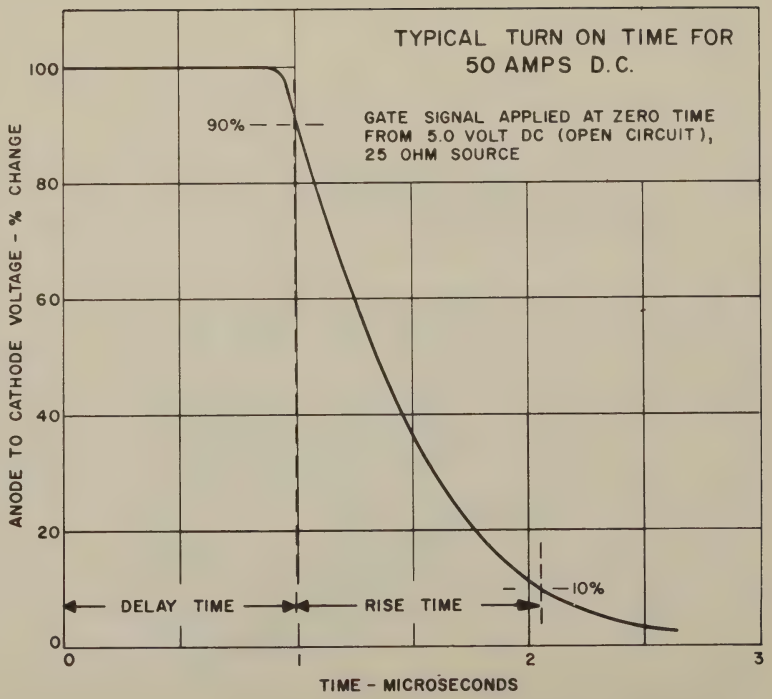
3. Maximum and Typical Reverse and Forward Blocking Characteristics



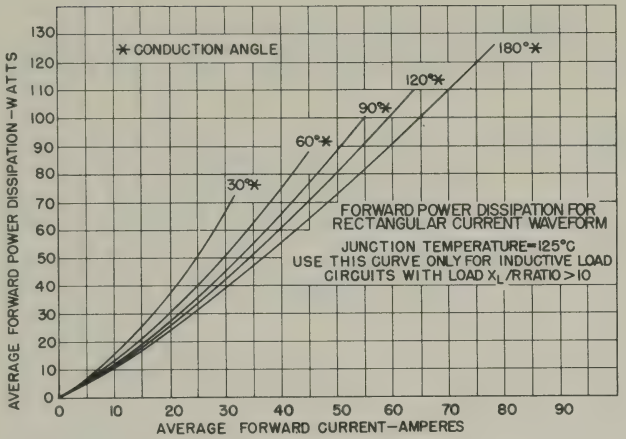
4. Maximum Allowable Stud Temperature for Sinusoidal Current Waveform



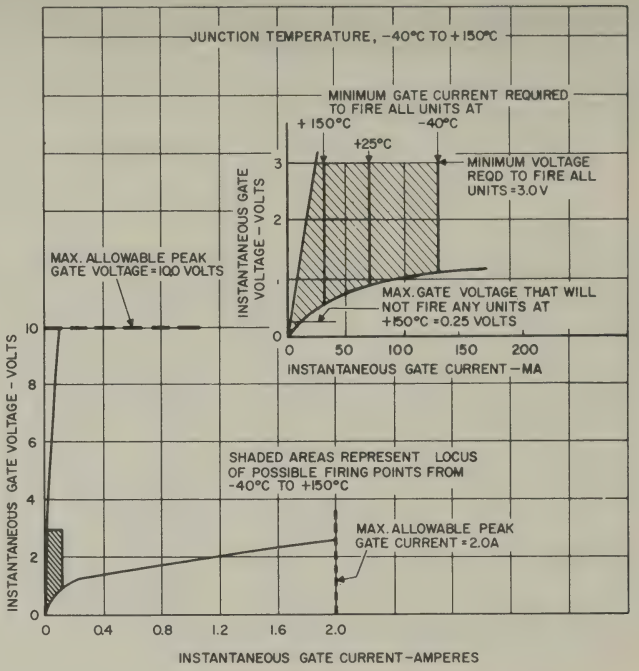
5. Sub-Cycle Rating



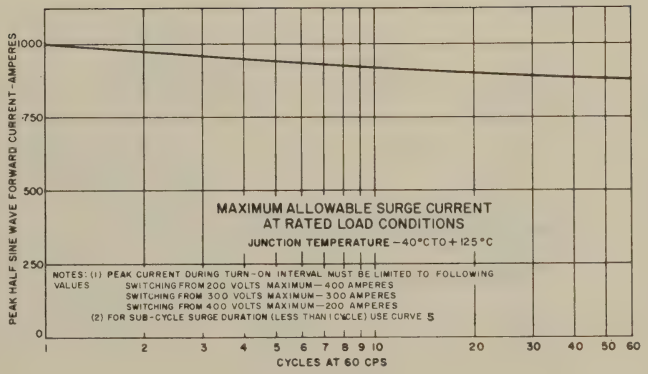
6. Typical Turn-On Time


* CONDUCTION ANGLE
180°*
120°*
90°*
60°*
30°*
FORWARD POWER DISSIPATION FOR RECTANGULAR CURRENT WAVEFORM
JUNCTION TEMPERATURE=125°C
USE THIS CURVE ONLY FOR INDUCTIVE LOAD CIRCUITS WITH LOAD X_L/R RATIO > 10
AVERAGE FORWARD POWER DISSIPATION - WATTS
AVERAGE FORWARD CURRENT - AMPERES
0 10 20 30 40 50 60 70 80 90
0 10 20 30 40 50 60 70 80 90 100 110 120 130

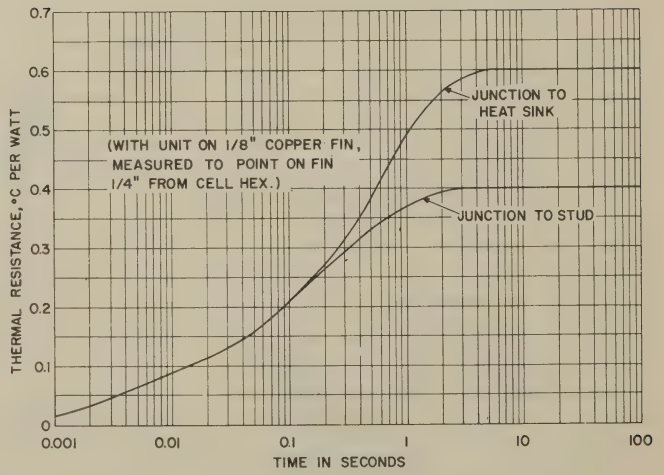
7. Forward Power Dissipation for Rectangular Current Waveform


JUNCTION TEMPERATURE, -40°C TO +150°C
MINIMUM GATE CURRENT REQUIRED TO FIRE ALL UNITS AT
+150°C
-40°C
+25°C
MINIMUM VOLTAGE REQD TO FIRE ALL UNITS = 3.0 V
INSTANTANEOUS GATE VOLTAGE - VOLTS
MAX. ALLOWABLE PEAK GATE VOLTAGE = 10.0 VOLTS
MAX. GATE VOLTAGE THAT WILL NOT FIRE ANY UNITS AT +150°C = 0.25 VOLTS
0 50 100 150 200
INSTANTANEOUS GATE CURRENT - MA
SHADED AREAS REPRESENT LOCUS OF POSSIBLE FIRING POINTS FROM -40°C TO +150°C
MAX. ALLOWABLE PEAK GATE CURRENT = 2.0A
INSTANTANEOUS GATE VOLTAGE - VOLTS
0 0.4 0.8 1.2 1.6 2.0
INSTANTANEOUS GATE CURRENT - AMPERES

8. Firing Characteristics


PEAK HALF SINE WAVE FORWARD CURRENT-AMPERES
1000
750
500
250
0
MAXIMUM ALLOWABLE SURGE CURRENT
AT RATED LOAD CONDITIONS
JUNCTION TEMPERATURE -40°C TO +125°C
NOTES: (1) PEAK CURRENT DURING TURN-ON INTERVAL MUST BE LIMITED TO FOLLOWING VALUES
SWITCHING FROM 200 VOLTS MAXIMUM—400 AMPERES
SWITCHING FROM 300 VOLTS MAXIMUM—300 AMPERES
SWITCHING FROM 400 VOLTS MAXIMUM—200 AMPERES
(2) FOR SUB-CYCLE SURGE DURATION (LESS THAN 1 CYCLE) USE CURVE 5
1 2 3 4 5 6 7 8 9 10 20 30 40 50 60
CYCLES AT 60 CPS

9. Maximum Allowable Surge Current at Rated Load Conditions



10. Maximum Transient Thermal Resistance

TYPE 2N2023-2N2029
(C60 Series)
C61 Series
Outline Drawing No. 5

High Current
Silicon Controlled Rectifier
110 Amperes
(High Temperature Type)

Maximum Allowable Ratings (Resistive or Inductive Load, 50 to 400 cps)

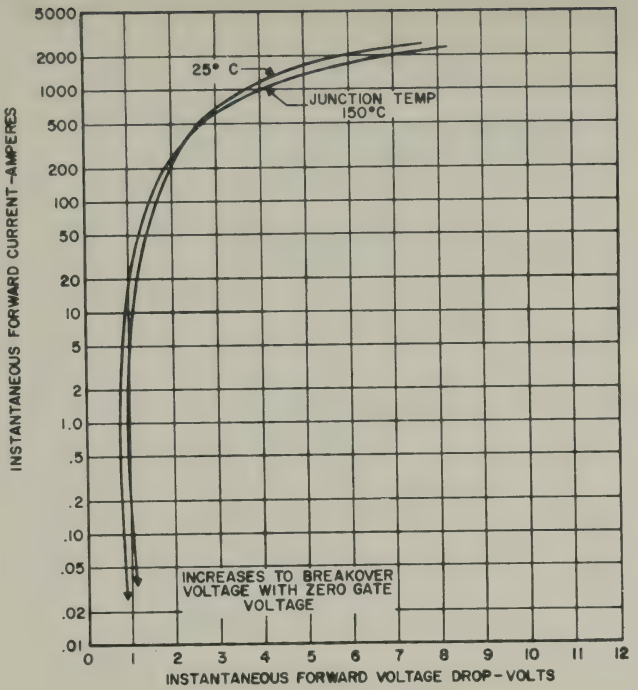
	2N2023 (C60U)	2N2024 (C60F)	2N2025 (C60A)	2N2026 (C60G)	2N2027 (C60B)	2N2028 (C60H)	2N2029 (C60C)	2N2030 (C60D)
Transient Peak Reverse Voltage (Non-recurrent <5 millisecond)*	35	75	150	225	300	350	400	500 volts
Repetitive Peak Reverse Voltage (PRV)*	25	50	100	150	200	250	300	400 volts
Repetitive Peak Forward Blocking Voltage (PFV)	400	400	400	400	400	400	400	500 volts
RMS Forward Current	110 amperes (For all conduction angles)							
Average Forward Current (I_F)	Depends on conduction angle (See Chart 3)							
Peak One Cycle Surge Current (I_{surge})	1000 amperes (See Chart 6)							
I^2t (for fusing)	Up to 4000 ampere² seconds (See Chart 7)							
Peak Gate Power (p_G)	5 watts							
Average Gate Power (P_G)	0.5 watts							
Peak Gate Current (i_G)	2 amperes							
Peak Gate Voltage (v_G) (Forward)	10 volts							
Peak Gate Voltage (v_G) (Reverse)	5 volts							
Storage Temperature	−65°C to +150°C For C60 (−40°C to 150°C For C61)							
Stud Torque	150 inch-pounds							

Characteristics at Maximum Ratings (150°C Junction Temperature)

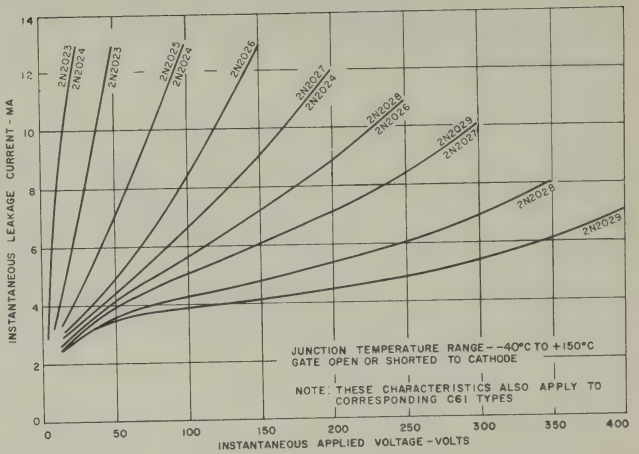
	2N2023 (C60U)	2N2024 (C60F)	2N2025 (C60A)	2N2026 (C60G)	2N2027 (C60B)	2N2028 (C60H)	2N2029 (C60C)	2N2030 (C60D)
Minimum Forward Breakover Voltage (V_{BO})	25	50	100	150	200	250	300	400 volts
Maximum Reverse (I_R) or Forward (I_S) Leakage Current (Full Cycle Average)*	6.5	6.5	6.5	6.5	6.0	5.5	5.0	4.5 ma
Maximum Forward Voltage Drop (Full Cycle Average) ($V_{F\ AVG.}$)	0.8 volts (70 amp avg., 180° conduction angle)							
Gate Firing Characteristics	(See Chart 5)							
Maximum Thermal Resistance (R_T)	.4°C/watt (Junction to Stud)							
Typical Holding Current (I_H)	20 ma							

*PRV ratings apply for zero or negative gate voltage. Minimum heatsink thermal resistance for which maximum PRV ratings apply equals 3.5°C/watt.

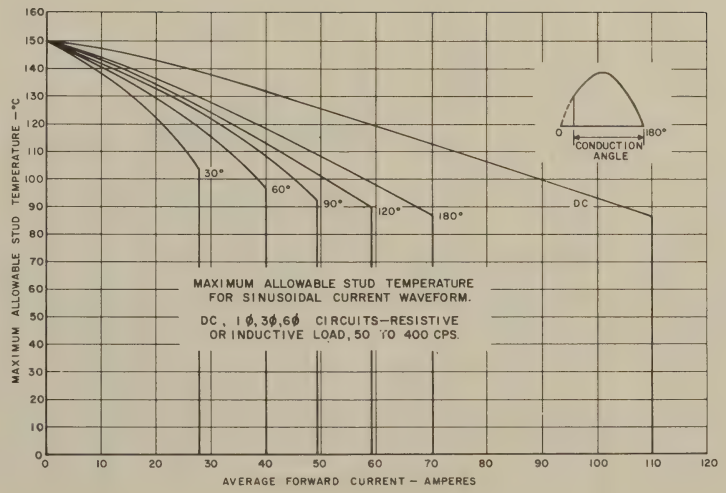
NOTE: Peak current during turn-on interval must be limited to the following values:
Switching from 200 volts or below —400 amperes
Switching from 201 volts or higher —300 amperes



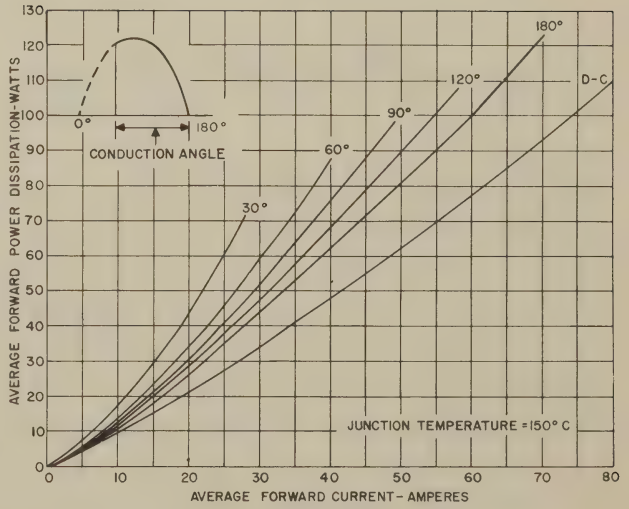
1. Maximum Forward Characteristics Conducting State



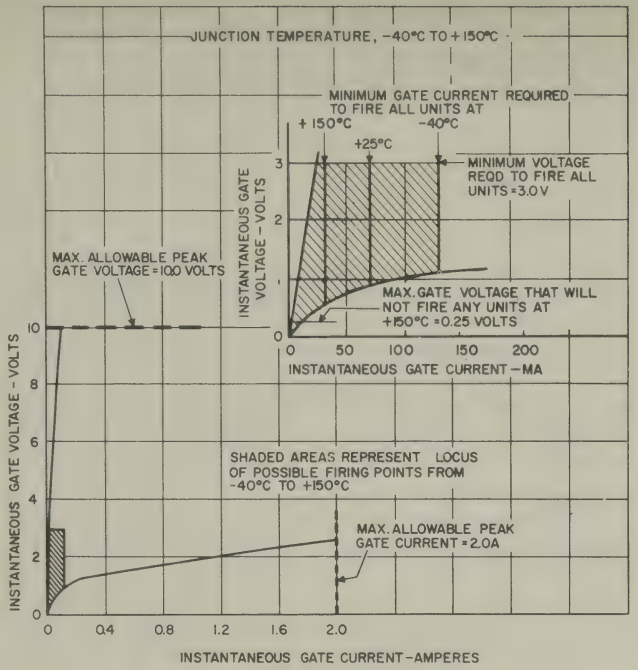
2. Maximum and Typical Reverse and Forward Blocking Characteristics



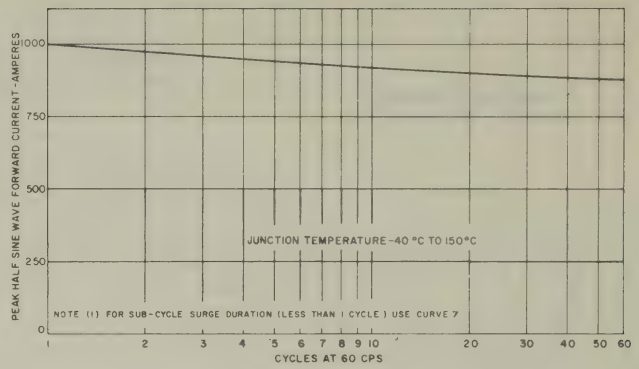
3. Maximum Allowable Stud Temperature for Sinusoidal Current Waveform



4. Forward Power Dissipation for Sinusoidal Current Waveform

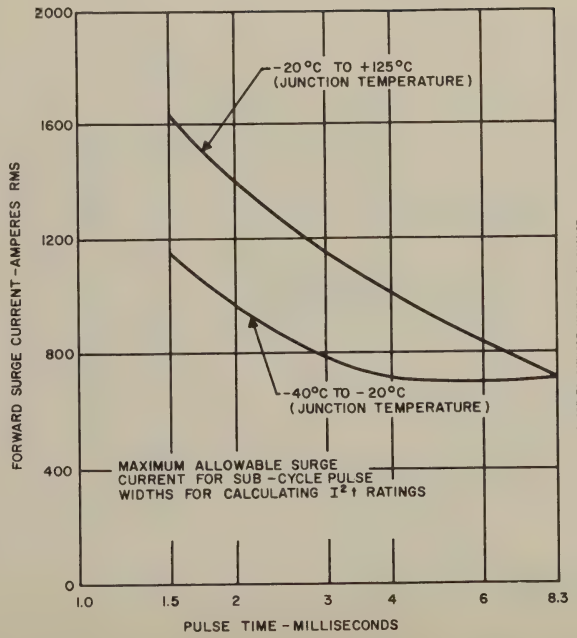

JUNCTION TEMPERATURE, -40°C TO +150°C
MINIMUM GATE CURRENT REQUIRED TO FIRE ALL UNITS AT
+150°C
-40°C
+25°C
MINIMUM VOLTAGE REQD TO FIRE ALL UNITS = 3.0 V
INSTANTANEOUS GATE VOLTAGE - VOLTS
MAX. ALLOWABLE PEAK GATE VOLTAGE = 10.0 VOLTS
MAX. GATE VOLTAGE THAT WILL NOT FIRE ANY UNITS AT +150°C = 0.25 VOLTS
INSTANTANEOUS GATE CURRENT - MA
SHADED AREAS REPRESENT LOCUS OF POSSIBLE FIRING POINTS FROM -40°C TO +150°C
MAX. ALLOWABLE PEAK GATE CURRENT = 2.0A
INSTANTANEOUS GATE VOLTAGE - VOLTS
INSTANTANEOUS GATE CURRENT - AMPERES

5. Firing Characteristics

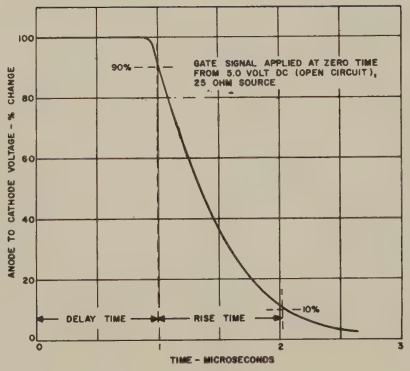

PEAK HALF SINE WAVE FORWARD CURRENT - AMPERES
JUNCTION TEMPERATURE -40 °C TO 150°C
NOTE (1) FOR SUB-CYCLE SURGE DURATION (LESS THAN 1 CYCLE) USE CURVE 7
CYCLES AT 60 CPS

6. Maximum Allowable Surge Current at Rated Load Conditions

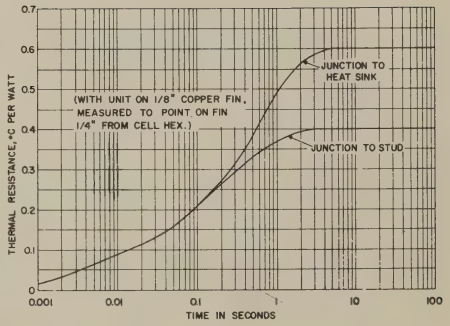
2N2023 (Continued)



7. Sub-Cycle Surge Rating



8. Typical Turn-On Time at Rated Load Conditions



9. Maximum Transient Thermal Resistance

INVERTER TYPE SCR's
C9, C12, C40, C55

Inverter types of Silicon Controlled Rectifiers are specially selected to meet inverter circuit applications, as well as other circuitry that requires a maximum limit on turn-off time. Each of these types is tested to insure that the turn-off time is less than the specified value under the specified test conditions. Turn-off time is defined as the time interval required for the silicon controlled rectifier to regain its forward blocking state after forward current conduction. This time is measured from the point where the forward current reaches zero to the time of reapplication of forward voltage.

For additional information on inverter specifications, refer to Chapter 5 or request the complete Specification Bulletin for the particular SCR.

INVERTER TYPE C9 — Low Current Silicon Controlled Rectifier

The C9 is specially selected from the 2N1929-1935 (C8) series. Ratings and characteristics (with the following additions) apply as described for type 2N1929-1935 (C8) SCR specifications.

Maximum Allowable Ratings *(Note 1)*

	C9U	C9F	C9A	C9G	C9B	C9H	C9C
Repetitive Peak Reverse Voltage (PRV)	25	50	100	150	200	250	300 v
Peak Reverse Current During Turn-Off	5 amperes						
Junction Temperature Range	−65°C to +125°C						

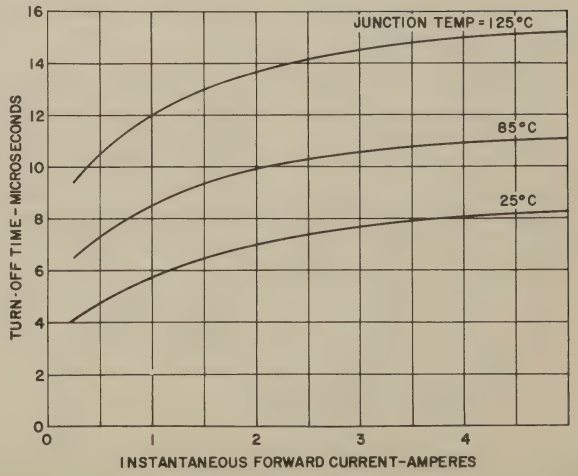
Maximum Turn-Off Time 12 microseconds

Test Conditions for Turn-Off (Note 2)

Instantaneous Forward Current Immediately Before Turn-Off	1 ampere
Peak Reverse Current	1 ampere
Rate of Rise of Reverse Current	1.0 ampere per μsecond
Rate of Rise of Reapplied Forward Blocking Voltage	20 volts per μsecond
Junction Temperature	+125°C

Typical Turn-Off vs Forward Current See Chart

Ambient Temperature Derating Constant for Frequencies above 400 cycles (Note 3) K = 20



Typical Turn-Off Time vs. Forward Current I_F = 1 Amp Peak

INVERTER TYPE C12

Low Current Silicon Controlled Rectifier

The C12 is specially selected from the 2N1770-1777 (C11) series. Ratings and characteristics (with the following additions) apply as described for type 2N1770-1777 (C11) SCR specifications.

Maximum Allowable Ratings *(Note 1)*

	C12U	C12F	C12A	C12G	C12B	C12H	C12C
Repetitive Peak Reverse Voltage (PRV)	25	50	100	150	200	250	300 v
Peak Reverse Current During Turn-Off	15 amperes						
Junction Temperature Range	−65°C to +125°C						

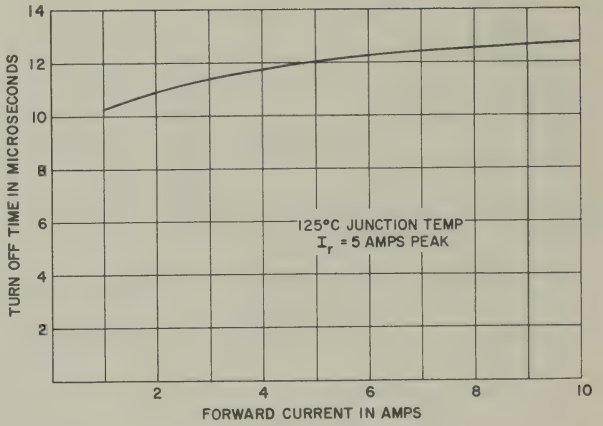
Maximum Turn-Off Time 12 microseconds

Test Conditions for Turn-Off (Note 2)

Instantaneous Forward Current Immediately Before Turn-Off	5 amperes
Peak Reverse Current	5 amperes
Rate of Rise of Reverse Current	5 amperes per μsecond
Rate of Rise of Reapplied Forward Blocking Voltage	20 volts per μsecond
Junction Temperature	+125°C

Typical Turn-Off vs Forward Current See Chart

Stud Temperature Derating Constant for Frequencies above 400 cycles (Note 3) K = 2



Typical Turn-Off Time vs. Forward Current

INVERTER TYPE C40 — Medium Current Silicon Controlled Rectifier

The C40 is specially selected from the 2N681-689 (C35) series. Ratings and characteristics (with the following additions) apply as described for type 2N681-689 (C35) SCR specifications.

Maximum Allowable Ratings *(Note 1)*

	C40U	C40F	C40A	C40G	C40B	C40H	C40C
Pepetitive Peak Reverse Voltage (PRV)	25	50	100	150	200	250	300 v
Peak Reverse Current During Turn-Off	20 amperes						
Junction Temperature Range	−65°C to +125°C						

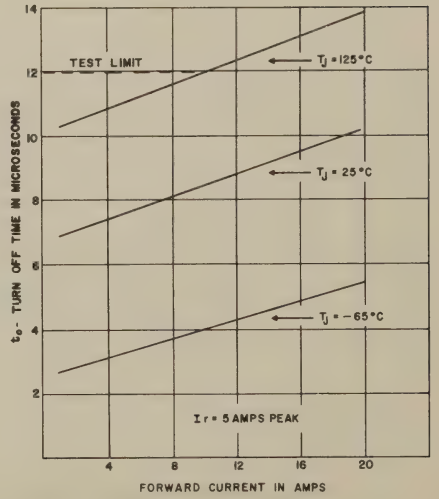
Maximum Turn-Off Time 12 microseconds

Test Conditions for Turn-Off (Note 2)

Instantaneous Forward Current Immediately Before Turn-Off	10 amperes
Peak Reverse Current	5 amperes
Rate of Rise of Reverse Current	5 amperes per μsecond
Rate of Rise of Reapplied Forward Blocking Voltage	20 volts per μsecond
Junction Temperature	+125°C

Typical Turn-Off vs Forward Current See Chart

Stud Temperature Derating Constant for Frequencies above 400 cycles (Note 3) K = 1.3



Typical Turn-Off Time vs. Forward Current

INVERTER TYPE C55 — High Current Silicon Controlled Rectifier

The C55 is specially selected from the 2N1906-1916 (C50) series. Ratings and characteristics (with the following additions) apply as described for type 2N1906-1916 (C50) SCR specifications.

Maximum Allowable Ratings *(Note 1)*

	C55U	C55F	C55A	C55G	C55B	C55H	C55C
Repetitive Peak Reverse Voltage (PRV)	25	50	100	150	200	250	300 v
Peak Reverse Current During Turn-Off	30 amperes						
Junction Temperature Range	−65°C to +125°C						

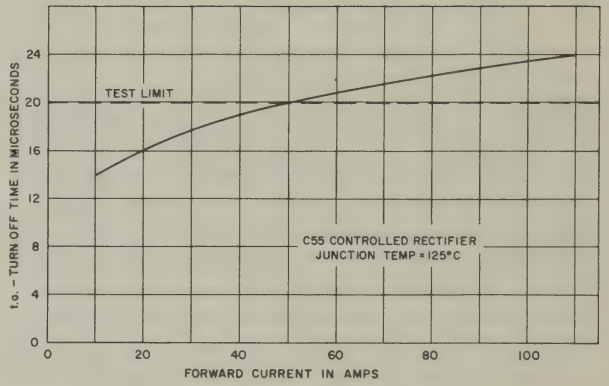
Maximum Turn-Off Time 20 microseconds

Test Conditions for Turn-Off (Note 2)

Instantaneous Forward Current Immediately Before Turn-Off	50 amperes
Peak Reverse Current	10 amperes
Rate of Rise of Reverse Current	5 amperes per μsecond
Rate of Rise of Reapplied Forward Blocking Voltage	20 volts per μsecond
Junction Temperature	+125°C

Typical Turn-Off vs Forward Current See Chart

Stud Temperature Derating Constant for Frequencies above 400 cycles (Note 3) K = 0.3



Typical Turn-Off Time vs. Forward Current I_F = 10 Amps Peak

Note 1

The specified peak reverse voltage (PRV) and peak reverse current ratings must not be exceeded. The peak reverse current during turn-off must be high enough to allow recovery of the device. The reverse voltage level during recovery affects both turn-off time and the rate of rise capability of the reapplied forward voltage. The factory test condition of 2.0 volts maximum reverse voltage during this interval is a conservative value and assures satisfactory performance at the higher reverse voltages.

Note 2

Many circuit variables have a pronounced effect on turn-off time. Decreasing the junction temperature from the test value of 125C to 25C reduces the turn-off time. Similarly, decreasing the magnitude of forward current just before turn-off reduces turn-off time. Note that the test conditions have been selected to give the maximum turn-off time of the SCR for nominal load conditions.

Note 3

At normal power frequencies in the range of 50 to 400 cps the switching losses are small and normally constitute a negligible portion of the total losses. At frequencies above 400 cps the switching losses during the turn-on interval can contribute significantly to the total losses if the circuit L/R time constant is short (10 microseconds or less) so that the build-up of current is essentially determined by the collapse of voltage across the controlled rectifier. When these conditions exist it becomes necessary to derate the average forward current vs. stud (ambient for C9) temperature relationship. The following equation gives the Stud Temperature derating in °C which must be subtracted from the value read on the inverter specification sheet for the particular average current and conduction angle:

$$\Delta T = K\, f V_m I_m \times 10^{-6}$$

where K = constant for the particular inverter type SCR

ΔT = stud temperature derating in °C (ambient temperature for C9)

f = operating frequency in cps

V_m = instantaneous anode voltage immediately prior to switching

I_m = instantaneous anode current immediately after switching

CONDENSED SPECIFICATION ON UNIJUNCTION TRANSISTORS 2N1671, 2N1671A, 2N1671B

Outline Drawing No. 6

The 2N1671 is intended for general purpose industrial applications where circuit economy is of primary importance. The 2N1671A is intended for industrial use in firing circuits for Silicon Controlled Rectifiers and other applications where a guaranteed minimum pulse amplitude is required. The 2N1671B is intended for applications where a low emitter leakage current and a low peak point emitter current (trigger current) are required.

For additional information on Unijunction Transistors, request the complete Specification Bulletin.

Electrical Characteristics (25°C)

Parameter	Symbol	Note	2N1671		2N1671A		2N1671B		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Intrinsic Standoff Ratio ($V_{BB} = 10v$)	η	3	0.47	0.62	0.47	0.62	0.47	0.62	
Interbase Resistance ($V_{BB} = 3V$, $I_E = 0$)	R_{BBO}	4	4.7	9.1	4.7	9.1	4.7	9.1	KΩ
Emitter Saturation Voltage ($V_{BB} = 10V$, $I_E = 50ma$)	$V_E(SAT)$			5		5		5	volts
Modulated Interbase Current ($V_{BB} = 10V$, $I_E = 50ma$)	$I_{B2}(MOD)$		6.8	22	6.8	22	6.8	22	ma
Emitter Reverse Current ($V_{B2E} = 30V$, $I_{B1} = 0$)	I_{EO}			12		12		0.2	μa
Peak Point Emitter Current ($V_{BB} = 25V$)	I_P			25		25		6	μa
Valley Point Current ($V_{BB} = 20V$, $R_{B2} = 100\Omega$)	I_V		8		8		8		ma
Base-One Peak Pulse Voltage	V_{OB1}	5			3.0		3.0		volts

Absolute Maximum Ratings (25°C)

RMS Power Dissipation	450 mw[1]
RMS Emitter Current	50 ma
Peak Emitter Current[2]	2 amperes
Emitter Reverse Voltage	30 volts
Interbase Voltage	35 volts
Operating Temperature Range	−65°C to +140°C
Storage Temperature Range	−65°C to +150°C

Notes:

(1) Derate 3.9 MW/°C increase in ambient temperature (Thermal resistance to case = 0.16°C/MW).

(2) Capacitor discharge—10μfd or less, 30 volts or less—total interbase power dissipation must be limited by external circuitry.

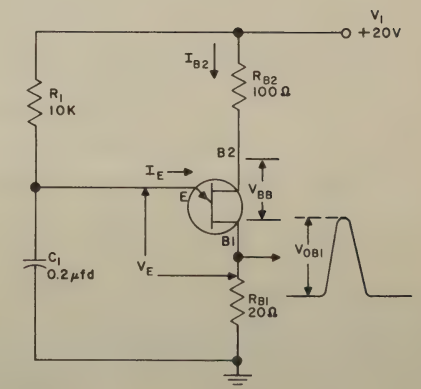
(3) The intrinsic standoff ratio, η, is essentially constant with temperature and interbase voltage. η is defined by the equation:

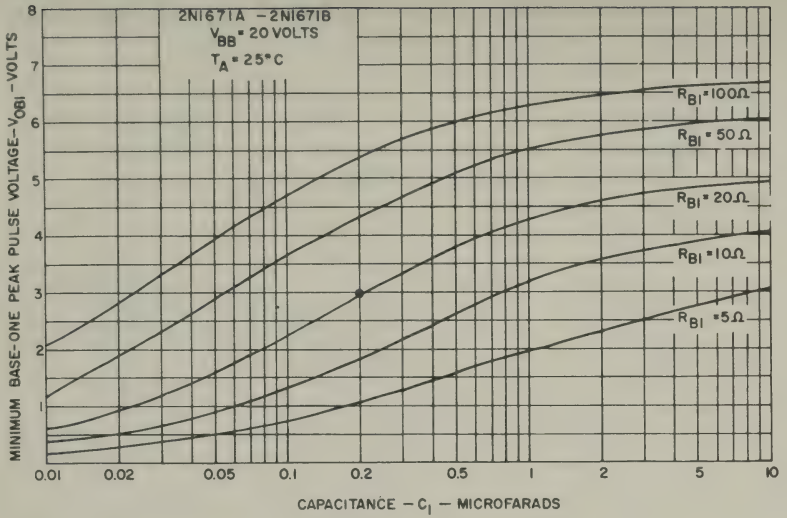
$$V_P = \eta V_{BB} + \frac{200}{T_J}$$

Where V_P = Peak point emitter voltage
V_{BB} = Interbase voltage
T_J = Junction temperature (degrees Kelvin)

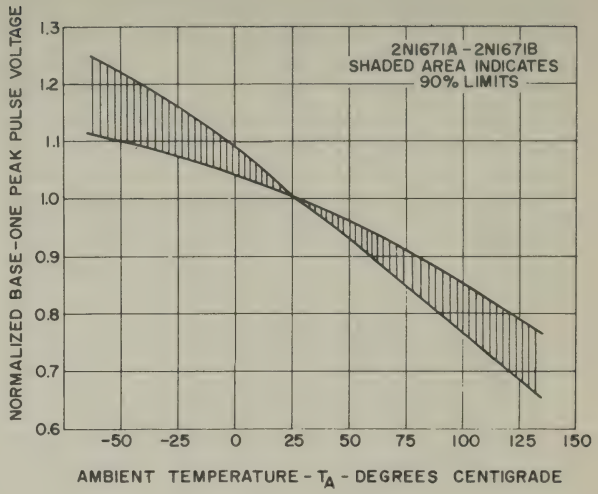
(4) The interbase resistance is nearly ohmic and increases with temperature in a well defined manner. The temperature coefficient at 25°C is approximatly 0.8%/°C.

(5) The base-one peak pulse voltage is measured in the circuit below. This specification on the 2N1671A is used to ensure a minimum pulse amplitude for applications in SCR firing circuits and other types of pulse circuits. The variation of pulse amplitude with temperature and circuit parameters is shown in the following figures:

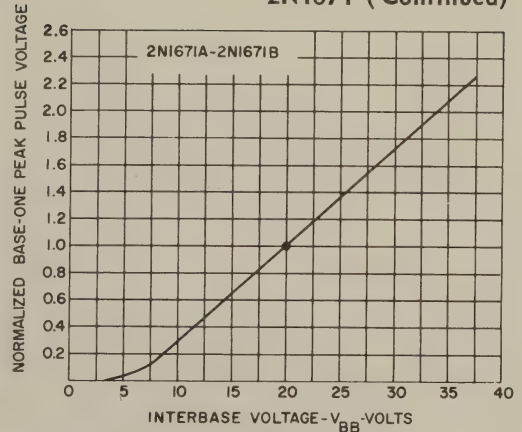




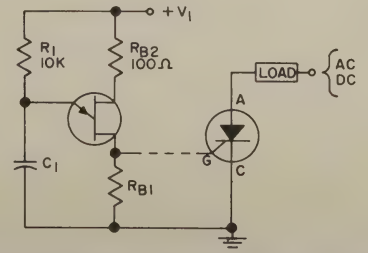
1. Minimum base-one peak pulse voltage vs. capacitance and base-one resistance in relaxation oscillator circuit.



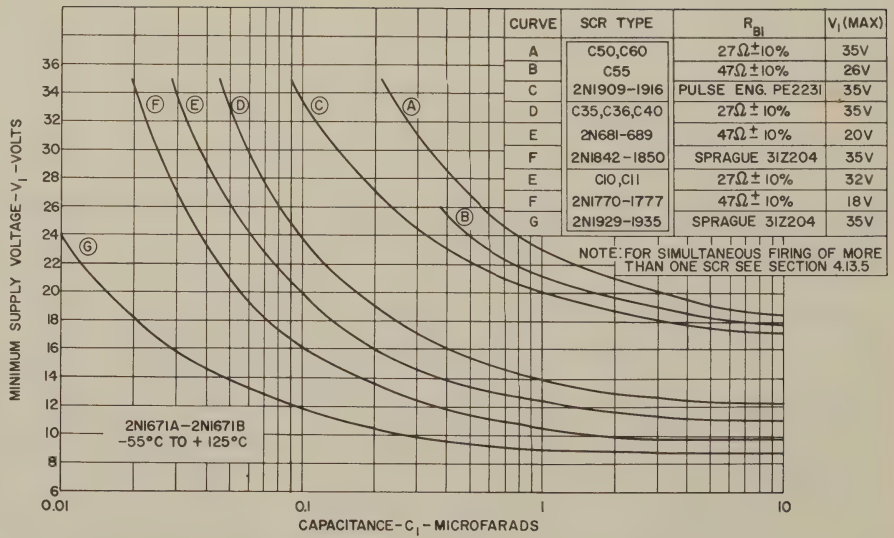
2. Normalized base-one peak pulse voltage vs. temperature in relaxation oscillator circuit.



3. Normalized base-one peak pulse voltage vs. interbase voltage in relaxation oscillator circuit.



5. Basic unijunction transistor firing circuit for silicon controlled rectifiers.


MINIMUM SUPPLY VOLTAGE-V_1-VOLTS
2N1671A-2N1671B
-55°C TO +125°C
CAPACITANCE-C_1-MICROFARADS
NOTE: FOR SIMULTANEOUS FIRING OF MORE THAN ONE SCR SEE SECTION 4.13.5

CURVE	SCR TYPE	R_{B1}	V_1(MAX)
A	C50,C60	27Ω±10%	35V
B	C55	47Ω±10%	26V
C	2N1909-1916	PULSE ENG. PE2231	35V
D	C35,C36,C40	27Ω±10%	35V
E	2N681-689	47Ω±10%	20V
F	2N1842-1850	SPRAGUE 31Z204	35V
E	C10,C11	27Ω±10%	32V
F	2N1770-1777	47Ω±10%	18V
G	2N1929-1935	SPRAGUE 31Z204	35V

4. Minimum supply voltage required to fire standard types of silicon controlled rectifiers vs. capacitance in circuit of Fig. 5.

Period of Relaxation Oscillator $\tau = 0.80\ R_1C_1$ ($\pm 0.21\ R_1C_1$)
Maximum Value of R_1 for oscillation (−55°C to +140°C)
R_1 (max) = $430\ V_1^2$ (2N1671-2N1671A)
R_1 (max) = $1800\ V_1^2$ (2N1671B)
τ = Period in Seconds

C_1 = Capacitance in Farads
R_1 = Resistance in ohms
V_1 = Supply voltage in volts

G-E SCR's, RECTIFIERS, AND UNIJUNCTION TRANSISTORS WORK WELL TOGETHER!

G-E CONTROLLED RECTIFIER (SCR) TYPE	COMPATIBLE RECTIFIER					COMPATIBLE UNIJUNCTION FIRING TRANSISTOR
	G-E Rectifier Type	Max. Cont. Rectifier Current @ Stud Temperature	Peak 1 Cycle Surge	Max. Rectifier Transient PRV	Package	
2N1595-2N1599	1N536-1N547	.75 A @ 50°C Amb.	15 A	800 V	Double Ended Lead	2N1671A
2N1929-1N1935 (C8)	1N1341A-1N1348A	7 A @ 140°C	150 A	800 V	7/16" Hex	2N1671A
C9	1N1341A-1N1348A	7 A @ 140°C	150 A	800 V	7/16" Hex	2N1671A
2N1770A-2N1777A (C10)	1N1341A-1N1348A	7 A @ 140°C	150 A	800 V	7/16" Hex	2N1671A
2N1770-2N1777 (C11)	1N1341A-1N1348A	7 A @ 140°C	150 A	800 V	7/16" Hex	2N1671A
C12	1N1341A-1N1348A	7 A @ 140°C	150 A	800 V	7/16" Hex	2N1671A
2N681-2N689 (C35)	1N1199A-1N1206A	12 A @ 150°C	240 A	800 V	7/16" Hex	2N1671A
	1N2154-1N2160	25 A @ 145°C	400 A	800 V	11/16" Hex	2N1671A
2N1842-2N1850 (C36)	1N1341A-1N1348A	7 A @ 140°C	150 A	800 V	7/16" Hex	2N1671A
	1N1199A-1N1206A	12 A @ 150°C	240 A	800 V	7/16" Hex	2N1671A
C40	1N1199A-1N1348A	12 A @ 150°C	240 A	800 V	7/16" Hex	2N1671A
2N1909-2N1916 (C50)	1N3289-1N3293	70 A @ 150°C	1600 A	1300 V	1 1/16" Hex	2N1671A
C55	1N3289-1N3293	70 A @ 150°C	1600 A	1300 V	1 1/16" Hex	2N1671A
2N2023-2N2030 (C60)	1N3289-1N3293	70 A @ 150°C	1600 A	1300 V	1 1/16" Hex	2N1671A

Stack assemblies available for all rectifier types listed.

RECTIFIER CELLS CONDENSED SPECIFICATIONS

A casual glance through the circuits on the foregoing pages shows that diode rectifier cells play an important role in SCR circuitry. Rectifiers in series with SCR's help them to block reverse voltage. Other rectifiers act as free-wheeling elements across inductive loads, and some circuits employ rectifiers as companion elements to SCR's in the non-controllable legs of bridge circuits. Low current rectifiers appear in large numbers of every practical SCR circuit as power supplies for control purposes, and as clamps and blocking elements in SCR gate firing circuits.

General Electric activity with metallic rectifiers dates back to 1927 when copper oxide ruled the dry type rectifier field unchallenged. Ten years later G.E. introduced its line of selenium rectifiers.

More recently, in 1950, General Electric made the first single crystal large area rectifier cell. Fabricated from germanium, this cell was the grandfather of the vast germanium and silicon rectifier industry that has sprung up in the decade since then.

In addition to their vital help in SCR circuitry, silicon and germanium rectifier cells have contributed to the success of the SCR in another significant way. In order to develop the first successful SCR, G.E. drew heavily on its long experience in designing and manufacturing reliable rectifier cells. Without the large storehouse of rectifier "know-how," the SCR might not be a reality even today. Welded hermetic seals, high voltage characteristics, surface stabilization techniques, absence of thermal fatigue limitations, rating and application philosophies . . . these are only a few of the areas in which the SCR capitalized on G-E rectifier preeminence.

General Electric's work in subduing Thermal Fatigue, a major Semiconductor killer, has helped earn it the reputation of being the quality Semiconductor Rectifier producer of the industry. In addition, the Rectifier Components Department has recognized the problems associated with Transient Voltages and has rated its devices accordingly.

In the medium and high-current rectifiers, General Electric has completely eliminated soft solder joints, thus greatly reducing the problem of thermal fatigue. This means that G-E Rectifiers and Controlled Rectifiers can be worked right up to maximum current and temperature ratings, even on highly cyclical loads.

In addition, all General Electric rectifiers and Controlled Rectifiers carry *transient* PRV ratings which give the user additional protection against voltage transients.

The rectifier cells shown are listed in ascending order based on forward current ratings in each section. Maximum full load voltage drop is taken at full cycle average unless otherwise specified.

Finned Assemblies

General Electric silicon and germanium rectifier cells are also available in pre-assembled stacks complete with heatsink and electrical interconnections for a great variety of typical rectifier circuits.

Potted High Voltage Assemblies

For applications up to 10,000 volts PRV, low current silicon rectifiers are also available in a preassembled encapsulation complete with high quality capacitors shunting the rectifier cells for commutation assistance and transient voltage protection.

You will find a General Electric rectifier cell or stack available for every job to be done in conjunction with SCR's. The following pages list the various germanium and silicon types together with condensed specifications on each.

Complete specifications are available through your Semiconductor Products District Sales office or through your authorized G-E Semiconductor Distributor.

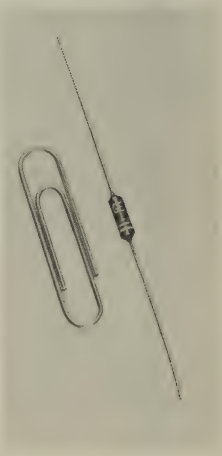
G-E rectifiers and SCR's work well together!

Silicon Subminiature Glass Rectifier Cells (Lead Mounted)

Up to 400 MA ***Up to 600 PRV***

JEDEC or GE Type Number	Repetitive PRV	Transient PRV	Max. I_{DC} at T°C	Max. Rev. Cur. (Full Cycle Av.)	Max. Full Load Voltage Drop	Max. Oper.*	Outline No.	COMMENTS
			@ 25°C	@ 100°C	@ 25°C			
1N645	225	275	400 ma	15 μa	1V	175°	7	
1N646	300	360	400 ma	15 μa	1V	175°	7	Designed for maximum thermal conductance. Rugged design to meet military requirements.
1N647	400	480	400 ma	20 μa	1V	175°	7	
1N648	500	600	400 ma	20 μa	1V	175°	7	
1N649	600	720	400 ma	25 μa	1V	175°	7	
1N677	100	120	400 ma	.2 ma @ 150°C	1V	175°	7	

1N676-1N679, 1N681-1N687 and 1N689 are also available in this package.



Germanium Low Current Rectifier Cells
Up to 1200 MA

Up to 400 PRV

JEDEC or GE Type Number	PRV	Max. I_{DC} at T°C	Max. Peak 1 cycle Surge	Max. Rev. Current (full cycle Av.)	Max. Full Load Voltage Drop	Max. Oper. °C	Outline No.	COMMENTS
		@ 55°C Amb.						
1N93	300	75 ma	25A	.6 ma	.18V	95°	8	
USN 1N93	300	75 ma	25A	.6 ma	.18V	95°	8	
1N315	300	75 ma	25A	Min. Fwd./Rev. Ratio-700 @ 55°C		85°	8	
USAF 1N315	300	75 ma	25A	Min. Fwd./Rev. Ratio-700 @ 55°C		85°	8	Industry standard for high reliability units. Feature extremely low forward resistance, high back resistance.
1N368	200	100 ma	25A	.3 ma @ 150 V.D.C.	.48V	55°	8	
1N92	200	100 ma	25A	.95 ma	.19V	95°	8	
1N91	100	150 ma	25A	1.35 ma	.22V	95°	8	
1N153	300	750 ma	25A			95°	9	
1N158	400	1000 ma	25A			95°	10	
1N152	200	1000 ma	25A			95°	9	
1N151	100	1200 ma	25A			95°	9	

Silicon Low Current Rectifier Cells (Lead Mounted)
Up to 750 MA — *Up to 1000 PRV*

JEDEC or GE Type Number	PRV	Max. I_{DC} @ T°C Amb.	Max. Peak 1 cycle Surge	Max. Rev. Cur. (Full cycle Av.)	Max. Full Load Voltage Drop	Max. Oper. °C	Outline No.	COMMENTS
		@ 50°C		@ 25°C	@ 25°C			
1N440	100	300 ma	15A	.3 μa	1.5V peak	150°	8	
1N441	200	300 ma	15A	.75 μa	1.5V	150°	8	Refer also to 1N440-B-5B
1N442	300	300 ma	15A	1.0 μa	1.5V	150°	8	Specification Sheet.
1N443	400	300 ma	15A	1.5 μa	1.5V	150°	8	
1N444	500	300 ma	15A	1.75 μa	1.5V	150°	8	
1N445	600	300 ma	15A	2.0 μa	1.5V	150°	8	
		@ 25°C			@ 200 ma			
1N599	50	600 ma	10A	1.0 μa	1.5V peak	150°	8	
1N599A	50	600 ma	10A	1.0 μa	1.5V	150°	8	
1N600	100	600 ma	10A	1.0 μa	1.5V	150°	8	
1N600A	100	600 ma	10A	1.0 μa	1.5V	150°	8	Refer also to 1N440-B-5B
1N601	150	600 ma	10A	1.0 μa	1.5V	150°	8	Specification Sheet.
1N601A	150	600 ma	10A	1.0 μa	1.5V	150°	8	
1N602	200	600 ma	10A	1.0 μa	1.5V	150°	8	
1N602A	200	600 ma	10A	1.0 μa	1.5V	150°	8	
1N603A	300	600 ma	10A	1.0 μa	1.5V	150°	8	
1N603A	300	600 ma	10A	1.0 μa	1.5V	150°	8	
1N604	400	600 ma	10A	1.5 μa	1.5V	150°	8	
1N604A	400	600 ma	10A	1.5 μa	1.5V	150°	8	
1N605	500	600 ma	10A	2.0 μa	1.5V	150°	8	
1N605A	500	600 ma	10A	2.0 μa	1.5V	150°	8	
1N606	600	600 ma	10A	2.5 μa	1.5V	150°	8	
1N606A	600	600 ma	10A	2.5 μa	1.5V	150°	8	
		@ 30°C		@ 150°C	@ 150°C			
1N560	800	600 ma	15A	.3 ma	0.5V	150°	8	Now with transient PRV
1N561	1000	600 ma	15A	.3 ma	0.5V	150°	8	ratings up to 1200V.

Silicon Low Current Rectifier Cells (Lead Mounted)

JEDEC or GE Type Number	PRV	Max. I_{DC} @ T°C Amb.	Max. Peak 1 cycle Surge	Max. Rev. Cur. (Full cycle Av.)	Max. Full Load Voltage Drop	Max. Oper. °C	Outline No.	COMMENTS
		@ 50°C		@ 100°C	@ 100°C			
1N1692	100	600 ma	20A	.5 ma	0.6V	115°	8	
1N1693	200	600 ma	20A	.5 ma	0.6V	115°	8	Similar to 1N536-47 series
1N1694	300	600 ma	20A	.5 ma	0.6V	115°	8	except for lower temp.
1N1695	400	600 ma	20A	.5 ma	0.6V	115°	8	and current operation. Lowest
1N1696	500	600 ma	20A	.5 ma	0.6V	115°	8	priced series.
1N1697	600	600 ma	20A	.5 ma	0.6V	115°	8	
				@ 25°C	@ 25°C			
1N444B	500	650 ma	15A	1.75 μa	1.5V peak	150°	8	
1N445B	600	650 ma	15A	2.0 μa	1.5V	150°	8	Very low leakage. Ideal for
1N440B	100	750 ma	15A	0.3 μa	1.5V	165°	8	magnetic-amplifier
1N441B	200	750 ma	15A	0.75 μa	1.5V	165°	8	applications.
1N442B	300	750 ma	15A	1.0 μa	1.5V	165°	8	Premium price.
1N443B	400	750 ma	15A	1.5 μa	1.5V	165°	8	
		@ 50°C		@ 150°C				
1N1100	100	750 ma	15A	.3 ma	1.5V peak	165°	8	
1N1101	200	750 ma	15A	.3 ma	1.5V	165°	8	Refer also to 1N536-540
1N1102	300	750 ma	15A	.3 ma	1.5V	165°	8	Specification Sheet.
1N1103	400	750 ma	15A	.3 ma	1.5V	165°	8	
		@ 25°C		@ 125°C	@ 125°C			
1N1487	100	750 ma	15A	.4 ma	.55V	140°	8	
1N1488	200	750 ma	15A	.3 ma	.55V	140°	8	Similar to 1N536-47 series.
1N1489	300	750 ma	15A	.3 ma	.55V	140°	8	Intermediate temp. operation.
1N1490	400	750 ma	15A	.3 ma	.55V	140°	8	Lower priced.
1N1491	500	750 ma	15A	.3 ma	.55V	125°	8	
1N1492	600	750 ma	15A	.3 ma	.55V	120°	8	

Silicon Low Current Rectifier Cells (Lead Mounted)

JEDEC or GE Type Number	PRV	Max. I_{DC} @ T°C Amb.	Max. Peak 1 cycle Surge	Max. Rev. Cur. (Full cycle Av.)	Max. Full Load Voltage Drop	Max. Oper. °C	Outline No.	COMMENTS
		@ 50°C		@ 150°C	@ 150°C			
1N536	50	750 ma	15A	.4 ma	.5V	165°	8	The popular line. Provides maximum forward conductance at high operating temperatures (165°C). Now with transient PRV ratings up to 800V.
1N537	100	750 ma	15A	.4 ma	.5V	165°	8	
1N538*	200	750 ma	15A	.3 ma	.5V	165°	8	
1N539	300	750 ma	15A	.3 ma	.5V	165°	8	
1N540*	400	750 ma	15A	.3 ma	.5V	165°	8	
1N1095	500	750 ma	15A	.3 ma	.5V	150°	8	
1N1096	600	750 ma	15A	.3 ma	.5V	150°	8	
1N547*	600	750 ma	15A	.3 ma	.5V	165°	8	
		@ 110°C		@ 150°C	@ 125°C			
1N1217	50	500 ma	15A	1.5 ma	1.0V	175°	8	
1N1217A					1.0V	175°	8	
1N1218	100	500 ma	15A	1.5 ma	1.0V	175°	8	
1N1218A					1.0V	175°	8	
1N1219	150	500 ma	15A	1.5 ma	1.0V	175°	8	
1N1219A					1.0V	175°	8	
1N1220	200	500 ma	15A	1.5 ma	1.0V	175°	8	
1N1220A					1.0V	175°	8	
1N1221	300	500 ma	15A	1.5 ma	1.0V	175°	8	
1N1221A					1.0V	175°	8	
		@ 100°C						
1N1222	400	500 ma	15A	1.5 ma	1.0V	175°	8	
1N1222A		@ 110°C			1.0V	175°	8	
		@ 100°C						
1N1223	500	500 ma	15A	1.5 ma	1.0V	175°	8	
1N1223A		@ 110°C			1.0V	175°	8	
		@ 90°C						
1N1224	600	500 ma	15A	1.5 ma	1.0V	175°	8	
1N1224A		@ 110°C			1.0V	175°	8	

*Military Approved units also available.

Silicon Low Current Rectifier Cells (Stud Mounted)
Up to 1.5 Amps — *Up to 1000 PRV*

JEDEC or GE Type Number	PRV	Max. I_{DC} @ T°C	Max. Peak 1 cycle Surge	Max. Rev. Cur. (Full cycle Av.)	Max. Full Load Voltage Drop	Max. Oper. °C	Outline No.	COMMENTS
1N256*	570	@ 135° Case 200 ma	1A, 3 ms	@ 135°C 25 ma	2V @ 500 ma	150°		Refer also to 1N1115-1120 Specification Sheet.
		@ 150° Case		@ 150°C				
1N340	100	200 ma	10A	1 ma	2V @ 400 ma	170°	11	
1N349	100	200 ma	10A	1 ma	2V @ 400 ma	170°	11	
1N337	200	200 ma	10A	1 ma	2V @ 400 ma	170°	11	
1N346	200	200 ma	10A	5 ma	2V @ 400 ma	170°	11	
1N335	300	200 ma	10A	2 ma	2V @ 400 ma	170°	11	For applications requiring moderate currents operating up to 170°C.
1N344	300	200 ma	10A	5 ma	2V @ 400 ma	170°	11	
1N333	400	200 ma	10A	2 ma	2V @ 400 ma	170°	11	
1N342	400	200 ma	10A	5 ma	2V @ 400 ma	170°	11	
1N339	100	400 ma	15A	1 ma	2V @ 800 ma	170°	11	
1N348	100	400 ma	15A	5 ma	2V @ 800 ma	170°	11	
1N336	200	400 ma	15A	1 ma	2V @ 800 ma	170°	11	
1N345	200	400 ma	15A	5 ma	2V @ 800 ma	170°	11	
1N334	300	400 ma	15A	2 ma	2V @ 800 ma	170°	11	
1N343	300	400 ma	15A	5 ma	2V @ 800 ma	170°	11	
1N332	400	400 ma	15A	2 ma	2V @ 800 ma	170°	11	
1N341	400	400 ma	15A	5 ma	2V @ 800 ma	170°	11	
1N562	800	400 ma†	15A	3 ma	.65V @ 150°C	150°	11	1N560-61 mounted on studs.
1N563	1000	400 ma†	15A	3 ma	.65V @ 150°C	150°	11	Popular model.

†at 100°C Case.
*Military Approved units also available.

Silicon Low Current Rectifier Cells (Stud Mounted)

JEDEC or GE Type Number	PRV	Max. I_{DC} @ T°C	Max. Peak 1 cycle Surge	Max. Rev. Cur. (Full cycle Av.)	Max. Full Load Voltage Drop	Max. Oper. °C	Outline No.	COMMENTS
		@ 100° Amb.		@ 25°C				
1N550	100	500 ma	4A, 3 ms	.5 μa	1.5V @ 25°C	150°	11	Very low leakage for magnetic amplifier applications. The 1N440B-5B series mounted on studs.
1N551	200	500 ma	4A, 3 ms	1.0 μa	1.5V @ 25°C	150°	11	
1N552	300	500 ma	4A, 3 ms	1.5 μa	1.5V @ 25°C	150°	11	
1N553	400	500 ma	4A, 3 ms	2.5 μa	1.5V @ 25°C	150°	11	
1N554	500	500 ma	4A, 3 ms	3.5 μa	1.5V @ 25°C	150°	11	
1N555	600	500 ma	4A, 3 ms	5.0 μa	1.5V @ 25°C	150°	11	
		@ 135° Case		@ 135°C				Refer also to 1N1115-1120 Specification Sheet.
1N254*	190	400 ma	15A	.1 ma	1.5V @ 500 ma	150°	11	
1N255*	380	400 ma	15A	.15 ma	1.5V @ 500 ma	150°	11	
		@ 100° Amb.		@ 25°C	@ 25°C			
1N607	50	1A	2A, .1 sec	.025 ma	1.5V @ 200 ma	150°	11	Refer also to 1N1115-1120 Specification Sheet, and the 1N550-5 Specification Sheet.
1N607A	50	1A	2A, .1 sec	.001 ma	1.5V @ 200 ma	150°	11	
1N608	100	1A	2A, .1 sec	.025 ma	1.5V @ 200 ma	150°	11	
1N608A	100	1A	2A, .1 sec	.001 ma	1.5V @ 200 ma	150°	11	
1N609	150	1A	2A, .1 sec	.025 ma	1.5V @ 200 ma	150°	11	
1N609A	150	1A	2A, .1 sec	.001 ma	1.5V @ 200 ma	150°	11	
1N610	200	1A	2A, .1 sec	.025 ma	1.5V @ 200 ma	150°	11	
1N610A	200	1A	2A, .1 sec	.001 ma	1.5V @ 200 ma	150°	11	
1N611	300	1A	2A, .1 sec	.025 ma	1.5V @ 200 ma	150°	11	
1N611A	300	1A	2A, .1 sec	.001 ma	1.5V @ 200 ma	150°	11	
1N612	400	1A	2A, .1 sec	.025 ma	1.5V @ 200 ma	150°	11	
1N612A	400	1A	2A, .1 sec	.0015 ma	1.5V @ 200 ma	150°	11	
1N613	500	1A	2A, .1 sec	.025 ma	1.5V @ 200 ma	150°	11	
1N613A	500	1A	2A, .1 sec	.002 ma	1.5V @ 200 ma	150°	11	
1N614	600	1A	2A, .1 sec	.025 ma	1.5V @ 200 ma	150°	11	
1N614A	600	1A	2A, .1 sec	.0025 ma	1.5V @ 200 ma	150°	11	

Silicon Low Current Rectifier Cells (Stud Mounted)

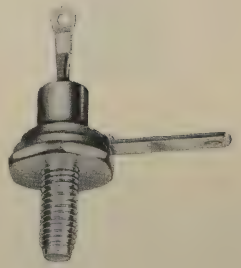
JEDEC or GE Type Number	PRV	Max. I_{DC} @ T°C	Max. Peak 1 cycle Surge	Max. Rev. Cur. (Full cycle Av.)	Max. Full Load Voltage Drop	Max. Oper. °C	Outline No.	COMMENTS
		@ 85° Case		@ 150°C				
1N1115	100	1.5A	15A	.4 ma	.65V @ 150°C	170°	11	The popular line. 1N536-40,
1N1116	200	1.5A	15A	.3 ma	.65V @ 150°C	170°	11	1N547, 1N1095-6 mounted
1N1117	300	1.5A	15A	.3 ma	.65V @ 150°C	170°	11	on studs.
1N1118	400	1.5A	15A	.3 ma	.65V @ 150°C	170°	11	
1N1119	500	1.3A	15A	.3 ma	.65V @ 150°C	155°	11	
1N1120	600	1.3A	15A	.3 ma	.65V @ 150°C	155°	11	
		@ 135° Case		@ 135°C				Refer also to 1N1115-1120
1N253*	95	1A	4A, 3 ms	.1 ma	1.5V @ 1A	150°	11	Specification Sheet.

†at 100°C Case.
*Military Approved units also available.

Silicon Low Current Rectifier Cells (Insulated Stud)

Up to 1.5 Amps — *Up to 600 PRV*

JEDEC or GE Type Number	PRV	Max. I_{DC} at T°C	Max. Peak 1 cycle Surge	Max. Rev. Cur. (Full cycle Av.)	Max. Full Load Voltage Drop	Max. Oper. °C	Outline No.	COMMENTS
		@ 50°C Case		@ 120°C	@ 120°C			
1N2851	500	1.5 Amps	15 Amps	.3 ma	.65V	150°	12	
1N2852	600	1.5 Amps	15 Amps	.3 ma	.65V	150°	12	Identical to the
		@ 75°C Case		@ 150°C	@ 150°C			1N1115-1N1120 series
1N2847	100	1.5 Amps	15 Amps	.4 ma	.65V	165°	12	except the stud is electrically
1N2848	200	1.5 Amps	15 Amps	.3 ma	.65V	165°	12	insulated from the junction.
1N2849	300	1.5 Amps	15 Amps	.3 ma	.65V	165°	12	
1N2850	400	1.5 Amps	15 Amps	.3 ma	.65V	165°	12	



Silicon Medium Current Rectifier Cells
Up to 25 Amps

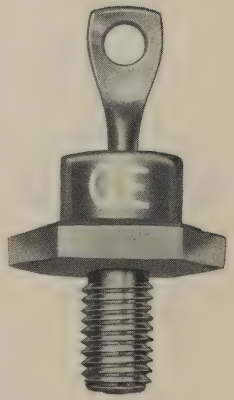
Up to 600 PRV

JEDEC or GE Type Number	Repetitive PRV	Transient PRV	Max. I_{DC} @ 145°C Stud Single Phase	Max. Peak 1 cycle Surge	Max. Rev. Cur. (Full cycle Av. @ Full load)	Max. Full Load Voltage Drop	Max. Oper. °C	Outline No.	COMMENTS
					@ 150°C Stud	@ 150°C Stud			
1N1341A	50	100	6A	150A	3 ma	.64V	200°	13	
1N1342A	100	200	6A	150A	2.5 ma	.64V	200°	13	
1N1343A	150	300	6A	150A	2.25 ma	.64V	200°	13	
1N1344A	200	350	6A	150A	2.0 ma	.64V	200°	13	
1N1345A	300	450	6A	150A	1.75 ma	.64V	200°	13	
1N1346A	400	600	6A	150A	1.5 ma	.64V	200°	13	
1N1347A	500	700	6A	150A	1.25 ma	.64V	200°	13	
1N1348A	600	800	6A	150A	1.0 ma	.64V	200°	13	
1N1199A	50	100	12A	240A	3 ma	.55V	200°	13	
1N1200A	100	200	12A	240A	2.5 ma	.55V	200°	13	
1N1201A	150	300	12A	240A	2.25 ma	.55V	200°	13	Designed for use in the 2 to 30
1N1202A	200	350	12A	240A	2.0 ma	.55V	200°	13	ampere range. High junction
1N1203A	300	450	12A	240A	1.75 ma	.55V	200°	13	temperature rating and
1N1204A	400	600	12A	240A	1.5 ma	.55V	200°	13	extremely low forward voltage
1N1205A	500	700	12A	240A	1.25 ma	.55V	200°	13	drop and thermal impedance
1N1206A	600	800	12A	240A	1.0 ma	.55V	200°	13	permit high current
						25°C T_J			operation with minimum
1N248	50		10A	200A	5 ma	1.5V*	175°	14	space requirements. May be
1N249	100		10A	200A	5 ma	1.5V*	175°	14	mounted directly to a chassis
1N250	200		10A	200A	5 ma	1.5V*	175°	14	or fin or may be insulated
1N248A	50		20A	350A	5 ma	1.5V**	175°	14	by using insulating kit
1N249A	100		20A	350A	5 ma	1.5V**	175°	14	provided. All units are also
USA-1N249B	100		20A	250A	5 ma	1.5V**	175°	14	available with negative polarity (stud is anode).

Silicon Medium Current Rectifier Cells

JEDEC or GE Type Number	Repetitive PRV	Transient PRV	Max. I_{DC} @ 145°C Stud Single Phase	Max. Peak 1 cycle Surge	Max. Rev. Cur. (Full cycle Av. @ Full load)	Max. Full Load Voltage Drop	Max. Oper. °C	Outline No.	COMMENTS
USA-									Designed for use in the 2 to 30 ampere range. High junction temperature rating and extremely low forward voltage drop and thermal impedance permit high current operation with minimum space requirements. May be mounted directly to a chassis or fin or may be insulated by using insulating kit provided. All units are also available with negative polarity (stud is anode).
1N250B	200		20A	250A	5 ma	1.5V**	175°	14	
1N250A	200		20A	350A	5 ma	1.5V**	175°	14	
USA-									
1N2135A	400		20A	250A	40 ma @ 145°C Stud	1.5V @ 145°C Stud	150°	14	
1N2154	50	100	25A	400A	5 ma	0.6V	200°	14	
1N2155	100	200	25A	400A	4.5 ma	0.6V	200°	14	
1N2156	200	350	25A	400A	4.0 ma	0.6V	200°	14	
1N2157	300	450	25A	400A	3.5 ma	0.6V	200°	14	
1N2158	400	600	25A	400A	3.0 ma	0.6V	200°	14	
1N2159	500	700	25A	400A	2.5 ma	0.6V	200°	14	
1N2160	600	800	25A	400A	2.0 ma	0.6V	200°	14	

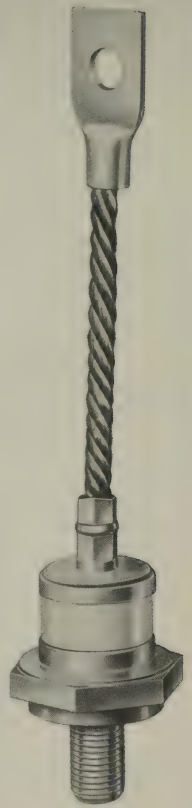
*@ 25A **@ 50A



Silicon High Current Rectifier Cells Up to 100A

Up to 1000 PRV

JEDEC or GE Type Number	Repetitive PRV	Transient PRV	Max. I_{DC} @ 130°C Stud Single Phase	Max. 1 Cycle Surge	Max. Instant. Leakage 1 at Rated PRV (milliamps.)	Max. Forward Voltage Drop @ 70A DC Single Phase 150°C	Max. Oper. Temp. °C	Outline No.	COMMENTS
1N3289	200	300	100A	1600A	24	.45V	200°C	15	Large area junction rectifiers for applications requiring d-c output as high as 100 amps per rectifying element at rms input voltages up to 700 Volts. The 1N3289—1N3295 is a "double diffused, all hard solder rectifier," which has high surge current capabilities and is highly resistant to thermal fatigue. Versatility is further increased by the availability of reverse polarity (stud is anode) units, designated by the suffix R, (IN3289R—1N3295R)
1N3290	300	400	100A	1600A	24	.45V	200°C	15	
1N3291	400	525	100A	1600A	24	.45V	200°C	15	
1N3292	500	650	100A	1600A	21	.45V	200°C	15	
1N3293	600	800	100A	1600A	17	.45V	200°C	15	
1N3294	800	1000	100A	1600A	13	.45V	200°C	15	
1N3295	1000	1300	100A	1600A	11	.45V	200°C	15	



These General Electric Silicon and Germanium Rectifiers Meet Military Specifications

Type	Military Specification	Single Phase Max. Ratings		Outline No.
		PRV	I_{DC} @ Temp.	
Germanium				
USN 1N93	MIL-E-1/895	300 Volts	75 ma @ 55°C amb.	8
USAF 1N315	MIL-E-1/1088	100 Volts	100 ma @ 71°C amb.	8
Silicon				
USA 1N249B	MIL-E-19500/134	125 Volts	20 A @ 150°C case	14
USA 1N250B		250 Volts	20 A @ 150°C case	14
JAN 1N253	MIL-E-1/1024A	100 Volts	1 A @ 135°C case	11
JAN 1N254	MIL-E-1/989B	200 Volts	400 ma @ 135°C case	11
JAN 1N255	MIL-E-1/990B	400 Volts	400 ma @ 135°C case	11
JAN 1N256	MIL-E-1/991B	600 Volts	200 ma @ 135°C case	11
JAN 1N538	MIL-E-1/1084A	240 Volts	250 ma @ 150°C amb.	8
USAF 1N538	MIL-E-1/1089	200 Volts	250 ma @ 150°C amb.	8
JAN 1N540	MIL-E-1/1085A	480 Volts	250 ma @ 150°C amb.	8
USAF 1N540	MIL-E-1/1089	400 Volts	250 ma @ 150°C amb.	8
JAN 1N547	MIL-E-1/1083A	720 Volts	250 ma @ 150°C amb.	8
USAF 1N547	MIL-E-1/1089	600 Volts	250 ma @ 150°C amb.	8
USA 1N2135A	MIL-S-195000/134	500 Volts	20 A @ 150°C case	14

SILICON AVALANCHE (ZENER) DIODES CONDENSED SPECIFICATIONS

These 1 watt Avalanche (Zener) Diodes utilize the 1N536 top hat package. The design incorporates know-how which assures very good voltage regulation, and voltage stability over a long period of time under the severest environmental conditions. Complete specifications are available upon request.

RATING TABLE

General Electric Type Number	Electrical Equivalent	V_{ZT} @ I_{ZT} ZENER VOLTAGE Volts @ 25°C Nominal	Test Current I_{ZT} mA	Maximum Dynamic Impedance Z_{ZT} @ I_{ZT} @ 25°C Ohms	Typical Voltage Regulation ΔV_Z Volts	MAXIMUM ZENER CURRENT I_{ZM}—MA T_A=50°C Maximum	Outline No.
4JZ4X5.1B	—	5.1	100	7.0	0.11	160	8
4JZ4X5.6B	1N1765	5.6	100	1.2	0.14	150	8
4JZ4X6.2B	1N1766	6.2	100	1.5	0.16	130	8
4JZ4X6.8B	1N1767	6.8	100	1.7	0.20	120	8
4JZ4X7.5B	1N1768	7.5	100	2.1	0.24	109	8
4JZ4X8.2B	1N1769	8.2	100	2.4	0.28	100	8
4JZ4X9.1B	1N1770	9.1	50	3.0	0.34	90	8
4JZ4X10B	1N1771	10.0	50	3.5	0.41	82	8
4JZ4X11B	1N1772	11.0	50	4.2	0.48	74	8
4JZ4X12B	1N1773	12.0	50	5.0	0.57	68	8
4JZ4X13B	1N1774	13.0	50	5.8	0.66	63	8
4JZ4X14B	—	14.0	50	6.6	0.75	58	8
4JZ4X15B	1N1775	15.0	50	7.6	0.86	54	8
4JZ4X16B	1N1776	16.0	50	8.6	0.97	51	8

NOTE: Standard types are supplied to the ±10% of voltage values listed. For 5% tolerance, Change B suffix to A suffix in GE Type Number (i.e., 4JZ4X5.1A).

SCR AND UNIJUNCTION
OUTLINE DRAWINGS

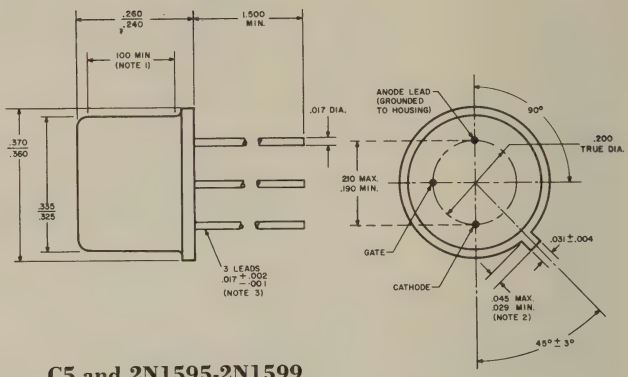
1

NOTE 1: THIS ZONE IS CONTROLLED FOR AUTOMATIC HANDLING. THE VARIATION IN ACTUAL DIAMETER WITHIN THIS ZONE SHALL NOT EXCEED .010.

NOTE 2: MEASURED FROM MAX. DIAMETER OF THE ACTUAL DEVICE.

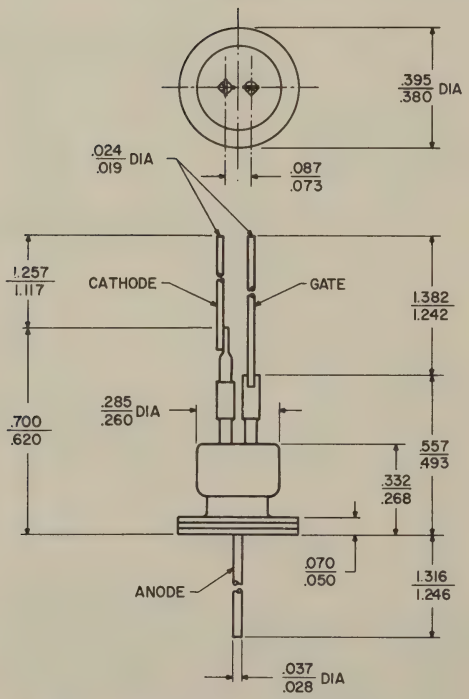
NOTE 3: THE SPECIFIED LEAD DIAMETER APPLIES IN THE ZONE BETWEEN .050 AND .250 FROM THE BASE SEAT. BETWEEN .250 AND 1.5 MAXIMUM OF .021 DIAMETER IS HELD. OUTSIDE OF THESE ZONES THE LEAD DIAMETER IS NOT CONTROLLED. LEADS MAY BE INSERTED, WITHOUT DAMAGE, IN .031 HOLES WHILE DEVICE ENTERS .371 HOLE CONCENTRIC WITH LEAD HOLE CIRCLE.

APPROX WEIGHT: .05 OZ
ALL DIMENSIONS IN INCHES



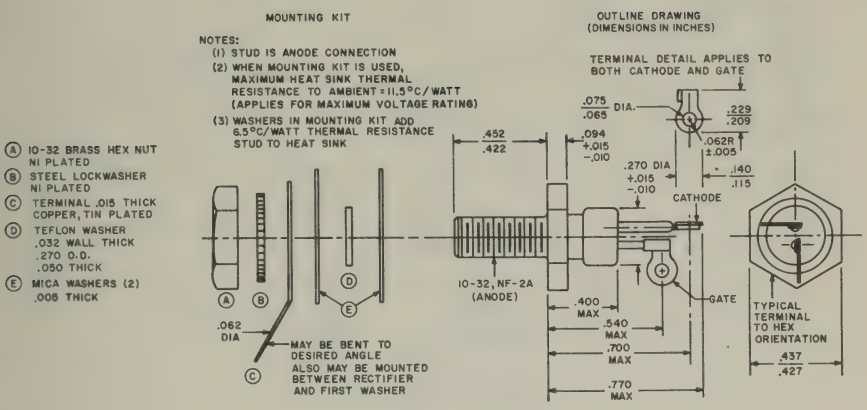
C5 and 2N1595-2N1599

2



2N1927-2N1935 (C8) and C9

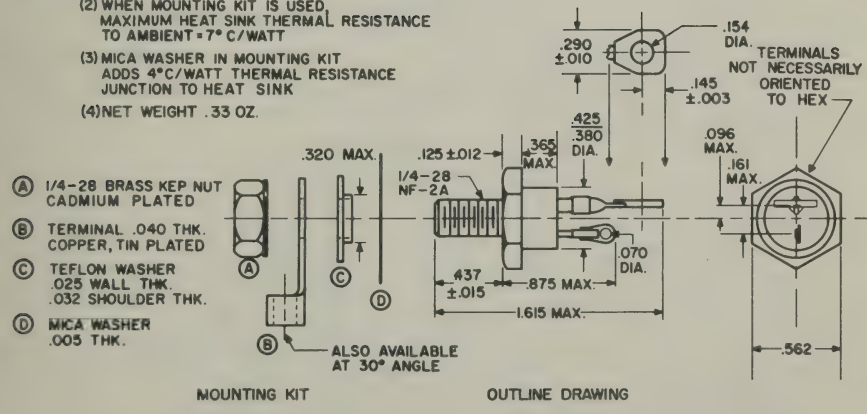
3


MOUNTING KIT
NOTES:
(1) STUD IS ANODE CONNECTION
(2) WHEN MOUNTING KIT IS USED, MAXIMUM HEAT SINK THERMAL RESISTANCE TO AMBIENT = 11.5°C/WATT (APPLIES FOR MAXIMUM VOLTAGE RATING)
(3) WASHERS IN MOUNTING KIT ADD 6.5°C/WATT THERMAL RESISTANCE STUD TO HEAT SINK
(A) 10-32 BRASS HEX NUT NI PLATED
(B) STEEL LOCKWASHER NI PLATED
(C) TERMINAL .015 THICK COPPER, TIN PLATED
(D) TEFLON WASHER .032 WALL THICK .270 O.D. .050 THICK
(E) MICA WASHERS (2) .006 THICK
.062 DIA
MAY BE BENT TO DESIRED ANGLE ALSO MAY BE MOUNTED BETWEEN RECTIFIER AND FIRST WASHER
OUTLINE DRAWING (DIMENSIONS IN INCHES)
TERMINAL DETAIL APPLIES TO BOTH CATHODE AND GATE
.075 .065 DIA.
.229 .209
.062R ±.005
.140 .115
.270 DIA +.015 -.010
CATHODE
GATE
.452 .422
.094 +.015 -.010
10-32, NF-2A (ANODE)
.400 MAX
.540 MAX
.700 MAX
.770 MAX
TYPICAL TERMINAL TO HEX ORIENTATION
.437 .427

2N1770-2N1777 (C11)
2N1770A-2N1777A (C10)
C12

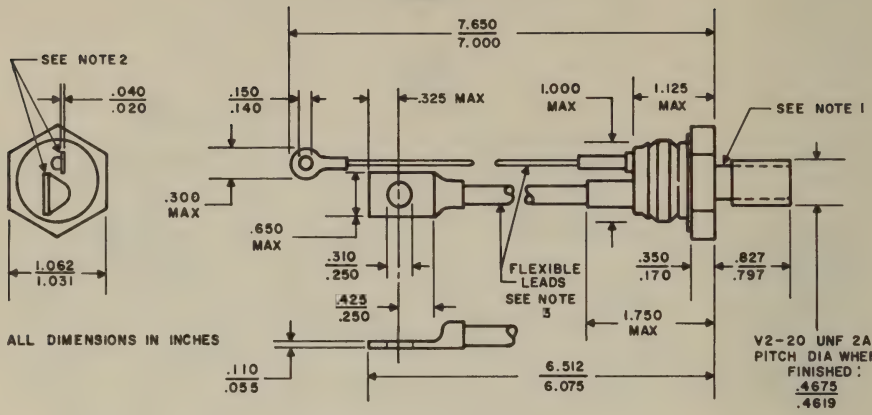
4

NOTES: (1) STUD IS ANODE CONNECTION
(2) WHEN MOUNTING KIT IS USED, MAXIMUM HEAT SINK THERMAL RESISTANCE TO AMBIENT = 7° C/WATT
(3) MICA WASHER IN MOUNTING KIT ADDS 4°C/WATT THERMAL RESISTANCE JUNCTION TO HEAT SINK
(4) NET WEIGHT .33 OZ.



2N1842-2N1850 (C36)
2N681-2N689 (C35)
C40

5



2N1909-2N1916 (C50)
C55
2N2023-2N2030 (C60)

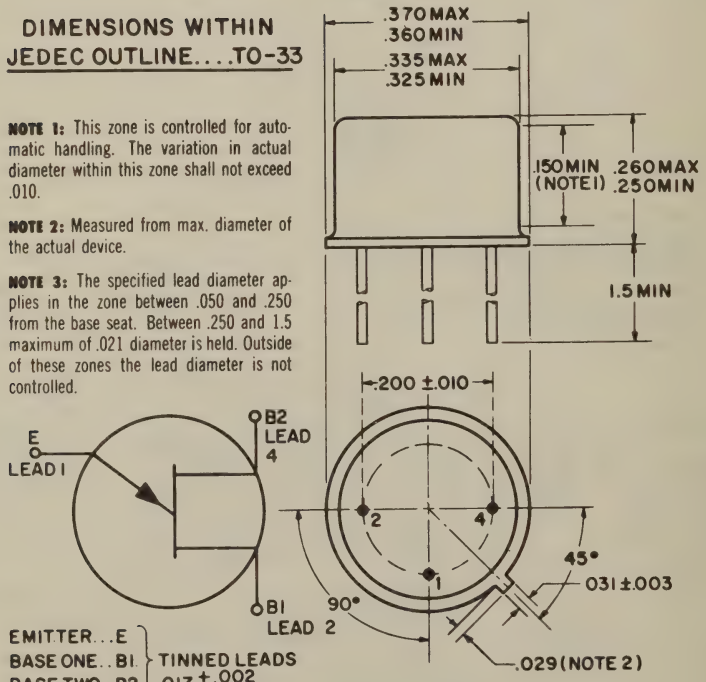
6

DIMENSIONS WITHIN JEDEC OUTLINE....TO-33

NOTE 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed .010.

NOTE 2: Measured from max. diameter of the actual device.

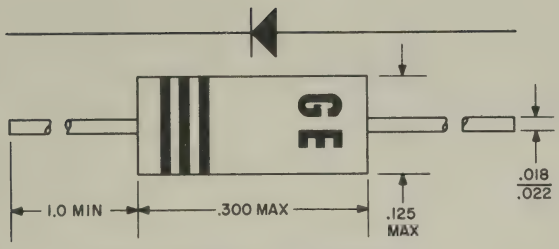
NOTE 3: The specified lead diameter applies in the zone between .050 and .250 from the base seat. Between .250 and 1.5 maximum of .021 diameter is held. Outside of these zones the lead diameter is not controlled.



2N1671, 2N1671A, 2N1671B

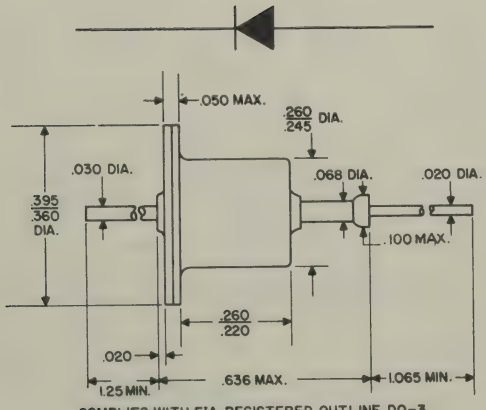
OUTLINE DRAWINGS

7



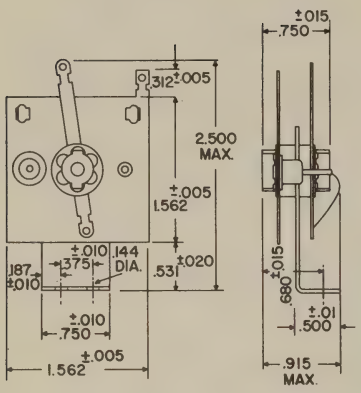
NOTES: 1. JEDEC COLOR CODED BANDS
DENOTE CATHODE END
2. UNIT WEIGHT — .25 GMS

8

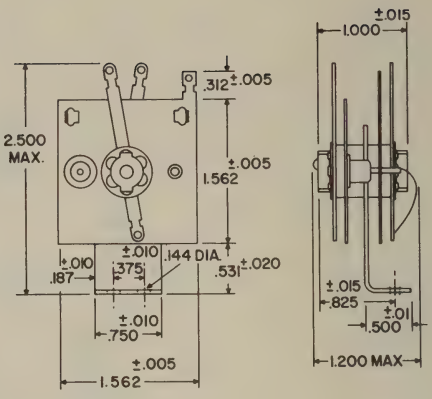


COMPLIES WITH EIA REGISTERED OUTLINE DO-3
APPROX. WEIGHT = .05 OZ.

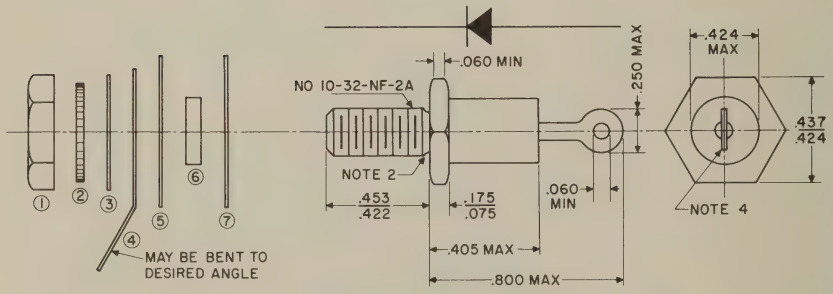
9



10



11



① 10-32 BRASS NI. PL. HEX. NUT

② LOCK WASHER (EXT.) STEEL NI. PL.

③ FLAT WASHER 7/16" O.D. .004 THK.

④ TERMINAL: .010 THK. COPPER TIN PL.

⑤ MICA WASHER .005 THK.

⑥ TEFLON WASHER .032 WALL THK.

⑦ MICA WASHER .005 THK.

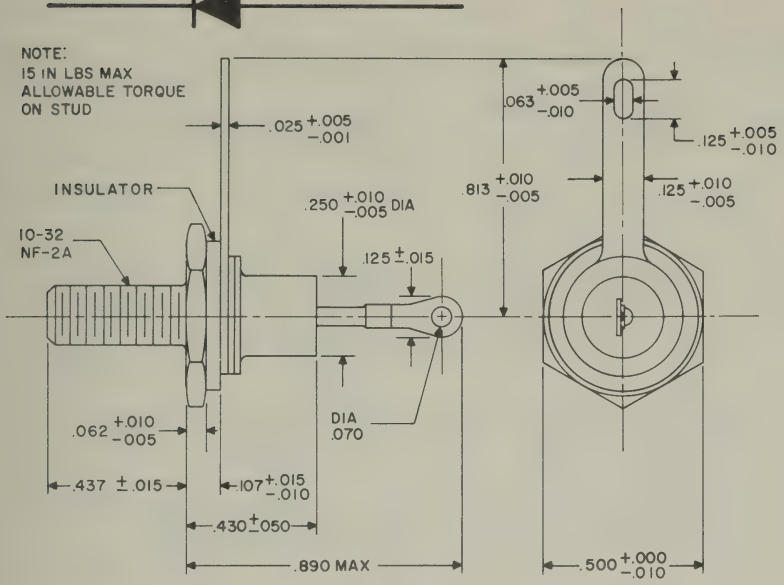
NOTES:

1. UNIT MUST NOT BE DAMAGED BY TORQUE OF 15 IN. LB. APPLIED TO 10-32-NF-2B NUT ASSEMBLED ON THREAD.
2. DIA. OF UNTHREADED PORTION .189 MAX. AND .169 MIN.
3. COMPLETE THREADS TO EXTEND TO WITHIN 2 1/2 THREADS OF HEAD.
4. ANGULAR ORIENTATION OF THIS TERMINAL IS UNDEFINED.
5. MAXIMUM PITCH DIAMETER OF PLATED THREADS SHALL BE BASIC PITCH DIAMETER (.1697) REFERENCE SCREW THREAD STANDARD FOR FEDERAL SERVICES 1957 HANDBOOK H28 1957 PI.

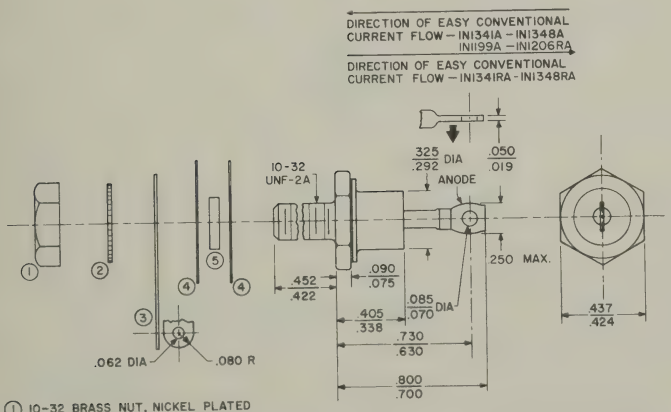
COMPLIES WITH EIA REGISTERED OUTLINE DO-4

APPROX WEIGHT = .15 OZ

12



13



① 10-32 BRASS NUT, NICKEL PLATED

② LOCKWASHER, NICKEL PLATED STEEL

③ COPPER TERMINAL, .016 THICK, TIN PLATED

④ MICA WASHERS, TWO, .625 OD, .204 ID, .005 THICK

⑤ TEFLON WASHER, .270 OD, .204 ID, .050 THICK

COMPLIES WITH
EIA REGISTERED OUTLINE DO-4

NOTES: (1) UNIT WEIGHT — .25 OZ
(2) MICA WASHER IN MOUNTING KIT MAY ADD APPROX 6.5°C/WATT THERMAL RESISTANCE STUD TO HEAT SINK

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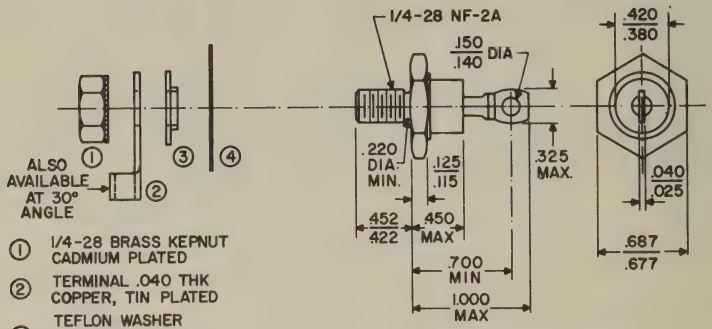
NOTE: MICA WASHER IN MOUNTING KIT MAY ADD UP TO 2.5°C/WATT THERMAL RESISTANCE STUD TO AMBIENT
UNIT WEIGHT .5 OZ.

DIRECTION OF EASY CONVENTIONAL CURRENT FLOW
IN2154–IN2160; IN248A–IN250A; IN248B–IN250B

DIRECTION OF EASY CONVENTIONAL CURRENT FLOW
IN2154R–IN2160R; IN248R–IN250R
IN248RA–IN250RA; IN248RB–IN250RB



① 1/4-28 BRASS KEPNUT CADMIUM PLATED

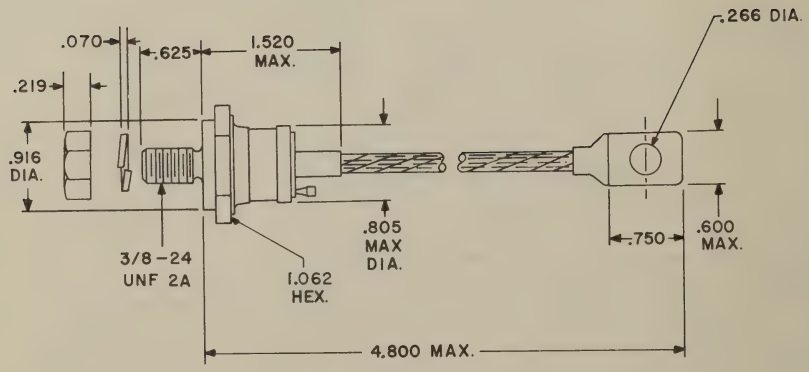
② TERMINAL .040 THK COPPER, TIN PLATED

③ TEFLON WASHER .025 WALL THK. .032 SHOULDER THK.

④ MICA WASHER .005 THK.

COMPLIES WITH EIA REGISTERED OUTLINE DO-5

15



CONFORMS TO JEDEC OUTLINE DO-8

APPLICATION AND SPECIFICATION LITERATURE

The following literature provides considerably greater detail on the foregoing application data and specifications on silicon controlled rectifiers. Single copies may be secured upon request to: Dept. SCRM

Advertising & Sales Promotion
Rectifier Components Dept.
General Electric Company
Auburn, New York

APPLICATION NOTES

Publication Number	Title
200.1	"Characteristics of Common Rectifier Circuits"
200.2	"Rectifier Selection Chart"
200.3	"Controlled Rectifiers and Radio Interference"
200.4	"Universal Motor Speed Controls"
200.5	"General Electric Selenium Thyrector Diodes: Transient Voltage Suppressors"
200.6	"Silicon Controlled Rectifier High Voltage Power Supply"
200.7	"Voltage Regulated SCR Inverter with Sinewave Output and Current Limiting"
200.8	"Accommodating Inrush Current with Silicon Controlled Rectifiers"
200.9	"Power Semiconductor Ratings Under Transient and Intermittent Loads"
200.10	"Overcurrent Protection of Semiconductor Rectifiers"
200.11	"Rectifier Voltage Transients: Their Generation, Detection and Reduction"
200.12	"Heatsinks for Stud Mounted Semiconductors"
200.13	"Thermal Fatigue and the G. E. 1N2154-60 Medium Current Silicon Rectifier"
200.14	"The Silicon Controlled Rectifier in Lamp Dimming and Heating Control Service"
200.15	"Turn-off Time Characterization and Measurement of Silicon Controlled Rectifiers"
200.16	"A Portable Transient Voltage Indicator for Semiconductor Circuits"
200.17	"Test Circuits for Silicon and Germanium Rectifiers"
200.18	"A Simple Firing Circuit for a Three-Phase SCR Bridge"
200.19	"The General Electric C5—A Low Current SCR with Unique New Usages"
200.20	"The General Electric 1N3289-95 (4JA70 series) High Current Rectifier"
640.1	"G-E Semiconductor Rectifier Components Guide" (50 cents)

SPECIFICATION SHEETS

150.10 C5 (A-U)
150.12 C8—2N1929-35
150.15 2N1595-99
150.20 C10 (A-U)—2N1770A-77A
150.21 C11 (A-U)—2N1770-77
160.20 C35—2N681-89
160.21 C36 (A-U)—2N1842-50
160.25 C40 (A-U)
170.1 C52 (A-U) and 2N1792-98
170.20 C50 (A-U)—2N1909-16
170.21 C55 (A-U)
170.26 C60—2N2023-30, and C61

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APPLICATION INDEX

The circuits referred to in the following figure numbers are intended as a starting point for the equipment designer in achieving the detailed requirements of his application. Since these circuits are not necessarily "ultimate" for every application, it is hoped the imaginative designer will use them simply as a jumping-off point for his own development. Likewise, many of these circuits can be used for other functions besides those mentioned in the text. As a guide to some of the various SCR circuits for accomplishing specific tasks, here is a tabulation of diagrams used in this manual:

Applications	For Basic Circuit Possibilities See Figure Number
AC Regulated Supplies	4.29, 8.2, 8.3, 8.4, 8.7, 9.26, 9.28, 9.34, 9.38, 9.42 9.47
AC Static Switches	4.7, 4.10, 7.1, 7.2, 7.5, 8.2
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